IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SENTIENT SENSORS, LLC, Plaintiff, v. XILINX INCORPORATED, Defendant.	**Civil Action No._____** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

This is an action for patent infringement in which Plaintiff Sentient Sensors, LLC ("Sentient" or "Plaintiff") by and for its Complaint against Defendant Xilinx Incorporated ("Xilinx" or "Defendant") hereby makes the following allegations:

THE PARTIES

1. Sentient Sensors, LLC is a New Mexico Limited Liability Company, with its principal place of business at 6022 Constitution Ave. NE, Albuquerque, New Mexico.

2. Sentient was founded by inventor and entrepreneur Kenneth Blemel. Mr. Blemel has been operating in Albuquerque, New Mexico for over 30 years. Mr. Blemel, an engineer by training and vocation, has developed numerous technologies in the areas of programmable logic devices, instrumentation and embedded systems over his long career. Mr. Blemel has successfully guided multiple research and development programs in several electronic hardware sub- disciplines, including the R&D program culminating in the issuance of the patent described herein.

3. Xilinx Incorporated is a Delaware corporation with its principal place of business at 2100 Logic Guide, San Jose, California 95124. Xilinx may be served through its registered agent The Corporation Trust Company, Trust Corporation Center, 1209 Orange St., New Castle, Delaware 19801.

4. Xilinx is registered to do business in the State of Delaware and has been since at least September 15, 2000.

JURISDICTION AND VENUE

5. This is an action for patent infringement arising under 35 U.S.C. §100, et seq., §§ 271-81, and §§ 284-85, among others.

6. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

7. Venue is proper in this judicial district pursuant to 28 U.S.C. § 1400(b). According to public records, Xilinx is a corporation organized under the laws of the State of Delaware, and therefore resides in this judicial district. Further, upon information and belief, Xilinx maintains a regular and established place of business within this district and has committed acts of infringement within this judicial district by selling the accused instrumentalities here.

8. Personal jurisdiction over Xilinx is proper in this district because Xilinx resides in this judicial district and transacts business from this district, including infringing activities, and also targets customers within this district for its infringing products, such that the Court's exercise of personal jurisdiction would not offend traditional notions of fair play and substantial justice. *See, e.g., WSOU Investments LLC d/b/a Brazos Licensing and Development v. Xilinx, Inc.*, C.A. No. 20-cv-01228, Answer (DI 41) at Paragraphs 5-6 (D. Del. Jn. 22, 2021) (admitting this district has personal jurisdiction over Xilinx and noting that Xilinx is not challenging venue as improper).

BACKGROUND

9. This lawsuit asserts causes of action for infringement of United States Patent No. 6,938,177 (the ’177 Patent). A true and correct copy of the ’177 patent is attached hereto as Exhibit A.

10. The ’177 Patent was properly assigned to Sentient Sensors, LLC, and Sentient Sensors, LLC has all rights, title, and interest in and to the ’177 Patent and to any and all other future inventions that disclose and claim improvements over the subject matter disclosed, including the right to sue for and recover or otherwise collect damages in respect of past acts of infringement thereof.

11. The inventions described and claimed in the ’177 Patent have been used to provide instrumentation for monitoring and control of systems and components of instruments, aircraft, ships, homes, and machinery. A few examples include:

- Monitoring signals on UH-60 helicopters
- Instrumentation for prognostic health monitoring of aircraft propulsion systems
- Instrumentation interface to paired flight data recorders
- Instrumentation monitoring health signatures of aircraft propulsion systems
- Instrumentation for monitoring and control of diesel generator sets
- Instrumentation for monitoring health of ballistic missiles
- Instrumentation of hybrid micro-grids
- Edge node flight data collection and analysis for B-52 and other military aircraft.

12. The teachings of the ’177 Patent enable the rapid prototyping and deployment of complex hardware and software platforms, providing enhanced flexibility for various real-world applications. As just one example, the ’177 Patent describes and claims an instrument controller including a microprocessor for controlling inputs and outputs, logic gates arranged in a manner consistent with a field programmable gate array (“FPGA”) that can be used as a freely re-configurable parallel processor, and a real-time clock for time-stamping of data before it is

stored in non-volatile memory, all of which contribute to the creation of a customizable development platform that allows for a wide range of hardware controller solutions.

13. At the time of the filing of the ’177 Patent application, the technology described and claimed in that application provided for a novel and innovative in-field control and monitoring system with time-stamped selectable collection and digitizing of analog and digital data streams. The technology described and claimed in the application for the ’177 Patent enabled, inter alia, real-time concurrent processing of data to measure and control stresses on components and to generate alerts for anomalous conditions. The use of programmable logic-based “system on a chip” and “network on a chip” instrument controllers is now widespread with diverse applications, including computer-based system control in general, machinery control, field programmable automation of process lines, telecommunications, and diagnostic and prognostic health monitoring of equipment.

14. The research and development program that led to the innovations described and claimed in the ’177 Patent was funded in part by the U.S. Air Force and conducted at Kirtland Air Force base in Albuquerque, New Mexico. These advancements were initially directed toward use in the Strategic Defense Initiative program initiated in the 1980s, colloquially known at the time as “Star Wars.” As a result of a collaborative research and development agreement (“CRADA”) with the U.S. government, the Air Force secured a license to practice the inventions of the ’177 Patent. Hardware purveyors such as Xilinx have adapted the inventions of the ’177 Patent for their own commercial exploitation, for example, as automotive control devices, and are used for controllers of a wide array of electronic devices.

15. The requirements of 35 U.S.C. § 287(a) have been met with respect to the ’177 patent.

16. Xilinx was put on actual notice of its infringement of the ’177 Patent through

numerous written communications beginning on December 21, 2016 through June 15, 2017 including to Moshe Gavrielov, Xilinx CEO and Justin Liu, Director of Intellectual Property at Xilinx.

17. Upon information and belief, Xilinx's infringement of the '177 Patent has been, and continues to be, willful.

18. At least as early as the 2016 notification date, Xilinx had knowledge of the '177 Patent, which is entitled to a statutory presumption of validity under 35 U.S.C. §282. Sentient intends to seek discovery on the issue of willfulness and reserves the right to seek a willfulness finding and treble damages under 35 U.S.C. § 284, as well as its attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT I
Direct Infringement of the '177 Patent

19. Sentient incorporates by reference the allegations set forth in the preceding paragraphs.

20. On August 30, 2005, the '177 Patent, entitled "Multi-Chip Module Smart Controller," was duly and legally issued by the United States Patent and Trademark Office to Kenneth Blemel as the sole named inventor.

21. Sentient is the assignee and the owner of the '177 Patent, holding all rights, title, and interest in and to the '177 Patent, and Sentient has the right to sue and recover damages for infringement thereof.

22. The '177 Patent and its underlying patent application have been cited by 23 United States patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '177 Patent and its underlying patent application as relevant prior art:

- Intel Corp.
- Advanced Micro Devices (AMD)
- STM Microelectronics S.r.L.
- Trend Micro Corp.
- Benq Inc.
- Emerson Electric GmbH
- SPM Instrumentation AB
- RMT, Inc.
- NXP B.V.
- Verily Life Sciences, LLC

23. Xilinx is not licensed under the ’177 Patent, and Xilinx actively practices inventions covered by the ’177 Patent for its own profit and financial benefit.

24. Upon information and belief, Xilinx has directly infringed, and is now directly infringing, inducing infringement or contributing to infringement, either literally or under the doctrine of equivalents, at least Claim 1 of the ’177 Patent by making, using, importing, providing, supplying, distributing, selling, and offering to sell infringing products and systems, and is thus liable to Sentient for its infringement pursuant to 35 U.S.C. § 271. Xilinx’s infringing products include at least the Zynq 7000 and Zynq UltraScale series products including Zynq-based Kria products, Versal products, and development kits associated therewith (collectively referred to herein as the “’177 Xilinx Products.”).

25. For example, the ’177 Xilinx Products meet all limitations of at least Claim 1 of the ’177 Patent.

26. One or more of the Xilinx ’177 Products include an instrument controller.

1.1 Overview

The Zynq®-7000 family is based on the Xilinx® SoC architecture. These products integrate a feature-rich dual or single-core ARM® Cortex™-A9 MPCore™ based processing system (PS) and Xilinx programmable logic (PL) in a single device, built on a state-of-the-art, high-performance, low-power (HPL), 28 nm, and high-k metal gate (HKMG) process technology. The ARM Cortex-A9MPCore CPUs are the heart of the PS which also includes on-chip memory, external memory interfaces, and a rich set of I/O peripherals.

The Zynq-7000 family offers the flexibility and scalability of an FPGA, while providing performance, power, and ease of use typically associated with ASIC and ASSPs. The range of devices in the Zynq-7000 SoC family enables designers to target cost-sensitive as well as high-performance applications from a single platform using industry-standard tools. While each device in the Zynq-7000 family contains the same PS, the PL and I/O resources vary between the devices. As aresult, the Zynq-7000 SoC devices are able to serve a wide range of applications including:

- Automotive driver assistance, driver information, and infotainment
- Broadcast camera
- Industrial motor control, industrial networking, and machine vision
- IP and smart camera
- LTE radio and baseband
- Medical diagnostics and imaging
- Multifunction printers
- Video and night vision equipment

Zynq-7000 SoC Technical Reference Manual (TRM) p.26
UG585 (v1.12.2) July 1, 2018

Application Overview

Zynq UltraScale+ MPSoC is the Xilinx second-generation Zynq platform, combining a powerful processing system (PS) and user-programmable logic (PL) into the same device. The processing system features the Arm® flagship Cortex®-A53 64-bit quad-core or dual-core processor and Cortex-R5F dual-core real-time processor. In addition to the cost and integration benefits previously provided by the Zynq-7000 devices, the Zynq UltraScale+ MPSoC and RFSoC devices also provide these new features and benefits.

- Automotive driver assistance, driver information, and infotainment.
- Broadcast camera.
- Industrial motor control, industrial networking, and machine vision.
- IP and smart camera.
- LTE radio and baseband.
- Medical diagnostics and imaging.
- Multifunction printers.
- Video and night vision equipment.
- Wireless radio.

Zynq UltraScale+ Device TRM pg. 27
UG1085 (v2.2) December 4, 2020

XILINX

Versal Architecture and Product Data Sheet: Overview

DS950 (v1.14) December 9, 2021 **Advance Product Specification**

General Description

Versal™ devices are the industry's first adaptive compute acceleration platform (ACAP), combining adaptable processing and acceleration engines with programmable logic and configurable connectivity to enable customized, heterogeneous hardware solutions for a wide variety of applications in Data Center, Automotive, SG Wireless, Wired, and Defense . Versal ACAPs feature transformational features like an integrated silicon host interconnect shell and Intelligent Engines **(AI** and DSP), Adaptable Engines, and Scalar Engines, providing superior performance/watt over conventional FPGAs, CPUs, and GPUs.

The Versal AI Edge series focuses on AI performance per watt for real-time systems in automated drive, predictive factory and healthcare systems, multi-mission payloads in aerospace & defense, and a breadth of other applications. More than just AI, the Versal AI Edge series accelerates the whole application from sensor to AI to real-time control, all with the highest levels of safety and security to meet critical standards such as ISO26262 and IEC 61508.

The Versal AI Core series delivers breakthrough AI inference acceleration with AI Engines that deliver over 100x greater compute performance than current server-class of CPUs. This series is designed for a breadth of applications, including cloud for dynamic workloads and network for massive bandwidth, all while delivering advanced safety and security features. AI and data scientists, as well as software and hardware developers, can all take advantage of the high-compute density to accelerate the performance of any application.

The Versal Prime series is the foundation and the mid-range of the Versal platform, serving the broadest range of uses across multiple markets. These applications include 100G to 200G networking equipment, network and storage acceleration in the Data Center, communications test equipment, broadcast, and aerospace & defense. The series integrates mainstream 58G transceivers and optimized I/O and DDR connectivity, achieving low-latency acceleration and performance across diverse workloads.

The Versal Premium series provides breakthrough heterogeneous integration, very high-performance compute, connectivity, and security in an adaptable platform with a minimized power and area footprint. The series is designed to exceed the demands of high-bandwidth, compute-intensive applications in wired communications, data center, test & measurement, and other applications. Versal Premium series ACAPs include 112G PAM4 transceivers and integrated blocks for 600G Ethernet, 600G Interlaken, PCI Express® Gen5, and high-speed cryptography.

Versal ACAP Technical Reference Manual p. 28-29
AM011 (v1.3) October 27, 2021

27. Xilinx documentation describes one or more of the Xilinx '177 Products as including a non-volatile memory such as ROM memory and controllers for interaction with other non-volatile memory.

1.1.1 Block Diagram

Figure 1-1 illustrates the functional blocks of the Zynq-7000 SoC. The PS and the PL are on separate power domains, enabling the user of these devices to power down the PL for power management if required.

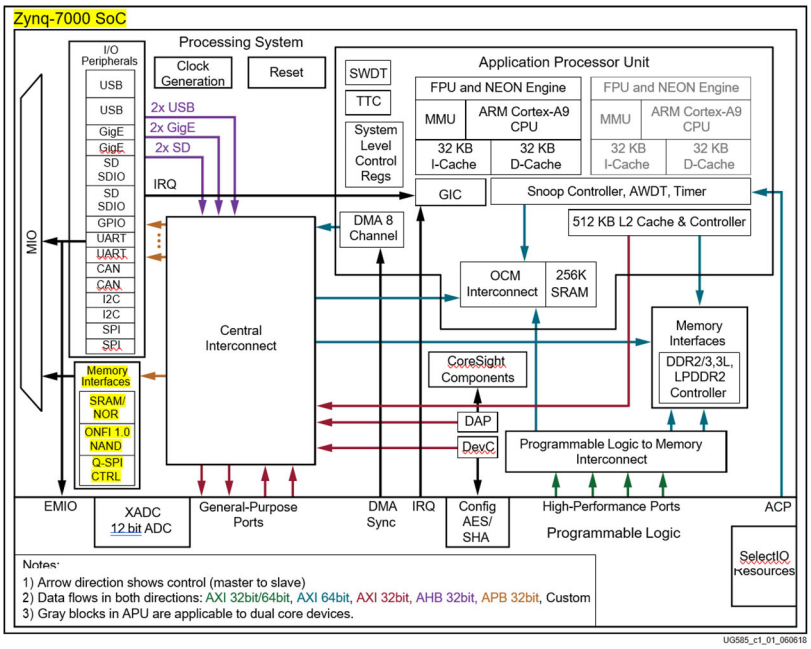

Figure 1-1: **Zynq-7000 SoC Overview**

Zynq-7000 SoC Technical Reference Manual p.26
UG585 (v1.12.2) July 1, 2018

6.1.5 BootROM Execution

The BootROM execution begins soon after a POR or non-POR reset. A POR reset causes the Hardware Boot stage to occur and then starts the BootROM execution. A non-POR reset skips the hardware stage and starts the BootROM execution almost immediately.

The BootROM executes the on-chip ROM code to perform the system boot process. The BootROM disables all access to the ROM code before transferring code execution over to the FSBL/User code. Details of how the system memory is remapped are shown in Figure 6-11, page 203.

Zynq-7000 SoC Technical Reference Manual p.26
UG585 (v1.12.2) July 1, 2018

XILINX

Zynq UltraScale+ MPSoC Data Sheet: Overview

DS891 (v1.9) May 26, 2021 **Product Specification**

General Description

The Zynq® UltraScale+™ MPSoC family is based on the Xilinx® UltraScale™ MPSoC architecture. This family of products integrates a feature-rich 64-bit quad-core or dual-core Arm® Cortex®-A53 and dual-core Arm Cortex-R5F based processing system (PS) and Xilinx programmable logic (PL) UltraScale architecture in a single device. Also included are on-chip memory, multiport external memory interfaces, and a rich set of peripheral connectivity interfaces.

PS Boot and Device Configuration

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decrypts and authenticates the images while the 4096-bit RSA block authenticates the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. The CSU executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the OCM.

External Memory Interfaces

- Multi-protocol dynamic memory controller
- 32-bit or 64-bit interfaces to DDR4, DDR3, DDR3L, or LPDDR3 memories, and 32-bit interface to LPDDR4 memory
- ECC support in 64-bit and 32-bit modes
- Up to 32GB of address space using single or dual rank of 8-, 16-, or 32-bit-wide memories
- Static memory interfaces
  - eMMC4.51 Managed NAND flash support
  - ONFI3.1 NAND flash with 24-bit ECC
  - 1-bit SPI, 2-bit SPI, 4-bit SPI (Quad-SPI), or two Quad-SPI (8-bit) serial NOR flash

Zynq UltraScale+ MPSoC Data Sheet Overview pages 2 and 39
DS891 (v1.9) May 26, 2021

Platform Management Controller

The Versal ACAP also includes the PMC. The PMC is responsible for boot, configuration, partial-reconfiguration, and other platform management tasks, such as security. The PMC includes the deeply embedded ROM code unit (RCU) for device boot and platform processing unit (PPU) that executes the platform loader and manager (PLM). The PLM also manages the processing system management (PSM) controller firmware downloads.

Versal ACAP Technical Reference Manual p. 33
AM011 (v1.3) October 27, 2021

Flash Memory Controllers

The flash memory controllers are located in the PMC and include:

- Quad SPI Controller
- Octal SPI Controller
- SD/eMMC Controllers (two in PMC)

Versal ACAP Technical Reference Manual p. 83
AM011 (v1.3) October 27, 2021

28. Xilinx documentation describes one or more of the Xilinx '177 Products as including a large volatile memory storage component such as SRAM and controllers for interaction with other volatile memory.

1.1.1 Block Diagram

Figure 1-1 illustrates the functional blocks of the Zynq-7000 SoC. The PS and the PL are on separate power domains, enabling the user of these devices to power down the PL for power management if required.

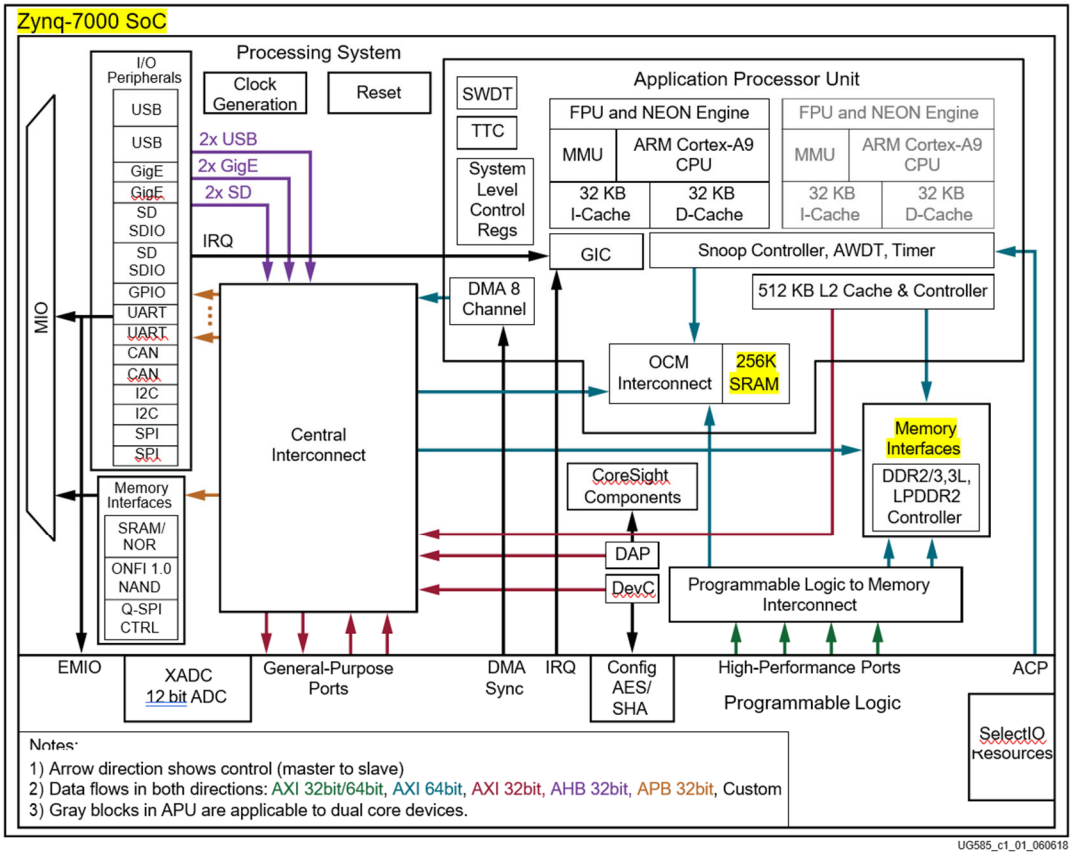

Figure 1-1: **Zynq-7000 SoC Overview**

Zynq-7000 SoC Technical Reference Manual p.26
UG585 (v1.12.2) July 1, 2018

XILINX

Zynq UltraScale+ MPSoC Data Sheet: Overview

DS891 (v1.9) May 26, 2021 **Product Specification**

General Description

The Zynq® UltraScale+™ MPSoC family is based on the Xilinx® UltraScale™ MPSoC architecture. This family of products integrates a feature-rich 64-bit quad-core or dual-core Arm® Cortex®-A53 and dual-core Arm Cortex-R5F based processing system (PS) and Xilinx programmable logic (PL) UltraScale architecture in a single device. Also included are on-chip memory, multiport external memory interfaces, and a rich set of peripheral connectivity interfaces.

On-Chip Memory

- 256KB on-chip RAM (OCM) in PS with ECC
- Up to 36Mb on-chip RAM (UltraRAM) with ECC in PL
- Up to 35Mb on-chip RAM (block RAM) with ECC in PL
- Up to 11Mb on-chip RAM (distributed RAM) in PL

External Memory Interfaces

- Multi-protocol dynamic memory controller
- 32-bit or 64-bit interfaces to DDR4, DDR3, DDR3L, or LPDDR3 memories, and 32-bit interface to LPDDR4 memory
- ECC support in 64-bit and 32-bit modes
- Up to 32GB of address space using single or dual rank of 8-, 16-, or 32-bit-wide memories
- Static memory interfaces
  - eMMC4.51 Managed NAND flash support
  - ONFI3.1 NAND flash with 24-bit ECC
  - 1-bit SPI, 2-bit SPI, 4-bit SPI (Quad-SPI), or two Quad-SPI (8-bit) serial NOR flash

Zynq UltraScale+ MPSoC Data Sheet Overview pages 1-2
DS891 (v1.9) May 26, 2021

On-Chip Memory (DCM)

In addition to the 32KB of L1 data cache, the RPU contains 256KB OCM with ECC. The OCM is accessed through two 128-bit AXI interfaces with one AXI interface dedicated to the two Cortex-RSF processors and the other AXI interface available to the APU and other masters. Memory accesses from the RPU are treated with higher priority than memory accesses through the general 128-bit AXI interface.

Some Versal ACAPs include accelerator RAM, an additional 4MB of on-chip memory with ECC located outside of the PS. This memory provides direct access from the RPU via a 128-bit AXI interface and can also be accessed from the PL through two 256-bit AXI interfaces. The memory is divided into three banks supporting concurrent read or write accesses from the PL and RPU to different banks.

UltraRAM

Dual-port UltraRAMs, each having 288K bits of storage capacity, can be configured as one 288Kb RAM. Each port can be configured as 32K x 9, 16K x 18, 8K x 36, or 4K x 72. The two ports can have different aspect ratios.

Versal Data Sheet Overview pages 19-20
DS950 (v1.14) December 9, 2021

29. Xilinx documentation describes one or more of the Xilinx '177 Products as including a processor composed of various ARM Cortex processing cores, which necessarily interface with both the volatile and non-volatile memory and memory controllers for the same.

1.1.1 Block Diagram

Figure 1-1 illustrates the functional blocks of the Zynq-7000 SoC. The PS and the PL are on separate power domains, enabling the user of these devices to power down the PL for power management if required.

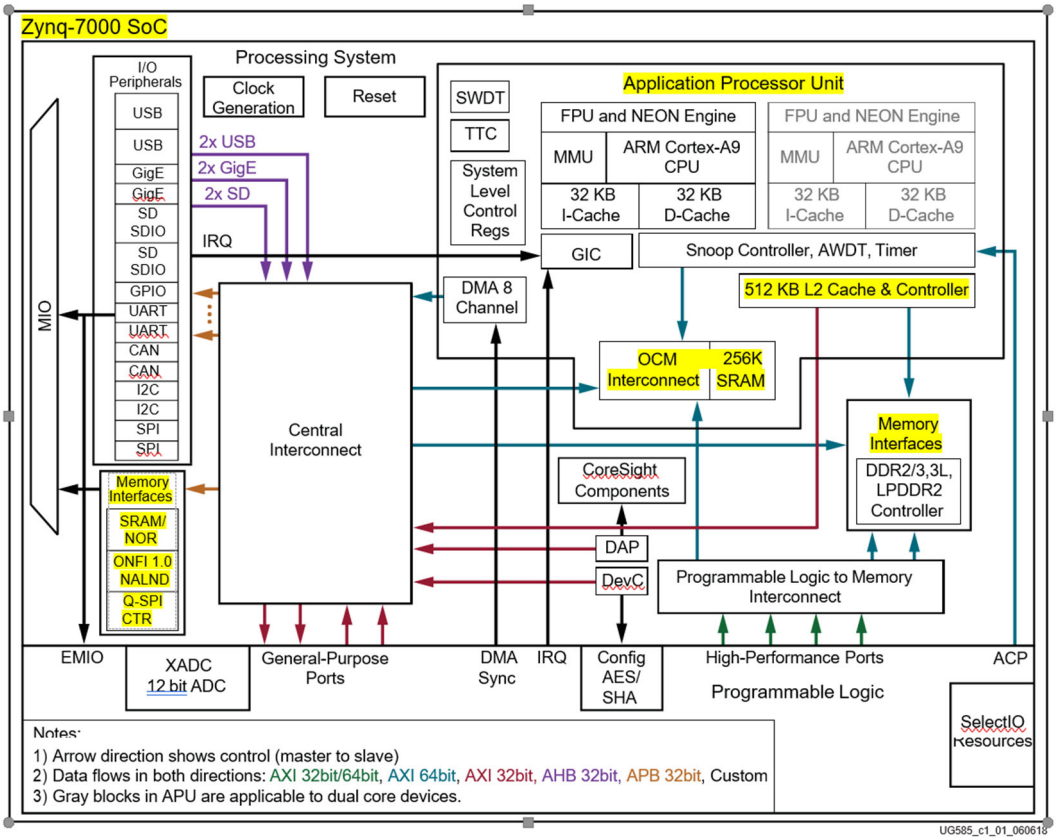

Figure 1-1: **Zynq-7000 SoC Overview**

Zynq-7000 SoC Technical Reference Manual p.26
UG585 (v1.12.2) July 1, 2018

Introduction

Introduction to the UltraScale Architecture

The Xilinx® UltraScale™ architecture enables multi-hundred gigabit-per-second levels of system performance with smart processing, while efficiently routing and processing data on-chip. UltraScale architecture-based devices address a vast spectrum of high-bandwidth, high-utilization system requirements by using industry-leading technical innovations, including next-generation routing, ASIC-like clocking, 3D-on-3D ICs, multiprocessor SoC technologies, and new power reduction features. The devices share many building blocks, providing scalability across process nodes and product families to leverage system-level investment across platforms.

Figure 3-2 shows a top-level functional diagram of the Cortex-A53 MPCore processor.

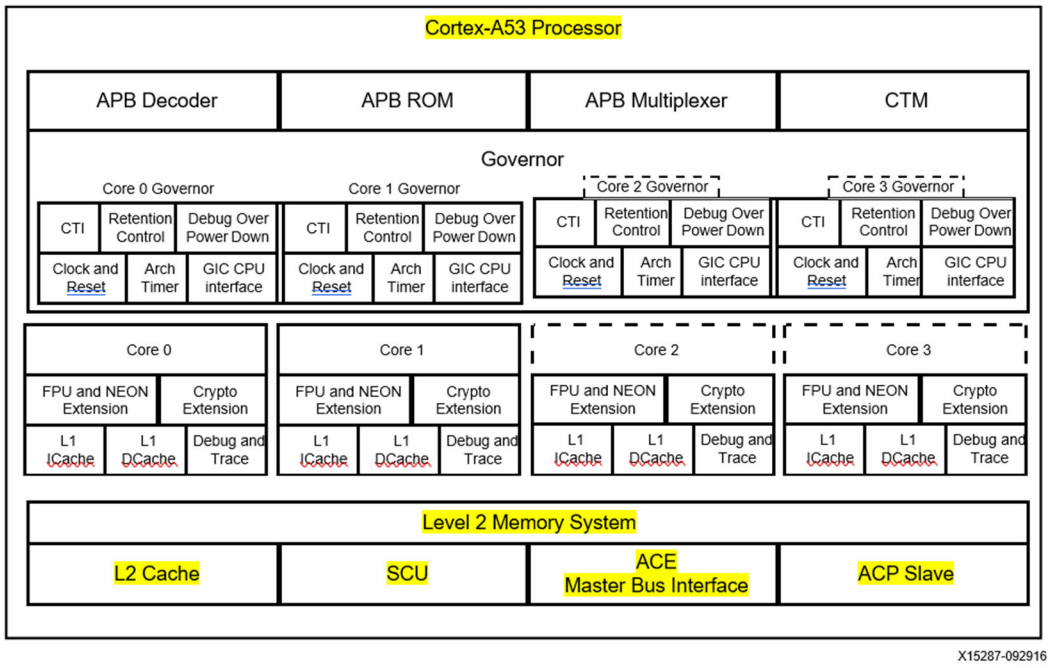

Figure 3-2: **APU Block Diagram**

Zynq UltraScale+ Device Technical Reference Manual pg. 58
UG1085 (v2.2) December 4, 2020

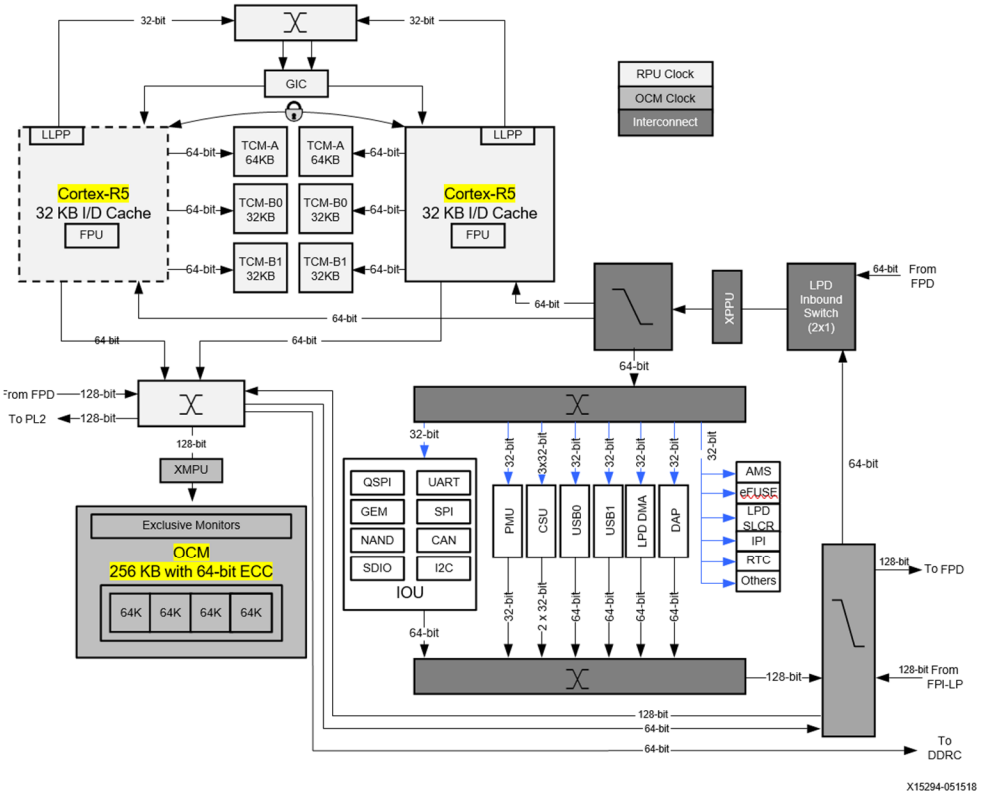

Figure 4-1: **System View of RPU**

Zynq UltraScale+ Device TRM pg. 85
UG1085 (v2.2) December 4, 2020

Processing System

All Versal devices contain a processing system (PS) consisting of Scalar Engines (APU and RPU) and peripherals. The PS is part of a group of architectural elements that include the platform managemer controller (PMC), CPM block, NoC, and integrated memory controllers that are tightly coupled, but are also capable of operating independently from each other. The simplified layout is shown in Figure 2.

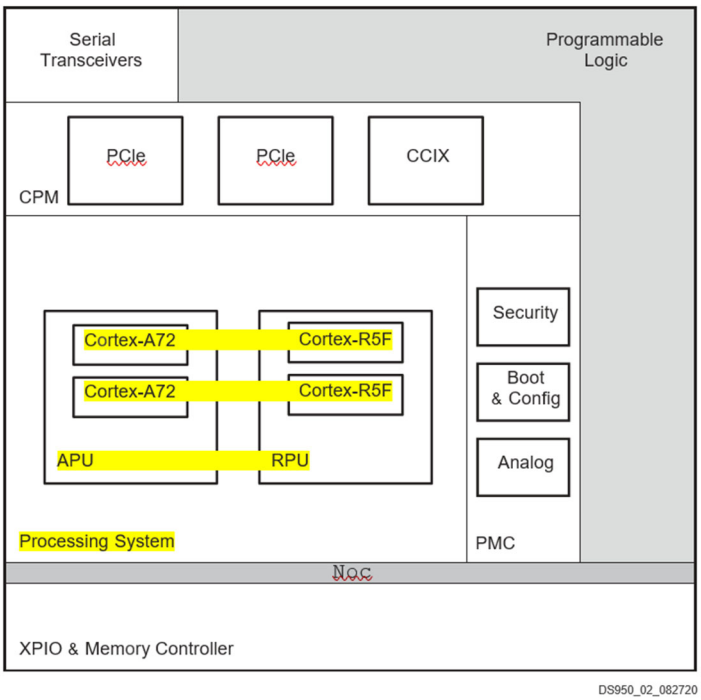

Figure 2: **PS and Surrounding Blocks**

Versal Data Sheet Overview pages 15-16
DS950 (v1.14) December 9, 2021

30. Xilinx documentation describes one or more of the Xilinx '177 Products as including a processor of various ARM Cortex processing cores, which are capable of both high and low frequency operations, and which include various low speed (low power) modes such as sleep and standby modes and full speed (full power) operation.

24.2.3 APU Maximum Frequency

For applications which do not require the maximum amount of processing performance, the APU maximum frequency can be reduced to meet application needs. A lower clock frequency can significantly reduce the operating power when compared to operating at a higher frequency.

24.4 Sleep Mode

Sleep mode is defined at the system level to include the APU in standby mode and multiple controllers being held in reset without a clock.

Going into sleep mode can greatly reduce power consumption. In sleep mode, most function clock groups are turned off or powered off. The only required active devices are one CPU, the snoop control unit (SCU), and a wake-up device. Ideally, the only devices causing dynamic power consumption should be the SCU and the wake-up peripheral device. The wake-up device can be UART, GPIO, or any device that can generate an interrupt.

If the wake-up device is an AXI bus master, which can start transactions targeting the DRAM, additional limitations apply. Because the whole interconnect and the DDR memory are in low power modes and inaccessible, it must be assured that the CPU goes through the full wake-up process before any transactions to the DRAM take place. This guarantees that potential transactions targeting the DRAM are served correctly.

Zynq-7000 SoC TRM pages 680-683
UG585 (v1.12.2) July 1, 2018

Application Overview

Zynq UltraScale+ MPSoC is the Xilinx second-generation Zynq platform, combining a powerful processing system (PS) and user-programmable logic (PL) into the same device. The processing system features the Arm® flagship Cortex®-A53 64-bit quad-core or dual-core processor and Cortex-R5F dual-core real-time processor. In addition to the cost and integration benefits previously provided by the Zynq-7000 devices, the Zynq UltraScale+ MPSoC and RFSoC devices also provide these new features and benefits.

- Scalable PS with scaling for power and performance.
- Low-power running mode and sleep mode.
- Flexible user-programmable power and performance scaling.
- Advanced configuration system with device and user-security support.

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Low-Power Operation Mode

In the low-power operation mode, hardware blocks on the low power rail are powered up in the PS block (PMU, RPU, CSU, and the IOP). The low-power mode includes all peripherals except the SATA and display port blocks. Table 6-1 shows the IP enabled in low-power mode.

Table 6-1: **Minimum and Typical Configurations for the Low-Power Mode**

System Elements	Typical Minimum Configuration	Typical Configuration Full Optimization	Comments
Cortex-R5F	One core @ 50 MHz	Two cores @maximum data sheet frequency	Clock is gated to the unused core.
TCM configuration OCM configuration	Powered down 128KB	64 KB instruction and 64 KB data 256 KB	Power is gated off to the unused TCM banks. Power is gated off to the unused banks

Zynq UltraScale+ Device TRM pg. 121
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Power

The device power architecture includes power domains and PS-based power islands. The power domains are large areas of the device that have their own set of power pins. The power islands are smaller areas within the LPD and FPD power domains. The power island are controlled by onboard power FETs. These FETs are controlled by register bits. The power domains and islands are shown in the Power Diagram.

Power Reduction Features

There are several power reduction features. In addition to power control, the processors have sleep modes. The power domains are controlled by output pins attached to external power supplies. The PS power islands are controlled by on-chip power FETs that are controlled by registers accessible to the PSM.

- Processor sleep/wake feature
- PS and PL clock frequency reduction and clock gating

Versal ACAP Technical Reference Manual p. 788-789
AM011 (v1.3) October 27, 2021

31. Xilinx documentation describes one or more of the Xilinx '177 Products as having a ROM memory and at least one ARM processing core that can boot independently without first retrieving a program stored in non-volatile memory.

Boot and Configuration

6.1 Introduction

Immediately after the PS_POR_B reset pin deasserts, the hardware samples the boot strap pins and optionally enables the PS clock PLLs. Then, the PS begins executing the BootROM code in the on-chip ROM to boot the system. The POR resets the entire device with no previous state saved. The non-POR type resets also cause the BootROM to execute, but without the hardware sampling the strap pins. After a non-POR reset, some registers values are preserved and the device is aware of its previous security mode. Non-POR resets include the PS_SRST_B pin and several internal reset sources.

The BootROM is the first software to run in the APU. The BootROM executes on CPU 0 and CPU 1 executes the wait-for-event (WFE) instruction. The main tasks of the BootROM are to configure the system, copy the Boot Image FSBL/User code from the boot device to the OCM, and then branch the code execution to the OCM. Optionally, the FSBL/User code can be executed directly from a Quad-SPI or NOR device in a non-secure environment.

Zynq-7000 SoC Technical Reference Manual p.148
UG585 (v1.12.2) July 1, 2018

PS Boot and Device Configuration

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decrypts and authenticates the images while the 4096-bit RSA block authenticates the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. The CSU executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the OCM.

After copying the FSBL to OCM, one of the processors, either the Cortex-A53 or Cortex-R5F, executes the FSBL. Xilinx supplies example FSBLs or users can create their own. The FSBL initiates the boot of the PS and

Zynq UltraScale+ MPSoC Data Sheet Overview p.39
DS891 (v1.9) May 26, 2021

RCU BootROM Code

The deeply embedded RCU is the first processor to start up after a power-on reset (POR). The RCU executes its BootROM code to initialize the system and validate the boot device. The RCU processes the boot header provided by the boot device. The RCU downloads the platform loader and manager (PLM) firmware into the PPU RAM and releases the reset on the PPU processor.

Versal ACAP Technical Reference Manual p. 39
AM011 (v1.3) October 27, 2021

32. Xilinx documentation describes one or more of the Xilinx '177 Products as including several general-purpose oscillating clock sources such as PLLs for low frequency and high frequency operation.

6.2.3 Clocks and PLLs

The PS_CLK reference clock is routed to multiple sections of the device, including the three PS clock PLLs. The frequency of the PS_CLK affects the boot time of the device. The PLLs multiply the PS_CLK to generate high frequency clocks for various system clock modules. When needed, the PLLs can be bypassed to deliver the PS_CLK frequency directly to the system clock modules.

If the PLLs are enabled, then the PS_CLK must be stable before the PLLs are enabled and must remain stable. The clock frequency must be within its operating range as specified in the data sheet.

If the PLLs are bypassed, the PS_CLK can be toggled as slow as desired and up to its rated input frequency. This can be used to single-step the bring-up processes, control the clock with software, or operate the system at a low clock frequency. Operating the system at a low clock frequency might preclude the use of some modules within the device (e.g., the USB ULPI clock must be at a lower frequency than the CPU_1x clock).

Zynq-7000 SoC Technical Reference Manual p.162
UG585 (v1.12.2) July 1, 2018

Low-Power Operation Mode

In the low-power operation mode, hardware blocks on the low power rail are powered up in the PS block (PMU, RPU, CSU, and the IOP). The low-power mode includes all peripherals except the SATA and display port blocks. Table 6-1 shows the IP enabled in low-power mode.

Table 6-1: **Minimum and Typical Configurations for the Low-Power Mode**

System Elements	Typical Minimum Configuration	Typical Configuration Full Optimization	Comments
Cortex-R5F	One core @ 50 MHz	Two cores @maximum data sheet frequency	Clock is gated to the unused core.
TCM configuration OCM configuration	Powered down 128KB	64 KB instruction and 64 KB data 256 KB	Power is gated off to the unused TCM banks. Power is gated off to the unused banks
Device security	Without AES	All, including AES	
Peripheral	One set of UART, I^2C, and Ethernet	All peripherals in LPS and one USB 2.0	USB can independently be powered down.
PLLs	One PLL	Two PLLs	PLLs that are not used are in the powered-down state.

Zynq UltraScale+ Device TRM pg. 121
UG1085 (v2.2) December 4, 2020

System PLL Clock Units

Two system PLL clock units are in the LPD and three are in the FPD power domain. Each PLL unit has two clock dividers on its output; one in the LPD and one in the FPD. These clock dividers can provide two different clocking frequencies from one PLL (in the two clock domains). The PLL output and clock frequencies are specified in the *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) [Ref 2]. The maximum clock output frequencies are somewhat lower for clocks crossing power domains.

Each system PLL unit has a suggested usage, but the individual clock generators can select from one of the three PLL clocks routed to it as defined by the registers listed in the Clock Generator Control Registers section.

The system PLL units reside in the LPD and FPD power domains:.

- Low power domain system PLLs:
  - I/O PLL (IOPLL): provides clocks for all low speed peripherals and part of the interconnect.
  - RPU PLL (RPLL): provides clocks for the RPU MPCore and part of the interconnect.
- Full-power domain system PLLs:
  - APU PLL (APLL): provides clocks for the APU MPCore clock and part of the interconnect.

Zynq UltraScale+ MPSoC Data Sheet Overview pg. 1127
DS891 (v1.9) May 26, 2021

Processing System (PS)

Arm Cortex-A53 Based Application Processing Unit (APU)

- Quad-core or dual-core
- CPU frequency: Up to 1.5GHz
- Extendable cache coherency

Dual-core Arm Cortex-R5F Based Real-Time Processing Unit (RPU)

- CPU frequency: Up to 600MHz
- Armv7-R Architecture
  - A32/T32 instruction set

Zynq UltraScale+ MPSoC Data Sheet Overview pg. 1
DS891 (v1.9) May 26, 2021

Main PLL Clocks

The majority of the logic in the PS is clocked from the three PLLs in the PS and one PLL in the PMC through user configurable clock divider circuits. These divider circuits generate clocks to all CPUs, main interconnects, the PMC, and all peripherals. The clocks and their associated PLLs are spread across three power domai ns: the PMC domain, containing the PMC; the low-power domain , containing the RPU and all peripheral clocks; and the full-power domain, containing all other clocks and their PLLs.

Versal Data Sheet Overview page 26
DS950 (v1.14) December 9, 2021

33. Xilinx documentation describes one or more of the Xilinx '177 Products as including multiple programmable logic devices based on programmable logic (PL) and configurable logic blocks arranged consistent with FPGA design paradigms, which can be arranged to run independent processes in parallel with the ARM processing core.

Programmable Logic Description

21.1 Introduction

The Zynq®-7000 SoC integrates a feature-rich dual/single core ARM® Cortex™-A9 MPCore™ based processing system (PS) and Xilinx programmable logic (PL) in a single device. Each Zynq-7000 device contains the same PS while the PL and I/O resources vary between the devices. The PL of the six smallest devices, the 7z010/7z015/7z020 (dual core) and the 7z007s/7z012s/7z014s (single core) is based on Artix®-7 FPGA logic. The three biggest devices, the 7z030, 7z035, 7z045, and 7z100 are based on Kintex®-7 FPGA logic. For documentation resources, refer to DS190, *Zynq-7000 SoC Overview*.

Zynq-7000 SoC Technical Reference Manual p.626
UG585 (v1.12.2) July 1, 2018

Application Overview

Zynq UltraScale+ MPSoC is the Xilinx second-generation Zynq platform, combining a powerful processing system (PS) and user-programmable logic (PL) into the same device. The processing system features the Arm® flagship Cortex®-A53 64-bit quad-core or dual-core processor and Cortex-R5F dual-core real-time processor. In addition to the cost and integration benefits previously provided by the Zynq-7000 devices, the Zynq UltraScale+ MPSoC and RFSoC devices also provide these new features and benefits.

Zynq UltraScale+ Device TRM pg. 27
UG1085 (v2.2) December 4, 2020

Programmable Logic (PL)

Configurable Logic Blocks (CLB)

- Look-up tables (LUT)
- Flip-flops
- Cascadable adders

36Kb Block RAM

- True dual-port
- Up to 72 bits wide
- Configurable as dual 18Kb

UltraRAM

- 288Kb dual-port
- 72 bits wide
- Error checking and correction

DSP Blocks

- 27 x 18 signed multiply
- 48-bit adder/accumulator
- 27-bit pre-adder

Zynq UltraScale+ MPSoC Data Sheet Overview pg. 2
DS891 (v1.9) May 26, 2021

Programmable Logic

This section covers the information about blocks in the Programmable Logic (PL).

Device Layout

UltraScale architecture-based devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. At the core of UltraScale+ MPSoCs is the processing system that displaces some of the full or partial columns of programmable logic resources. Figure 1 shows a device-level view with resources grouped together. For simplicity, certain resources such as the processing system, integrated blocks for PCIe, configuration logic, and System Monitor are not shown.

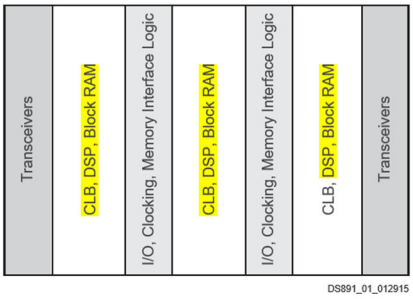


Figure 1: **Device with Columnar Resources**

Zynq UltraScale+ MPSoC Data Sheet Overview pg. 27
DS891 (v1.9) May 26, 2021

XILINX

Zynq® UltraScale+™ MPSoC Family

Xilinx's MPSoC family offers solutions for EG/EV devices with Trenz SoMs

Xilinx's Zynq UltraScale+ MPSoC offers a dual(CG) and quad(EG/EV) core Arm® Cortex®-A53 application processor, a dual-core Arm Cortex-RS real-time processor, and Mali™-400 MP2 graphics processor for EG/EV devices. They include FPGA fabric together with block RAM and UltraRAM. Several development kits and system on modules (SoM) are available from Xilinx and Trenz along with a variety of ICs.

Digikey Product website (last accessed FEB 2, 2022)
https://www.digikey.com/en/product-highlight/x/xilinx/zynq-ultrascale-mpsoc-family

PL Overview

The programmable logic (PL) is a scalable structure that provides the ability to create many possible functions. The PL logic regions include DSP engines, configurable logic blocks, and two types of RAM arrays. These are configured together to create almost any type of hardware functionality including accelerators, processors, functional pipeline units, and peripherals. The PL includes connections for the integrated hardware and peripherals, ports to the NoC interconnect, access to CMOS and gigabit high-speed I/O, and interface channels to the PS.

Versal ACAP Technical Reference Manual p. 84
AM011 (v1.3) October 27, 2021

Xilinx Rolls Out Rugged Versal Families for Aerospace and Defense

Sept. 13, 2021

Xilinx's Versal chips combine hard-core Arm CPUs, AI accelerators, DSP engines, and the same type of programmable logic in its field-programmable gate arrays (FPGAs). Now the company is expanding the Versal family to space- and military-grade systems.

https://www.electronicdesign.com/technologies/embedded-revolution/article/21175156/electronic-design-xilinx-rolls-out-rugged-versal-families-for-aerospace-and-defense

34. Xilinx documentation describes one or more of the Xilinx '177 Products as including analog to digital converters ("ADCs") and on-chip temperature sensing ADCs and configurable interfaces for external ADCs that can operate at multiple bit depths.

XADC (Analog-to-Digital Converter)

Highlights of the XADC architecture at I-grade temperature specs include:

- Dual 12-bit 1 MSPS analog-to-digital converters (ADCs)
- Up to 17 flexible and user-configurable analog inputs
- On-chip or external reference option
- On-chip temperature (±4°C max error) and power supply (±1% max error) sensors
- Continuous JTAG access to ADC measurements

All XA Zynq-7000 SoCs integrate a new flexible analog interface called XADC. When combined with the programmable logic capability of the XA Zynq-7000 SoCs, the XADC can address a broad range of data acquisition and monitoring requirements. For more information, go to: http://www.xilinx.com/ams.

The XADC contains two 12-bit 1 MSPS ADCs with separate track and hold amplifiers, an on-chip analog multiplexer (up to 17 external analog input channels supported), and on-chip thermal and supply sensors. The two ADCs can be configured to simultaneously sample two external-input analog channels. The track and hold amplifiers support a range of analog input signal types, including unipolar, bipolar, and differential. The analog inputs can support signal bandwidths of at least 500 KHz at sample rates of 1MSPS. It is possible to support higher analog bandwidths using external analog multiplexer mode with the dedicated analog input (see UG480, *7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide*).

The XADC optionally uses an on-chip reference circuit (±1%), thereby eliminating the need for any external active components for basic on-chip monitoring of temperature and power supply rails. To achieve the full 12-bit performance of the ADCs, an external 1.25V reference IC is recommended.

Zynq-7000 SoC Datasheet Overview p.23
DS188 (v1.3.2) July 2, 2018

Measurement Registers

The ADCs produce a 16-bit conversion result, and the full 16-bit result (or averaged result) is stored in the 16-bit measurement registers. The specified 10-bit accuracy corresponds to the 10 MSBs (most significant or left-most bits) in the 16-bit ADC conversion result. The unreferenced LSBs can be used to minimize quantization effects or improve resolution through averaging or filtering.

Zynq UltraScale+ Device TRM pg. 200
UG1085 (v2.2) December 4, 2020

System Monitoring

The PMC contains system monitoring capability for monitoring voltage and temperature in the PS and PL to enhance the overall safety, security, and reliability of the system. The core of the system monitor is a 10-bit 200kSPS ADC, which can be accessed via JTAG, PMBus, or I2C interfaces, via the PS directly, and via the **PL** through the NoC.

Versal Data Sheet Overview page 14
DS950 (v1.14) December 9, 2021

System Monitor

The System Monitor (SYSMON) resides in the PMC and monitors operating conditions on the device. The SYSMON can access internal sensors for monitoring internal power supplies and temperature. MIO or high-density I/O (HDIO) pins can be used by the SYSMON for measuring voltage levels external to the device. The results captured by the SYSMON are stored in a register map that is accessible through platform management controller resources. See the *Versal ACAP System Monitor Architecture Manual* (AM006) for more information.

Versal ACAP Technical Reference Manual p. 77
AM011 (v1.3) October 27, 2021

35. Xilinx documentation describes one or more of the Xilinx '177 Products as including programmable logic for signal processing applications, such as digital signal processing (DSP).

Programmable Logic (PL)

Configurable Logic Blocks (CLB)

- Look-up tables (LUT)
- Flip-flops
- Cascadeable adders

36 Kb Block RAM

- True Dual-Port
- Up to 72 bits wide
- Configurable as dual 18 Kb

DSP Blocks

- 18 x 25 signed multiply
- 48-bit adder/accumulator
- 25-bit pre-adder

Digital Signal Processing — DSP Slice

Some highlights of the DSP functionality include:

- 25 × 18 twos complement multiplier/accumulator high-resolution (48 bit) signal processor
- Power saving pre-adder to optimize symmetrical filter applications
- Advanced features: optional pipelining, optional ALU, and dedicated buses for cascading

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All XA Zynq-7000 SoCs have many dedicated, full custom, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 25 × 18 bit two's complement multiplier and a 48-bit accumulator, both capable of operating up to 464 MHz. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The DSP also includes a 48-bit-wide Pattern Detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

Zynq-7000 SoC Datasheet Overview pgs. 2 and 19
DS188 (v1.3.2) July 2, 2018

Programmable Logic (PL)

Configurable Logic Blocks (CLB)

- Look-up tables (LUT)
- Flip-flops
- Cascadable adders

36Kb Block RAM

- True dual-port
- Up to 72 bits wide
- Configurable as dual 18Kb

UltraRAM

- 288Kb dual-port
- 72 bits wide
- Error checking and correction

DSP Blocks

- 27 x 18 signed multiply
- 48-bit adder/accumulator
- 27-bit pre-adder

Zynq UltraScale+ MPSoC Data Sheet Overview pg. 2
DS891 (v1.9) May 26, 2021

Programmable Logic

This section covers the information about blocks in the Programmable Logic (PL).

Device Layout

UltraScale architecture-based devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. At the core of UltraScale+ MPSoCs is the processing system that displaces some of the full or partial columns of programmable logic resources. Figure 1 shows a device-level view with resources grouped together. For simplicity, certain resources such as the processing system, integrated blocks for PCIe, configuration logic, and System Monitor are not shown.

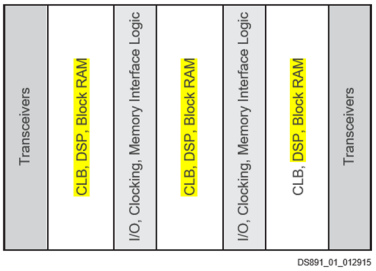


Figure 1: **Device with Columnar Resources**

Zynq UltraScale+ MPSoC Data Sheet Overview pg. 27
DS891 (v1.9) May 26, 2021

PL Overview

The programmable logic (PL) is a scalable structure that provides the ability to create many possible functions. The PL logic regions include DSP engines, configurable logic blocks, and two types of RAM arrays. These are configured together to create almost any type of hardware functionality including accelerators, processors, functional pipeline units, and peripherals. The PL includes connections for the integrated hardware and peripherals, ports to the NoC interconnect, access to CMOS and gigabit high-speed I/O, and interface channels to the PS.

Versal ACAP Technical Reference Manual p. 84
AM011 (v1.3) October 27, 2021

36. Xilinx documentation describes one or more of the Xilinx '177 Products as including a flexible and configurable routing architecture for internal signal distribution and routing.

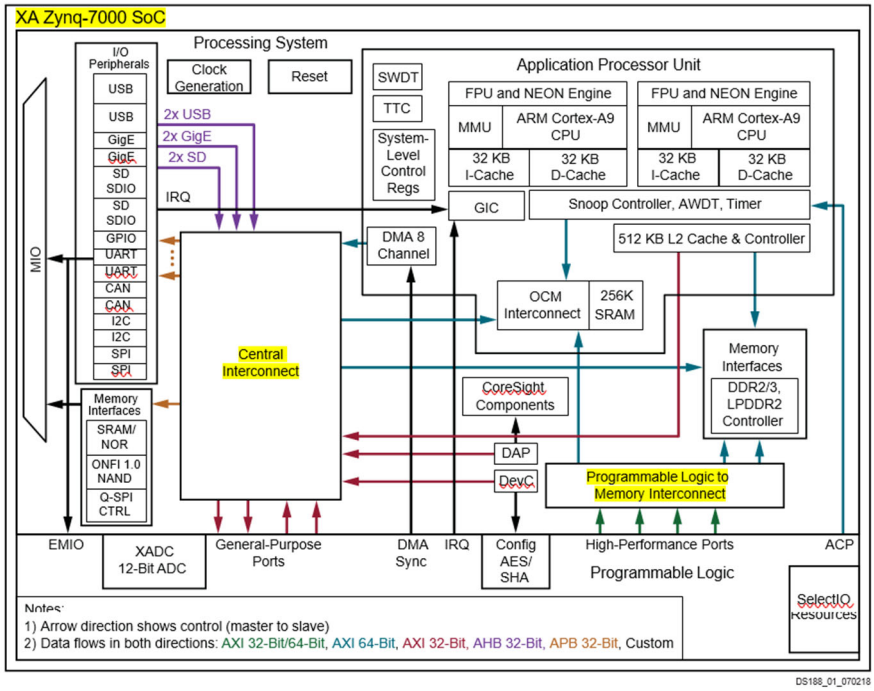


Figure 1: **XA Zynq-7000 SoC Overview**

Zynq-7000 SoC Technical Reference Manual p.27
UG585 (v1.12.2) July 1, 2018

Programmable Logic

This section covers the information about blocks in the Programmable Logic (PL).

Device Layout

UltraScale architecture-based devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. At the core of UltraScale+ MPSoCs is the processing system that displaces some of the full or partial columns of programmable logic resources. Figure 1 shows a device-level view with resources grouped together. For simplicity, certain resources such as the processing system, integrated blocks for PCIe, configuration logic, and System Monitor are not shown.

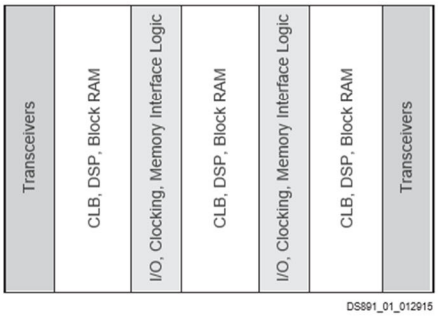


Figure 1: **Device with Columnar Resources**

Zynq UltraScale+ MPSoC Data Sheet Overview pg. 27
DS891 (v1.9) May 26, 2021

Within every CLB are dedicated interconnect paths for connecting LUTs without having to exit and re-enter a CLB, drastically reducing the use of global routing resources. In addition, new CLB features such as cascade multiplexers allow flexible carry logic structures to be created.

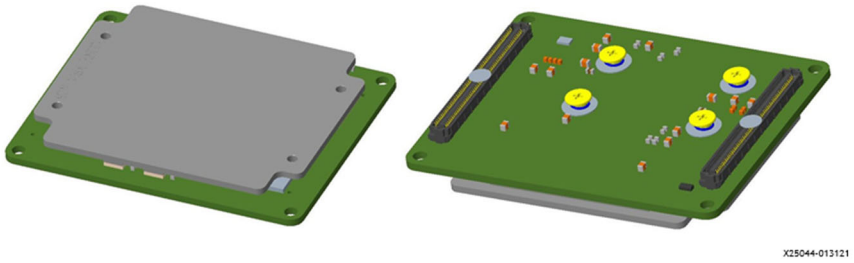
Versal ACAP Technical Reference Manual p. 87
AM011 (v1.3) October 27, 2021

37. Xilinx's other accused Zynq products based on the Zynq-7000 and Zynq UltraScale+ products such as its Kria line of products and associated development kits such as the Ultrascale+ ZCU102, ZCU104, ZCU106 and Zynq 7000 Soc ZC702, ZC704 and ZC706 Evaluation Boards infringe for at least the same reasons given above.

Module Description

The Xilinx® Kria™ K26 system-on-module (SOM) is a compact embedded platform that integrates a custom-built Zynq® UltraScale+™ MPSoC that runs optimally (and exclusively) on the K26 SOM with DDR memory, nonvolatile storage devices, a security module, and an aluminum thermal heat spreader. The SOM is designed to be plugged into a carrier card with solution-specific peripherals. Key target applications include smart city, machine vision, industrial robotics, and AI/ML computing. The following figure shows the top-side and bottom-side connector view.

Figure 1: **K26 SOM**



Functional Overview and Block Diagram

The K26 SOM leverages the XCK26-SFVC784-2LV-C/I, a custom-built Zynq UltraScale+ MPSoC that runs optimally (and exclusively) on the SOM. It provides an embedded processing system (PS) with tightly integrated programmable logic and a rich set of configurable I/O capabilities. The SOM hardware features include:

- Zynq UltraScale+ MPSoC (XCK26 in commercial (C) grade or industrial (I) grade)
- 4 GB 64-bit wide, 2400 Mb/s memory
- Integrated non-volatile memory devices
  - 512 Mb QSPI
  - 16 GB eMMC
  - 64 Kb EEPROM

Kria SOM Datasheet pgs. 1-2
DS987 (v1.1) July 23, 2021

38. The ’177 Patent is well-known within the industry, as demonstrated by multiple citations to the ’177 Patent in published patents and patent applications assigned to technology companies and academic institutions, as well as previous infringement litigations against other well-known semiconductor companies. Xilinx is utilizing the technology claimed in the ’177 Patent without paying a reasonable royalty. Xilinx is infringing the ’177 Patent in a manner that is willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, or flagrant.

39. As a result of Xilinx’s infringement of the ’177 Patent, Sentient has suffered

monetary damages, and seeks recovery in an amount adequate to compensate for Xilinx's infringement, but in no event less than a reasonable royalty for the use made of the invention by Xilinx together with interest and costs as fixed by the Court

COUNT II
Inducement of Infringement of the '177 Patent

40. Sentient incorporates by reference the allegations set forth in the preceding paragraphs.

41. On information and belief, Xilinx has also indirectly infringed and is currently indirectly infringing the '177 Patent under 35 U.S.C. § 271(b) by inducing others, including its customers, to make, use, import, provide, supply, distribute, sell, and offer to sell products and systems that Xilinx knows infringe one or more claims of the '177 Patent in the United States generally, and in Delaware, and within this judicial district in particular.

42. On information and belief, Xilinx has intentionally induced infringement, or at least has been willfully blind to infringement of the '177 Patent, by others, including its customers, since at least the date of the notification letter in 2016.

43. By way of example, Xilinx provides use instructions and product literature to its customers that induce infringement of the '177 Patent.

44. Furthermore, Xilinx induces infringement of certain claim elements by providing memory controllers on the '177 Xilinx Products to interact, communicate with, and direct the action of various external memories, such as the volatile and non-volatile memories as described in Count I above. *See, e.g.,* Zynq 7000 SoC Datasheet, DS188 (v1.3.2) July 2, 2018, p. 1.

45. On information and belief, Xilinx intended to induce patent infringement by third-party customers and users of the Xilinx '177 Products and had knowledge that its inducing acts would cause direct infringement or was willfully blind to the likelihood that its inducing acts

would cause direct infringement, for example in its Development Kits. Xilinx was aware that the normal and customary use of the Xilinx '177 Products would infringe the '177 Patent. Xilinx performed the acts that constitute induced infringement, and would induce direct infringement, with knowledge of the '177 Patent and with the knowledge that the induced acts would constitute infringement. For example, Xilinx provides the Xilinx '177 Products, which have the capability of operating in a manner that directly infringe one or more of the claims of the '177 Patent, including at least claim 1, and Xilinx further provides documentation and training materials that cause customers and end users of the Xilinx '177 Products to utilize the products in a manner that directly infringes one or more claims of the '177 Patent. By providing instructions and training to customers and end-users on how to use the Xilinx '177 Products in a manner that directly infringes one or more claims of the '177 Patent, including at least claim 1, Xilinx specifically intended to induce infringement of the '177 Patent. On information and belief, Xilinx engaged in such inducement to promote the sales of the Xilinx '177 Products, *e.g.*, through Xilinx's Development Kits and related materials, user manuals, product support, marketing and advertising materials, and through training materials and activities to actively induce the users of the Xilinx '177 Products to infringe the '177 Patent. Accordingly, Xilinx has induced and continues to induce users of the Xilinx '177 Products to use the Xilinx '177 Products in their ordinary and customary way to infringe the '177 Patent, knowing that such use constitutes infringement of the '177 Patent.

46. The '177 Patent is well-known within the industry as demonstrated by multiple citations to the '177 Patent in published patents and patent applications assigned to technology companies and academic institutions as well as previous infringement litigations against other well-known semiconductor companies. Xilinx is utilizing the technology claimed in the '177 Patent without paying a reasonable royalty. Xilinx is infringing the '177 Patent in a manner that

is willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, or flagrant.

47. As a result of Xilinx's infringement of the '177 Patent, Sentient has suffered monetary damages, and seeks recovery in an amount adequate to compensate for Xilinx's infringement, but in no event less than a reasonable royalty for the use made of the invention by Xilinx together with interest and costs as fixed by the Court.

COUNT III
Contributory Infringement of the '177 Patent

48. Sentient incorporates by reference the allegations set forth in the preceding paragraphs.

49. Upon information and belief, Xilinx also has indirectly infringed and is currently indirectly infringing the '177 Patent under 35 U.S.C. §271(c) by contributing to the infringement of others, including its customers, by making, using, importing, providing, supplying, distributing, selling, and offering to sell at least the '177 Xilinx Products and systems that infringe one or more claims of the '177 Patent in the United States generally, and in Delaware, and in this judicial district in particular.

50. On information and belief, Xilinx has intentionally contributed to infringement, or at least has been willfully blind to infringement of the '177 Patent, by its customers since at least the date of the notification letter in 2016.

51. By way of example, Xilinx provides use instructions and product literature to its customers that contribute to infringement of the '177 Patent, which include the above-referenced Evaluation Kits.

52. Furthermore, Xilinx contributes to infringement by providing the Xilinx '177 Products, which include memory controllers, to interact, communicate with, and direct the action of various external memories, such as the volatile and non-volatile memories as described in Count I above. *See, e.g.,* Zynq 7000 SoC Datasheet, DS188 (v1.3.2) July 2, 2018, p. 1.

53. On information and belief, end users have used, and continue to use, the '177 Xilinx Products in a manner that directly infringes one or more claims of the '177 Patent. More specifically, Xilinx sells and offers to sell infringing products to its customers that are not staple articles of commerce and that have no substantial uses outside of those that infringe the '177 Patent.

54. The acts of infringement by Xilinx have caused and will continue to cause damage to Sentient in its capacity as assignee of the '177 Patent, and Sentient is entitled to recover damages from Xilinx in an amount no less than a reasonable royalty pursuant to 35 U.S.C. §284. The full measure of damages sustained as a result of Xilinx's wrongful acts will be proven at trial.

55. The infringement of Sentient's exclusive rights under the '177 Patent by Xilinx has damaged Sentient, and unless enjoined will continue to damage Sentient, causing irreparable harm, for which there is no adequate remedy at law.

56. Upon information and belief, Xilinx has infringed and continues to infringe the '177 Patent despite having knowledge of the '177 Patent and its applicability to the '177 Xilinx Products.

57. Upon information and belief, Xilinx's infringement of the '177 Patent has been, and continues to be, willful.

JURY DEMAND

PRAYER FOR RELIEF

WHEREFORE, Sentient prays for judgment and requests that the Court find in its favor and against Xilinx, and that the Court grant Sentient the following relief:

a. Judgment that one or more claims of the '177 Patent have been or are infringed, either literally or under the doctrine of equivalents, by Xilinx and by others whose infringement has been induced by Xilinx and to whose infringement Xilinx has contributed;

b. Judgment that the '177 Patent is not invalid and is not unenforceable;

c. Preliminary and permanent injunctive relief enjoining Xilinx and its officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in concert therewith from infringing, inducing infringement, or contributing to infringement of the '177 Patent;

d. Judgment that Xilinx account for and pay to Sentient all damages and costs incurred by Sentient as a result of Xilinx's infringing activities under 35 U.S.C. 284, such that Sentient is adequately compensated for Xilinx's infringement of the '177 Patent, but in no event less than a reasonable royalty for the use made by Xilinx of the inventions claimed in the '177 Patent, including supplemental damages for any continuing post-verdict infringement up until entry of final judgment, with an accounting, as needed, and enhanced damages as provided by 35 U.S.C. 284;

e. Pre-judgment and post-judgment interest on the damages caused by Xilinx's infringing activities and other conduct complained of herein or otherwise;

f. A declaration that this is an exceptional case and an award of Sentient's reasonable attorneys' fees and costs in accordance with 35 U.S.C. 285 or as otherwise permitted by law;

g. All costs of suit; and,

h. Such other and further relief as the Court may deem just and proper under the circumstances.

Dated: February 8, 2022

Respectfully submitted,

FARNAN LLP

/s/ Michael J. Farnan
Brian E. Farnan (Bar No. 4089)
Michael J. Farnan (Bar No. 5165)
919 N. Market St., 12th Floor
Wilmington, DE 19801
Telephone: (302) 777-0300
Facsimile: (302) 777-0301
bfarnan@farnanlaw.com
mfarnan@farnanlaw.com

OF COUNSEL:

Michael Shanahan
Matthew Harper
YK Law LLP
32 E. 57th Street, 8th Floor
New York, NY 10022
Telephone: 646-286-9286
mshanahan@yklaw.us
mharper@yklaw.us

Gerald J. Flattmann
Andrew Cochran
King & Spalding
1185 6th Avenue
New York, NY 10036
Telephone: (212) 556-2100
GFlattmann@KSLAW.com
ACochran@KSLAW.com

Attorneys for Plaintiff
Sentient Sensors, LLC