IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

OASIS TOOLING, INC., a Delaware Corporation, Plaintiff, v. GLOBALFOUNDRIES U.S. INC., a Delaware Corporation, Defendant.	)	C.A. No. _____ **DEMAND FOR JURY TRIAL**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Oasis Tooling, Inc. ("Oasis") files this Complaint for Patent Infringement and Demand for Jury Trial against GlobalFoundries U.S., Inc. ("GlobalFoundries") and alleges as follows:

1. Oasis is seeking to protect its valuable intellectual property from ongoing willful infringement by GlobalFoundries. Oasis, a semiconductor company, developed and patented novel technology generally directed to methods and devices for the independent evaluation of cell integrity, changes, and verification of origin in chip design for production workflow (the "Oasis Inventions").

THE PARTIES

2. Oasis is a Delaware corporation with its principal place of business at 151 4th Street, Ketchum, Idaho.

3. Thomas Grebinski, a semiconductor pioneer, who continues to actively innovate in this important field, founded Oasis in 2004. Oasis obtained a portfolio of patents covering the Oasis Inventions.

4. GlobalFoundries is a Delaware corporation. GlobalFoundries may be served through its agent for service of process, Corporation Service Company, at 251 Little Falls Drive, Wilmington, Delaware, 19808.

5. GlobalFoundries developed and is responsible for the Accused Products (defined below).

JURISDICTION AND VENUE

6. This action for patent infringement arises under the patent laws of the United States, 35 U.S.C. § 101 *et seq*. This Court has original jurisdiction over this controversy pursuant to 28 U.S.C. §§ 1331 and 1338.

7. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and 1400(b).

8. The Court has personal jurisdiction over GlobalFoundries because it is incorporated within this District and because GlobalFoundries has committed acts of direct and indirect infringement in this District, including through selling and offering for sale infringing products and services in this District. Additionally, GlobalFoundries has availed itself of this forum by bringing six suits in this District to enforce its own patents. *See* Case Nos. 1:19-cv-01571; 1:19-cv-01572; 1:19-cv-01573; 1:19-cv-01574; 1:19-cv-01575; 1:19-cv-01576. Given the above, the exercise of jurisdiction by this Court over GlobalFoundries in this action would be reasonable.

OASIS' INNOVATIONS AND ASSERTED PATENTS

9. Oasis' founder and CEO, Thomas Grebinski, started and led the SEMI working group that developed the Open Artwork System Interchange Standard (OASIS®) in June 2001 (through SEMI's Data Path Task Force). OASIS® is a language used by computers to represent

electronic patterns for integrated circuits during the design and manufacture stages. OASIS® replaced GDSII as the dominant standard, and is now widely used in the semiconductor industry, including by foundries, fabless semiconductor companies, integrated device manufacturers, IP suppliers, and electronic design automation (EDA) vendors.

10. Oasis develops integrated circuit-design flow optimization software for the semiconductor and fabrication industry, including relating to the OASIS® language. Oasis delivered the industry's first commercial reference implementation for OASIS®.

11. Oasis' offerings have grown to include a number of industry firsts, including (1) software products in standard compliance, (2) OASIS® reference implementations, (3) OASIS®/GDSII design layout equivalence checking, (4) OASIS® Reader/Writer Source Code, (5) OASIS®/GDSII Stress Test Cases, (6) on-premises design workflow auditing utilities, and (7) cloud-based ecosystem workflow view and management applications.

12. The United States Patent and Trademark Office ("USPTO") awarded to Oasis patents covering the Oasis Inventions for improving semiconductor chip design and manufacturing processes using specific techniques.

13. On March 23, 2010, the USPTO issued U.S. Patent No. 7,685,545 (the "'545 Patent"), entitled "Methods and Devices for Independent Evaluation of Cell Integrity, Changes and Origin in Chip Design for Production Workflow." The '545 Patent lists Thomas Grebinski and David Chapman as its inventors, and states that it was assigned to Oasis. Attached hereto as Exhibit 1 is a true and correct copy of the '545 Patent.

14. On September 11, 2012, the USPTO issued U.S. Patent No. 8,266,571 (the "'571 Patent"), entitled "Methods and Devices for Independent Evaluation of Cell Integrity, Changes and Origin in Chip Design for Production Workflow." The '571 Patent lists Thomas Grebinski

and David Chapman as its inventors, and states that it was assigned to Oasis. Attached hereto as Exhibit 2 is a true and correct copy of the '571 Patent.

15. The '545 and '571 Patents (together, the "Asserted Patents") are generally directed to specific techniques for the granular analysis of design and manufacturing data used to prepare chip designs for manufacturing and to identify similarities and differences among parts of design data files using a variety of components, including a parser, normalizer logic, syntax tree, canonical forming modules, digester, and reporter, amongst others.

16. The Asserted Patents disclose and specifically claim inventive concepts that represent significant improvements over conventional systems. Specifically, each of the Asserted Patents describe various techniques, including the ability to parse data into syntax trees and normalize the trees into canonical forms, which are used to generate a specific digest per a selected partition, amongst other functionality (the "Oasis Tools").

17. The Oasis Tools were not available in the art because conventional tools did not have ways to identify cells that were functionally the same but described differently in design files, or to ascertain those differences using the components set forth in the claims of the Asserted Patents.

18. The Asserted Patents disclose more than just a simple combination of generic components to perform conventional activities. The claimed inventions improve the functionality and capabilities of computers used in the process of designing, verifying, and fabricating semiconductor chips. The claimed inventions do so by enabling the detection of cells that are functionally the same, even if they are differently described in design files, variously using new components in an unconventional manner, including, for example, design units that

include header and/or cell data which correspond to parts of a physical circuit design and parsing syntax of and normalizing design data into canonical forms.

19. The Asserted Patents include specific, non-conventional steps and concepts which are rooted in computer technology that make the claimed inventions concrete and non-abstract. For example, certain claims of the Asserted Patents variously recite: (1) parsing syntax of and normalizing design data within cells into canonical forms that reduce sensitivity of data analysis to non-functional variations in the design data within a cell; (2) partitioning functionally significant design data from non-significant data within the canonical forms; (3) calculating and storing digests of the cells including at least the functionally significant design data; and (4) then comparing the digests of the cells in two design files.

20. None of the aforesaid steps were known, let alone conventional, in the art at the time of the inventions because then-conventional chip-level design and manufacturing data management systems could not determine or summarize what changed within a given collection of cell and block data found within a file.

21. In addition, the claims are rooted in computer technology as they are specifically directed toward computer chip design and manufacturing and provide the capability to evaluate cell equivalence at the cell level and determine the changes to an individual cell, which was not available in the art. Thus, the claims of the Asserted Patents recite specific steps to accomplish the desired result and go beyond simply claiming a result.

22. Accordingly, the inventions of the Asserted Patents allow for a new kind of system that was not previously possible, enabling a new level of granular analysis of design data used to prepare chip designs for manufacturing with new types of digests, including canonical cell digests and canonical design unit digests.

GLOBALFOUNDRIES' KNOWLEDGE OF OASIS' PATENTS

23. GlobalFoundries has prior and direct knowledge of Oasis' patents and patented technology through various officers and employees, as set forth below.

A. AMD's Prior and Direct Knowledge of Oasis' Patents

24. Advanced Micro Devices, Inc. ("AMD") is an American multinational semiconductor company based in Santa Clara, California. AMD develops computer processors and related technologies.

25. In 2009, AMD divested its semiconductor fabrication business as GlobalFoundries.

26. In 2008 and 2009, prior to AMD's divestiture of GlobalFoundries, AMD investigated Oasis' technology.

27. Through AMD's investigation of Oasis' technology, AMD learned that Oasis was seeking patents to protect the Oasis Inventions.

28. AMD entered into an NDA with Oasis to further its investigation of Oasis' technology.

29. For example, on or about September 2008, Oasis, through Mr. Grebinski, sent an NDA to AMD describing some of the Oasis Inventions.

30. On or about November 13, 2008, Oasis, through Mr. Grebinski, sent a presentation describing some of the Oasis Inventions to Chris Spence.

31. At that time, Mr. Spence was a Senior Fellow at AMD. Ex. 3 (Spence profile).

32. The presentation explained that Oasis' technology included normalizing design data and assigning identifiers to one or more cells, one or more libraries of one or more cells, or

one or more design files, in order to compare the various versions of cells, libraries of cells, or design files.

33. On or about December 15, 2008, Oasis, through Mr. Grebinski, sent an updated presentation to Mr. Spence.

34. The updated presentation contained additional information about the Oasis Inventions, such as normalizing design data and using the Oasis Inventions to perform comparisons and error isolation in the design and manufacturing processes.

35. In its presentation, Oasis offered to partner with AMD.

36. Luigi Capodieci, an AMD R&D Fellow, was also involved in investigating Oasis' technology. Ex. 4 (Capodieci profile).

37. During the November 2008 through January 2009 timeframe, Mr. Grebinski had several telephone conversations and at least one in-person meeting with Mr. Spence and Mr. Capodieci.

38. When AMD divested GlobalFoundries later in 2009, Mr. Capodieci and Mr. Spence remained with GlobalFoundries.

39. On information and belief, at least Mr. Capodieci was involved in developing the Accused Products (defined below). *See* Exs. 3-4 (Capodieci and Spence profiles)

B. Qualcomm's Prior Knowledge of Oasis' Patents

40. Qualcomm is an American multinational corporation headquartered in San Diego, California. Qualcomm creates semiconductors, software, and services related to wireless technology.

41. Qualcomm, through its Senior Director and Principal Engineer, Riko Radojcic, and its Principal Manager/Engineer, Illam Pakkirisamy, investigated the Oasis Inventions. Ex. 5 (Pakkirisamy profile).

42. In November 2008, Mr. Grebinski sent a presentation describing some of the Oasis Inventions to Qualcomm's Mr. Radojcic.

43. For example, the presentation explained that Oasis' technology included normalizing design data and assigning identifiers to one or more cells, one or more libraries of one or more cells, or one or more design files, in order to compare the various versions of cells, libraries of cells, or design files.

44. On the slides in the presentation providing technical details, there was a legend stating that the Oasis Inventions were patent pending.

45. In its presentation, Oasis offered to partner with Qualcomm.

46. On or about November 24, 2008, Mr. Radojcic introduced Mr. Pakkirisamy to Mr. Grebinski.

47. On or about June 16, 2009, Mr. Pakkirisamy pointed out to Qualcomm's Staff Engineer, Chris Ashburn, that Oasis' software solved some of the problems that Qualcomm was facing.

48. On information and belief, on or about June 16, 2009, Qualcomm decided to conduct an evaluation of Oasis' software. Mr. Pakkirisamy suggested to Mr. Ashburn that he contact Mr. Grebinski to learn more about the Oasis Inventions.

49. In February 2010, Qualcomm's Messrs. Pakkirisamy and Ashburn conducted a successful evaluation of Oasis' Smart Signature Comparison software, which was able to

compare and report changes to one or more cells, one or more libraries of cells, and one or more design files.

50. Oasis' Smart Signature Comparison software was able to scan a library of GDSII and/or OASIS library designs, and detect and report any meaningful electrical, physical and/or functional changes to that library of design data.

51. Oasis identified its Smart Signature Comparison software as covered by pending patent applications.

52. Through leading Qualcomm's evaluation of Oasis' technology, Mr. Pakkirisamy became familiar with the Oasis Inventions and knew that Oasis was pursuing patents to protect those same inventions.

53. Mr. Grebinski's last update to Mr. Pakkirisamy was on or about May 10, 2010.

54. In September 2010, Mr. Pakkirisamy joined GlobalFoundries as a Director. Ex. 5 at 2 (Pakkirisamy Profile).

55. On information and belief, while Mr. Pakkirisamy worked for GlobalFoundries, he became involved in developing the Accused Products.

C. GlobalFoundries' Officers and Employees Knew About Oasis' Patents

56. GlobalFoundries is fully aware of the Asserted Patents and that its Accused Products infringe the Asserted Patents through at least its former Director, Mr. Capodieci, its former Senior Fellow, Mr. Spence, and its former Director, Mr. Pakkirisamy, all of whom, on information and belief, participated in developing the Accused Products.

57. GlobalFoundries is further aware of the Asserted Patents and that its Accused Products infringe the Asserted Patents through its receipt of this complaint.

GLOBALFOUNDRIES' INFRINGING DRC+ DESIGN SOLUTIONS SUITE

58. GlobalFoundries makes, uses, tests, sells, offers for sale, and/or imports into the United States, including in this District, products and services that infringe the Asserted Patents (the "Accused Products"), including its DRC+ tool and its open process technology platforms. The Accused Products include a variety of infringing modules and features, which are summarized below. The Accused Products' infringement of the Asserted Patents is set forth in Counts I-IV below.

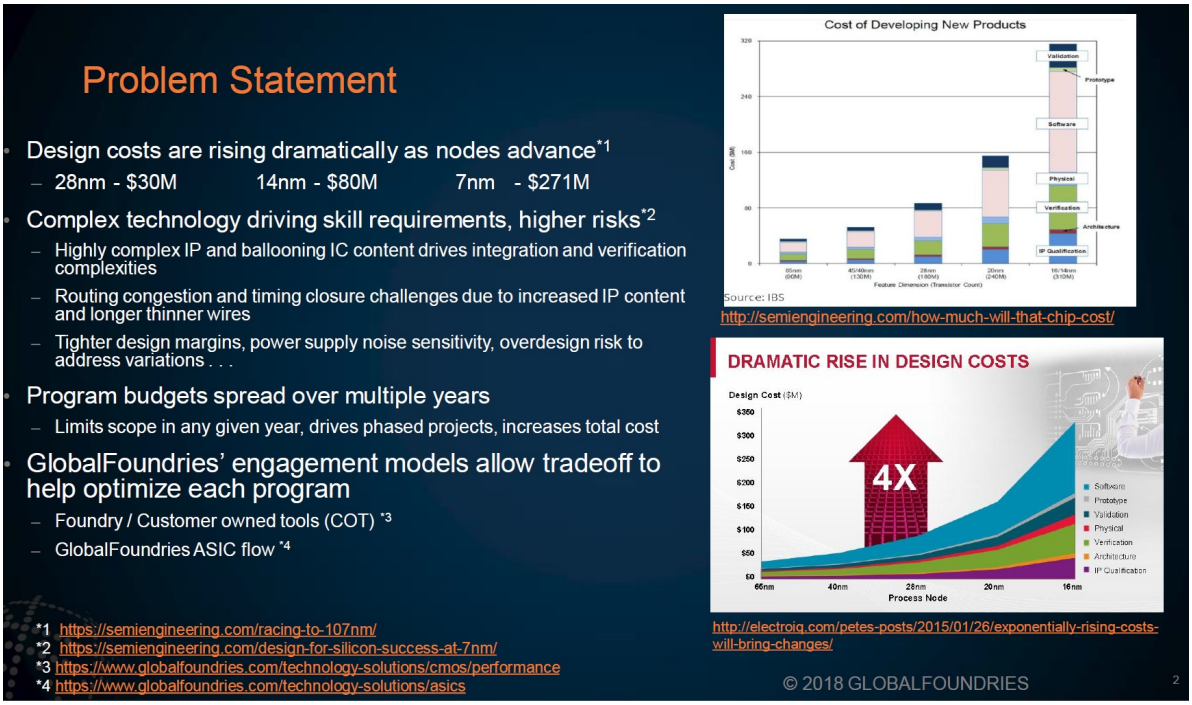
59. GlobalFoundries is a semiconductor contract manufacturing company (often referred to as a "fab"), that manufactures integrated circuits ("ICs") for a variety of customers for a variety of markets, including mobility, automotive, computing, connectivity, Internet of Things, and industrial applications. *See* Ex. 6 at 1-6 (describing GlobalFoundries as a semiconductor manufacturer); Ex. 7 (discussing markets served).

60. The IC design, verification, and manufacturing process flow involves a variety of different functions at different stages, which are referred to as "nodes" in the overall process. Throughout the process, different nodes need to communicate with each other, share design information, and verify design information. Ex. 8 at 1 (discussing traditional foundry design flow issues).

61. One important step in the process is the application of design rule constraints/design rule checking ("DRC"). DRC is the application of a set of geometric rules by a chip fabricator, such as GlobalFoundries, to ensure that a chip design will have a reasonably high yield. Among other things, DRC often involves checking that cells comply with minimum separation rules so that normal manufacturing variation will not result in an excessive number of defective chips. Ex. 9 at 1 (DRC used to ensure physical and electrical manufacturability of

circuits by applying geometric rules to design layouts); Ex. 10 at 1 (discussing DRC as fundamental principles in constraining circuit designs).

62. Each chip fabricator can have its own design rules based on its specific equipment and manufacturing processes. Due to the desire to miniaturize chip designs to the full extent possible, chip designers often seek to use cells in their chip designs which fail DRC but are known to still be operable, which is known as a design rule waiver. As the industry progresses and devices get smaller and smaller, the complexity of the geometric rules needed to ensure the manufacturability of the circuits has become more difficult to define and manufacturing costs have increased. *See* Ex. 9 at 1 (describing the issues with designing and producing smaller and smaller circuits).



Ex. 11 at 2.

63. GlobalFoundries' DRC+ is a pattern-based design for manufacturability ("DFM") tool that is run during the integrated circuit design process. DRC+ provides a pattern-based rule library for identifying and matching 2D layout pattern anomalies that could be difficult to

manufacture. *See* Ex. 9 at 1 (describing DRC+ as having rules that identify problematic patterns that violate constraints and indicate how to fix the error); Ex. 10 at 1 (describing DRC+ as a pattern based rule deck to identify design anomalies); Ex. 12 at 1 (describing DRC+ as a pattern-based DFM tool that uses pattern matching to identify layout configurations).

64. The DRC+ library provides rules to designers comprising of a "yield detracting pattern to avoid" and offers a "recommended DFM rule to follow." Ex. 12 at 1. Designers are then able to fix potential DRC violations by avoiding known problematic patterns, recognizing approving waived violations, and enforcing the given rule to ensure a high yield manufacturing process. *Id.*

65. One way to create a DRC+ rule is to identify hotspots using printability verification simulation, and then craft a DRC+ rule to disallow the problematic pattern in the design. The problematic pattern is flagged with a hotspot marker where the simulated minimum width of the contour at a process corner is less than a manufacturing threshold set by GlobalFoundries. To construct a pattern for the library, the geometries surrounding the marker (in green) are taken into consideration and extracted around the marker, creating the patterns in blue below:

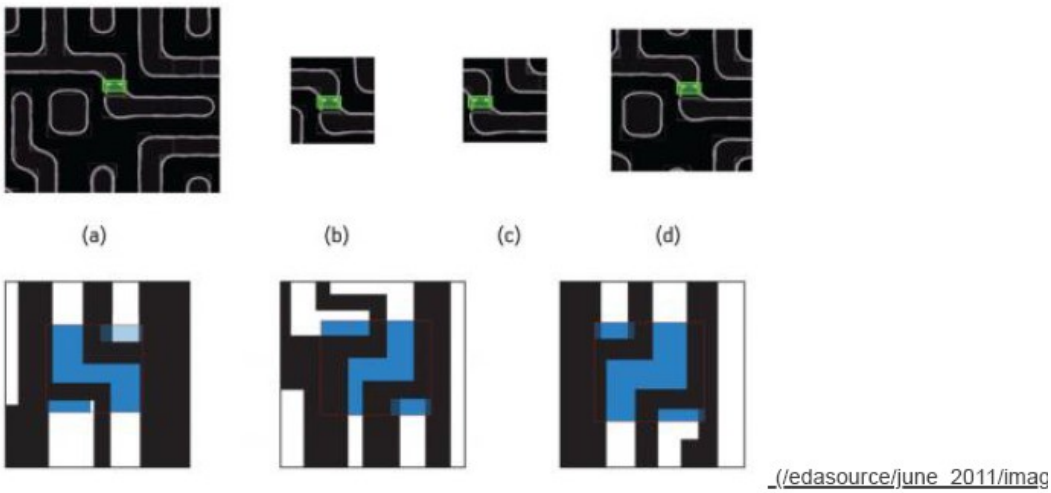


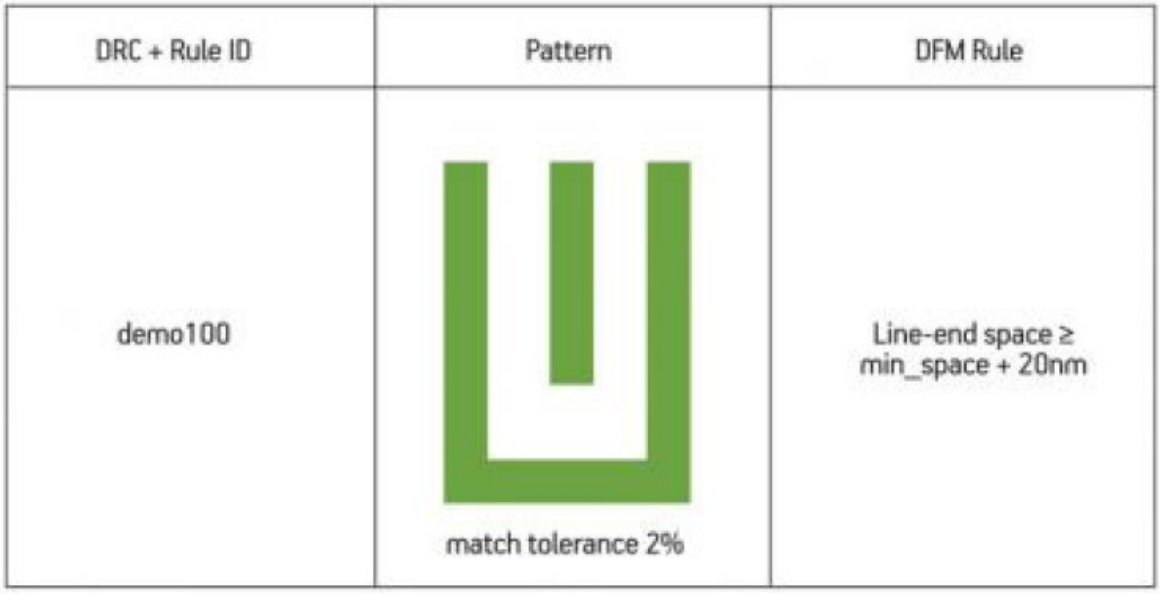
FIGURE 3
Potential DRC+ patterns resulting from (a) hotspot, (b) a small pattern, (c) an off-center pattern, and (d) a large pattern
Source: GlobalFoundries

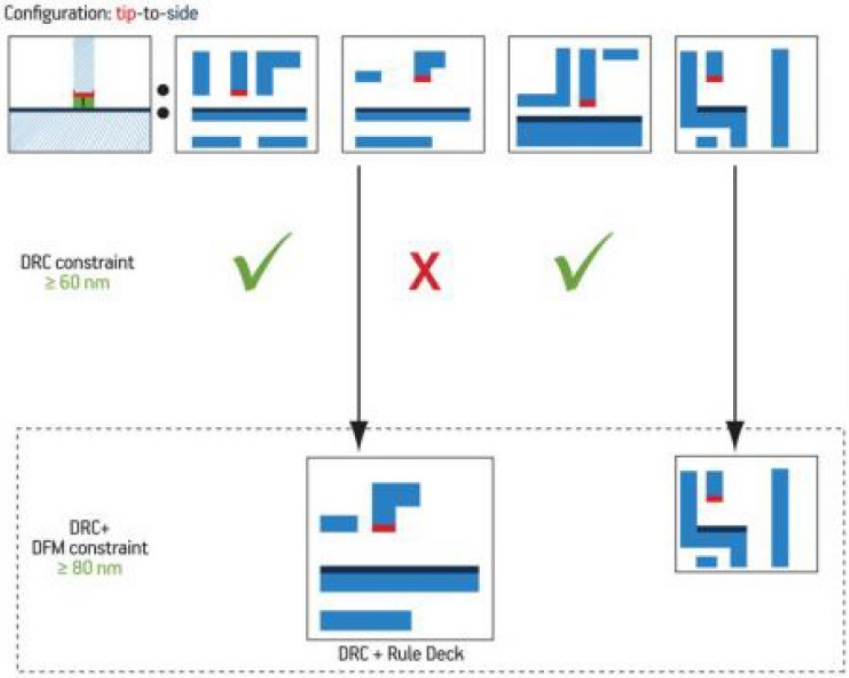
Ex. 9 at 3; Ex. 10 at 2 (DRC+ identifies and analyzes hotspots).

66. Because the process of examining hotspots one at a time can be very time consuming and results in creation of few rules, DRC+ instead uses hotspots as a starting point from the "perspective of design, design style, and design variability to establish at the outset which patterns should be considered for DRC+ rules." Ex. 9 at 3; Ex. 10 at 2; *see also* Ex. 12 at 1 and 4 (DRC+ finds hot spots more efficiently than other techniques).

67. These patterns will cover the design space of a sample layout by construction and can be directly translated into a DRC+ rule so no optimization is necessary to determine what the pattern should be. As a result, DRC+ analysis provides effective screening of hot patterns enablling higher efficiency and yield for the entire chip. *See* Ex. 9 at 3; Ex. 10 at 2 (DRC+ analysis results in "hot patterns").

68. A DRC+ rule enforces a constraint on design geometry, and when the constraint is violated, an error marker is generated with the constraint value, indicating how to fix the error.





Ex. 10 at 2. "In this example, patterns one and three are not considered problem patterns and are not included in the DRC+ deck. The standard constraint is applied and they pass DRC checking. The second pattern matches a DRC+ rule and fails because it does not meet the 80nm constraint, while the last pattern passes since it has sufficient spacing." Ex. 9 at 1-2; *see also* Ex. 10 at 1-2.

69. DRC+ then employs a series of steps to identify pattern configurations by developing situation classes determined by extracting patterns from representative designs to develop a histogram of classes that can be evaluated based upon permutations and occurrences.

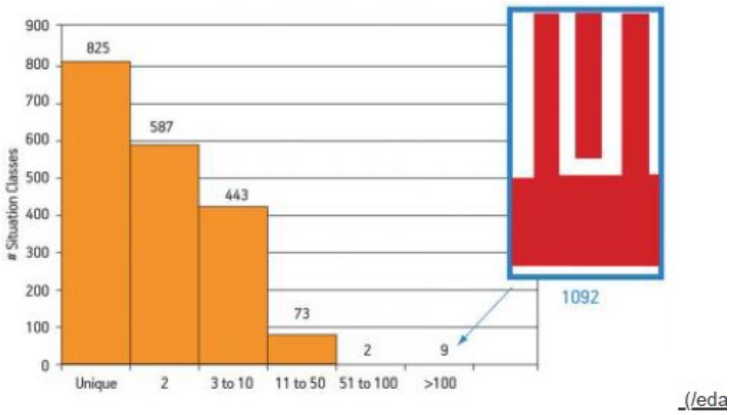
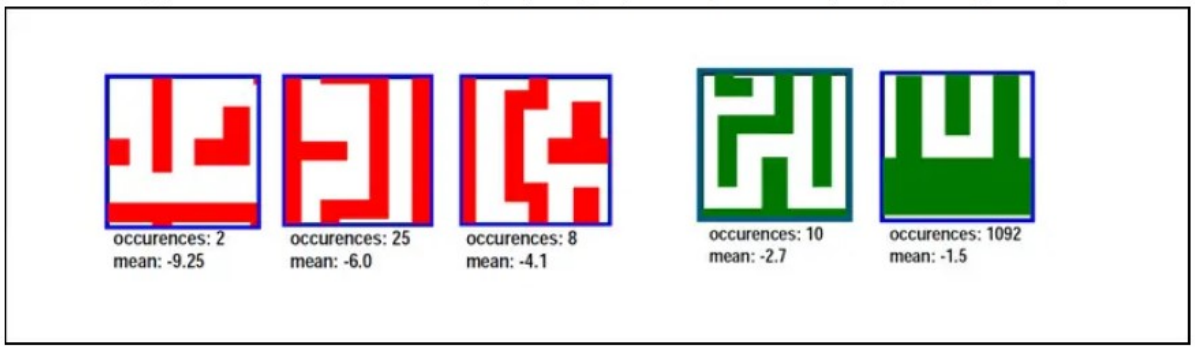


FIGURE 4
Class histogram for the tip-to-side pattern configuration
Source: GlobalFoundries

Ex. 9 at 3; *see also* Ex. 10 at 2.

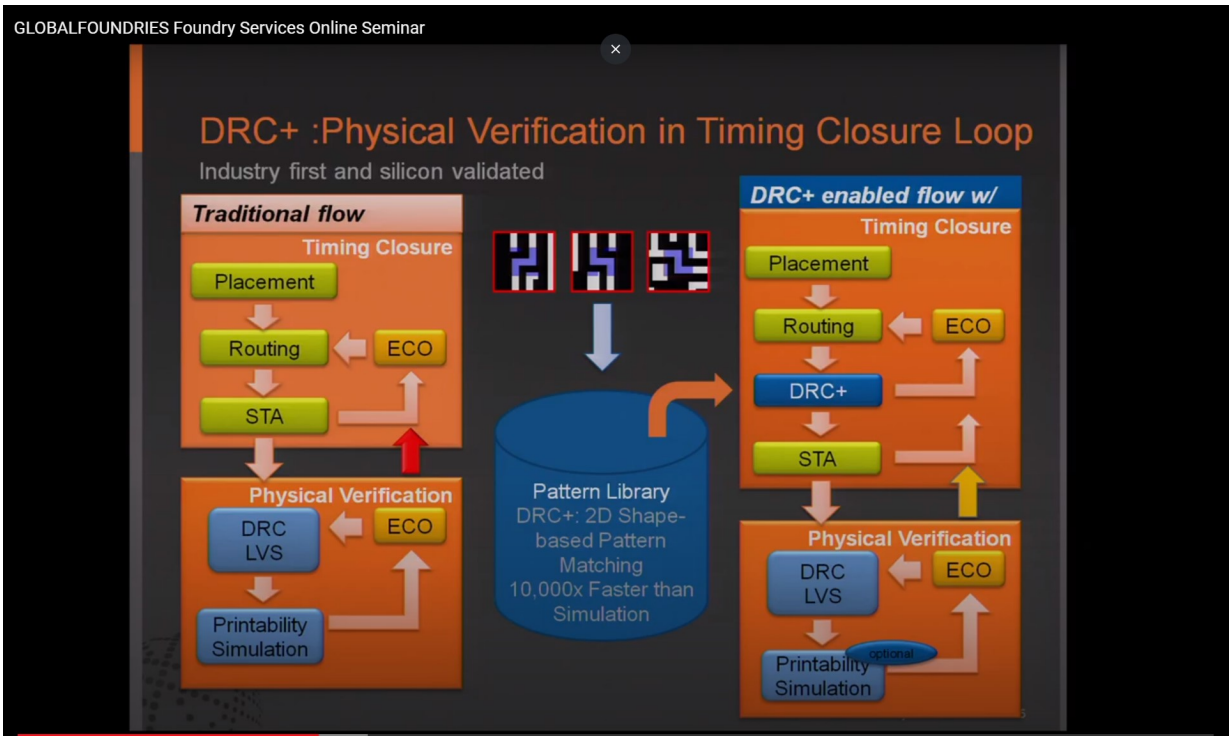
70. Using the graphs provided by DRC+ to determine which classes have lower than average printability, DRC+ is able to identify candidates for potential rules. The printability of each class is determined by a metric called Design-Induced Edge Printing Variability (DIEPV) that represents printing errors over the process window for a given situation. The greater the DIEPV metric, the more likely a printing error is to occur. *See* Ex. 9 at 3-4; Ex. 10 at 2-3.

71. DRC+ uses the statistics derived from measurements of the situation classes as an alternative to simple CD (critical dimension) or EPE (edge placement error) thresholds used in classic printability verification to identify situation classes that have bad printability statistics, to make DRC+ rules.



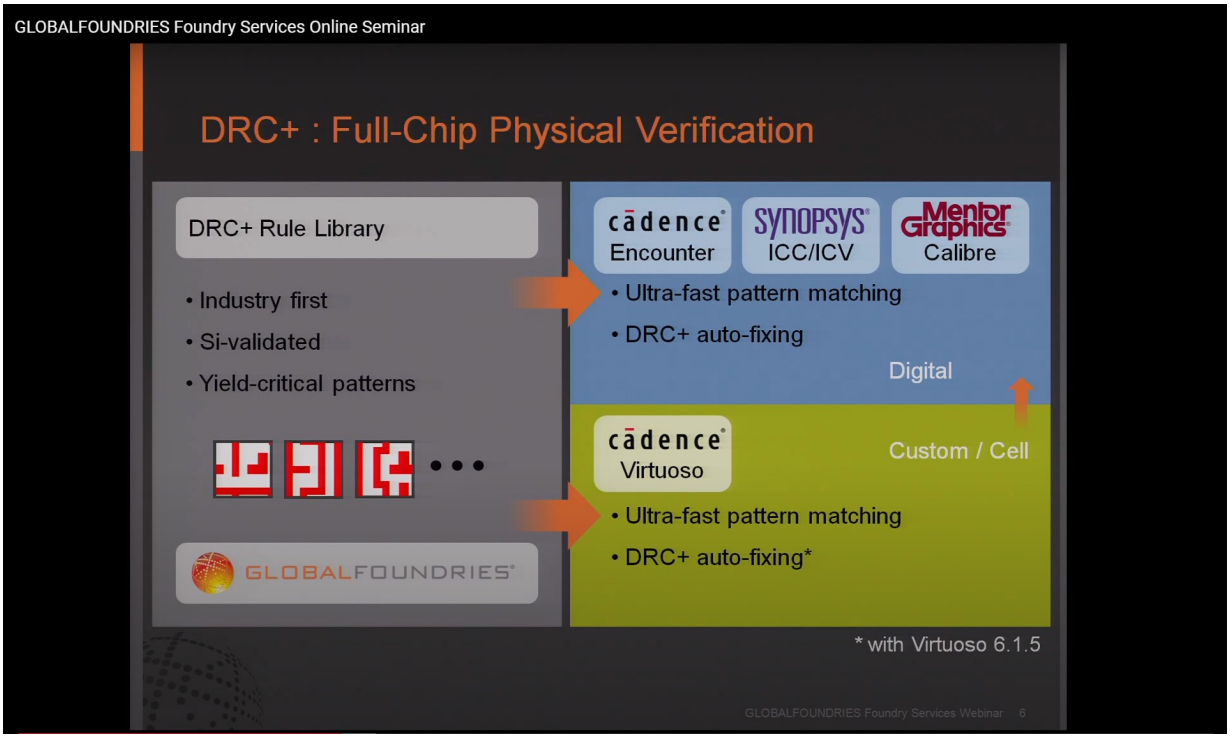
Ex. 10 at 3; *see also* Ex. 9 at 3-5.

72. DRC+ is compatible with various Electronic Design Automation ("EDA") tools used by designers. DRC+ provides designers with the errors triggering the DRC+ rule in question and hints on how to fix the violation. DRC+ normalizes the generated patterns into readable forms so designers can identify and correct potential design variations that violate a design rule. Ex. 10 at 3; *see also* Ex. 9 at 5 (DRC+ is implemented in latest generation of EDA tools).



https://www.youtube.com/watch?v=TFE5p3P74pg (Global Foundries Services Webinar), Slide 5, Screen capture at 06:03.

73. GlobalFoundries reports that DRC+ provides GlobalFoundries with "ultra-fast pattern matching" and "auto-fixing" that significantly cuts down the time and costs required to verify chips' physical designs.



https://www.youtube.com/watch?v=TFE5p3P74pg (Global Foundries Services Webinar), Slide 6, Screen capture at 06:53.

74. DRC+ is part of GlobalFoundries' open process technology platforms that are offered to customers joining GlobalFoundries' Design Enablement Network or as part of process design kits ("PDKs") for existing EDA tools. Ex. 13 at 1 (the Design Enablement Network is composed of the "IP, EDA, Design Services, OSAT and specialized FDX and RF networks."); Ex 17 at 4 (A key element to GlobalFoundries' design enablement and PDK delivery is "a collection of reference flows and design guidelines, which are essential in representing how the

design flow works and for providing recommendations to our clients to get the best results with the PDK.").

75. GlobalFoundries uses its open process technology platforms to manage and exchange IC design information with its customers. Ex. 13 at 1 ("Accelerate the migration to [GlobalFoundries] FDX platforms . . . while reducing design effort to achieve first-time-right results in application-specific hardware.").

76. GlobalFoundries' open process technology platforms interoperate with leading IC design tools, such as Mentor Graphics' Calibre and Cadence Design Systems' software. Ex. 14 at 4 (GlobalFoundries Design Enablement organization's goal is to enable all the EDA tools used by clients: "As part of a reference flow, our team collaborates very closely with EDA vendors to ensure all key features enabling [GlobalFoundries'] differentiated technology are supported in the tools.").

77. GlobalFoundries' open process technology platforms include functionality for a variety of infringing process management tools, including DFM, Layout vs. Schematic Comparisons ("LVS"), Electrical Rule Checking ("ERC"), and Design for Assembly ("DFA") functionality. Ex. 13 at 1 (the Design Enablement Network allows customers to "[d]esign with confidence, reduce turnaround time, costs and risks and differentiate your hardware by leveraging [GlobalFoundries] in-house assets, along with a broad range of validated, platform/application-optimized partner services and solutions."); Ex. 14 (PDKs are a collection of files describing the details of the semiconductor process the EDA tool uses to ensure the foundry can produce the chip that is designed).

COUNT I
(Direct Infringement of the '571 Patent)

78. Oasis repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs, as set forth above.

79. GlobalFoundries has infringed and continues to infringe at least Claim 16 of the '571 Patent in violation of 35 U.S.C. § 271(a) by, among other things, its making, testing, using, importing, selling, and/or offering for sale in the United States the Accused Products.

80. GlobalFoundries' infringement is based upon literal infringement, infringement under the doctrine of equivalents, or both.

81. GlobalFoundries' acts of making, using, testing, importing, selling, and/or offering for sale infringing products and services have been without the permission, consent, authorization, or license of Oasis.

82. The Accused Products infringe at least Claim 16, as set forth above, because they are software with program code stored on non-transitory computer readable storage media for, evaluating similarities and differences between design data files for circuits using the techniques set forth in the Asserted Patents. Ex. 10 at 1 (describing DRC+ as an pattern based application to efficiently identify 2D pattern anomalies); Ex. 13 at 1 (the Design Enablement Network gives customers access to EDA software tools, design IP, design services and OSAT partners); Ex. 14 at 3 (PDKs have "[t]echnology files that describe the relevant design rules, along with design rule checking tools").

83. For example, DRC+ creates a design verification library, including LVS physical verification, used to evaluate the similarities and differences between design data for circuits in order to detect and correct any design anomalies:

> Over the past few years GLOBALFOUNDRIES has developed a novel DFM capability called DRC+ that provides faster design rule verification, several orders of magnitude faster than industry-standard lithography printability simulations [5,6]. At the root of DRC+ is a library of "yield-critical" design patterns stored in a consolidated pattern database (PDB). The criticality metrics are derived based on both process simulations and early silicon learning from electrical/parametric test and advanced inline defect inspection techniques. The verification and update of the criticality of the patterns in the PDB is done during the process window qualification and process set up in the Fab. The critical patterns are provided to the GLOBALFOUNDRIES customers with the DRC+ library decks for layout verification prior to release of customer GDS to GLOBALFOUNDRIES.

Ex. 15 at 1.

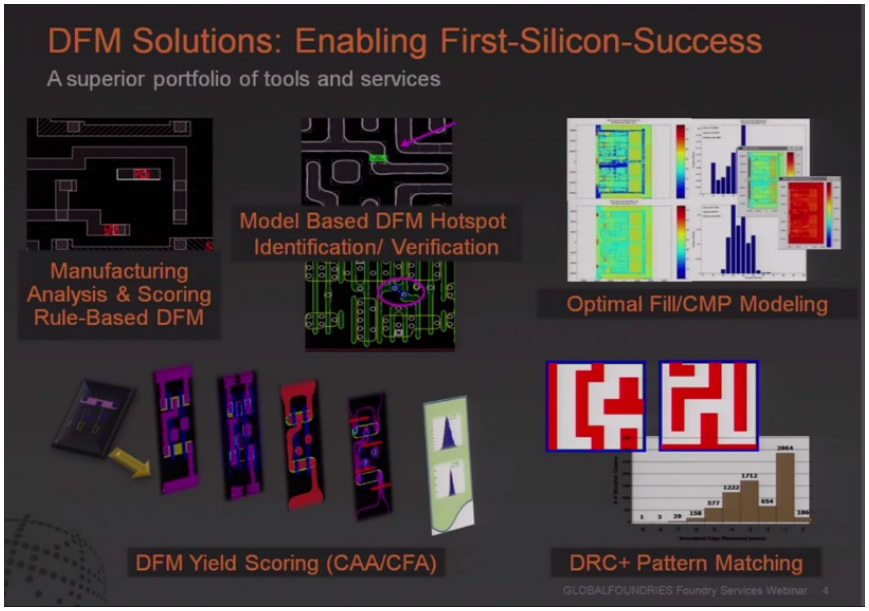
84. The Accused Products receive design files as an input and parse the design file according to the rule set for pattern matching to create one or more syntax trees and store the resulting data in memory. Because reliability checks include geometrical results, a complete waiver process must apply waivers for reliability rules that combine "topological and geometrical information." Ex. 16 at 2.

85. Design waivers are designs that trigger a DRC violation yet are still allowed within the context of the entire design to go forward to manufacturing. In doing so, the syntax tree based on the rule sets is set up to parse the design files into pre-defined formats for verification. *See* Ex. 17 (U.S. 9,032,346 ("*Filippi*")) at 1:22-2:30.

86. The Accused Products use checksums to represent graphical design layout data in canonical form by associating a unique numerical format with the design. *See id.* at 2:5-20, 2:53-3:31. The Accused Products incorporate the methods described in *Filippi*, which is assigned to GlobalFoundries. *Id.* at Cover.

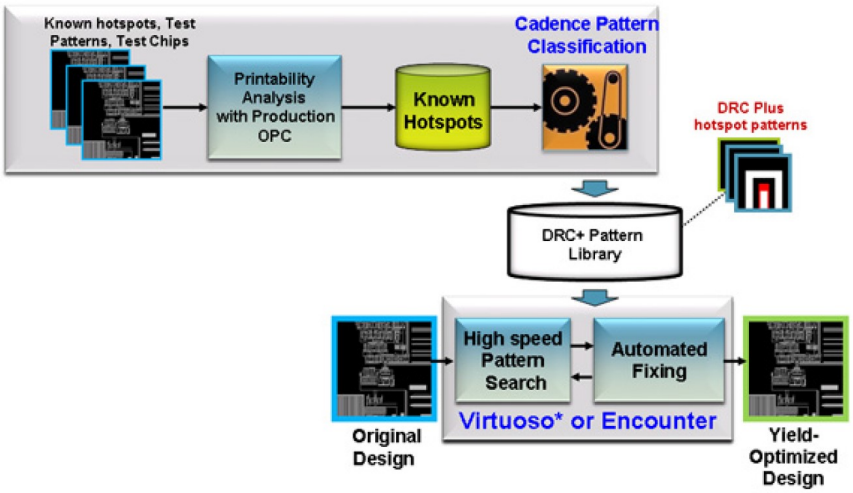
87. *Filippi* explains that an "identifier associated with a cell of the block" can have "one or more checksums corresponding to one or more DRC error" designs in the block. *Id.* at 3:8-12. By storing records of these checksums to a repository, the Accused Products can check if any design triggering an error may be waived via a violation waiver. *Id.* at 6:53-7:7.

88. The Accused Products leverage of pattern matching to identify the design of cells represented in checksums allows the EDA tools to represent the design rule definitions in data formats that are easy to analyze (header and cell partitions). Differentiating waivers for rules by a cell name associated with the rule generating the waived results allows designers to place all waived results within a single GDSII/OASIS layer. Ex. 18 at 2-3 (discussing the waiver process and auto-waiver implementation).

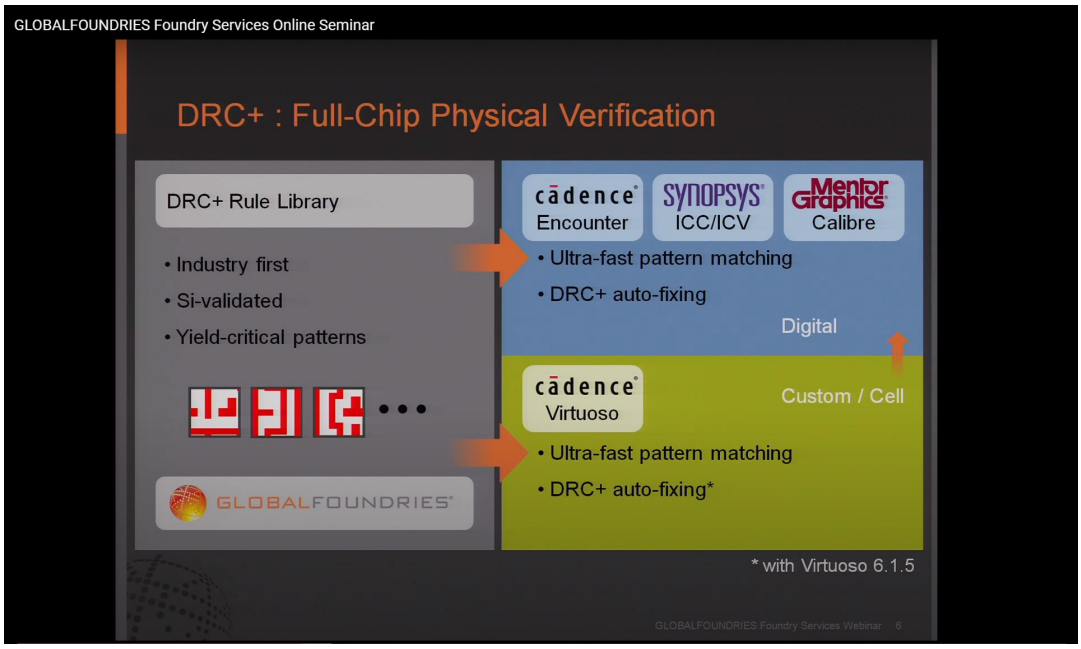


https://www.youtube.com/watch?v=TFE5p3P74pg (Global Foundries Services Webinar), Slide 4, Screen capture at 03:25.

89. The Accused Products compatibility with various EDA tools allows for receipt of the canonical data to be calculated and stored in memory. The received data can then be compared to the known data of acceptable designs stored in the database(s) allowing the Accused Products to provide designers with the design violation and either auto correct the violation or provide ways to fix the violation.



Ex. 12 at 2-3.

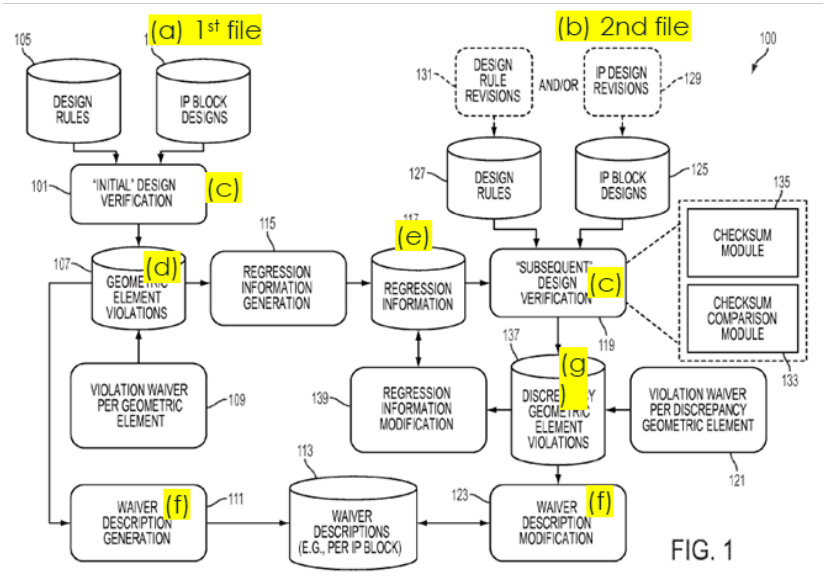


https://www.youtube.com/watch?v=TFE5p3P74pg (Global Foundries Services Webinar), Slide 6, Screen capture at 6:53.

90. The Accused Products manage design verification waivers by "analyzing, based on at least one design rule, layout data corresponding to an integrated circuit including a block of intellectual property having at least one geometric element, generating, if the at least one geometric element violates the at least one design rule, at least one geometric element error,

comparing the at least one geometric element error with waiver information stored in association with a version of the block, and disregarding the at least one geometric element error if the at least one geometric element error corresponds to at least some of the waiver information." *Filippi* at 5:48-58. Thus, DRC+ can compare rule violations against a database of approved waivers for circuit design.

91. As illustrated in *Fillipi* Figure 1, reproduced below, the Accused Products' waiver update process starts with two files stored in the computer memory, the first file (IP block design) (annotated as "a" in the figure below) and the second file (IP Design revisions) ("b"). The Accused Products' initial and subsequent design verification ("c") will parse and normalize the design data in GDSII and OASIS formats into canonical form while non-functional variations are ignored. The geometrics violation ("d") (digest) is calculated and the result is stored in ("e") regression information and ("f") waiver description. The Accused Products also compares and creates geometric violations ("g"), generating reports of the result of the comparison.



Id., FIG. 1 (process for generating waivers, annotated).

92. GlobalFoundries provides a library of design data. Because the library of design data is unique to GlobalFoundries' manufacturing constraints, GlobalFoundries has to repeatedly use, update, and test the Accused Products to ensure its design and manufacturing compatibility is current. Ex. 10 at 1 (DRC+ is a pattern based rule deck provided by GlobalFoundries); Ex. 12 at 2 (DRC+ needs a library of yield-detractor patterns and DFM rules to enforced that are provided by GlobalFoundries); *see also* Ex. 9 at 1 (a good DRC+ rule deck has all 2D patterns that pass DRC but have manufacturability issues).

93. GlobalFoundries' direct infringement of the '571 Patent through at least its use and testing and through offering the Accused Products to its customers has injured and continues to injure Oasis in an amount to be proven at trial, but not less than a reasonable royalty. GlobalFoundries' actions are willful, blatant, and in egregious disregard for Oasis' patent rights.

94. GlobalFoundries' infringement has caused and is continuing to cause damage and irreparable injury to Oasis, and Oasis will continue to suffer damage and irreparable injury unless and until that infringement is enjoined by this Court.

95. GlobalFoundries acted recklessly, willfully, wantonly, and deliberately engaged in acts of infringement of the '571 Patent, justifying an award to Oasis of increased damages under 35 U.S.C. § 284, and attorney's fees and costs incurred under 35 U.S.C. § 285.

COUNT II
(Indirect Infringement of the '571 Patent)

96. Oasis repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs.

97. As discussed above, GlobalFoundries knew about Oasis' patented technology, including the '571 Patent, by no later than February 2010, and further knows about the '571 Patent from its receipt of this Complaint.

98. In addition to directly infringing the '571 Patent, as discussed above with respect to Count I, GlobalFoundries knew or was willfully blind to the fact that it was inducing infringement of at least Claim 1 of the '571 Patent under 35 U.S.C. § 271(b) by instructing, encouraging, directing, and requiring third parties to directly infringe by, in the United States, performing the method of Claim 1 and using the computer-readable medium of Claim 16 by using and installing the Accused Products.

99. GlobalFoundries is also liable for contributory infringement of at least Claim 16 of the '571 Patent under 35 U.S.C. § 271(c) by knowing or being willfully blind to the fact that it was contributing to infringement by providing to its customers and offering to sell and selling in the United States the Accused Products.

100. The Accused Products are software that infringe at least Claim 16 when installed on a computer and are not a staple article or commodity of commerce suitable for substantial non-infringing use. Specifically, as described above, the Accused Products include the parser, normalizer logic, partitioning module, canonical forming module, digester, comparer, and reporter elements recited in Claim 16 and, therefore, necessarily infringe when they are placed on computer-readable storage media. Ex. 10 at 1 (describing DRC+ as a pattern based application to efficiently identify 2D pattern anomalies); Ex. 13 at 1 (the Design Enablement Network gives customers access to GlobalFoundries' optimized EDA software tools, design IP, design services and OSAT partners); Ex. 14 at 3 (PDKs have "[t]echnology files that describe the relevant design rules, along with design rule checking tools").

101. GlobalFoundries knowingly and actively encouraged, aided and abetted, and contributed to the direct infringement of the '571 Patent by instructing and encouraging its customers, developers, and partners to use and install the Accused Products, including through

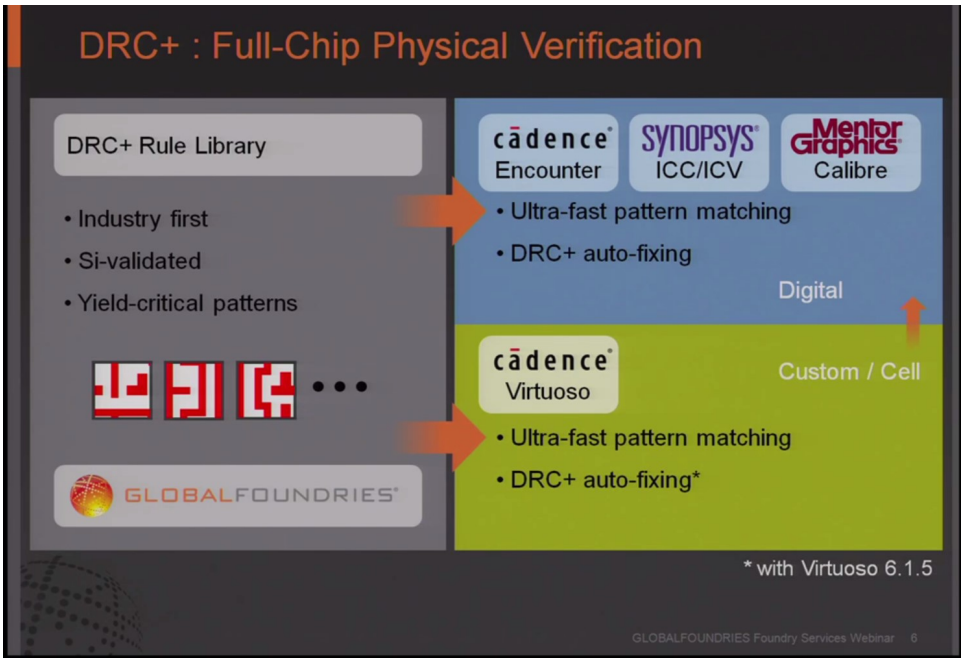
its Design Enablement Network and its offering of PDKs, requiring designers such as Mentor Graphics, Cadence, and others to integrate it into their EDA tools in order to use GlobalFoundries as a manufacturer.

Does GLOBALFOUNDRIES require DRC+?

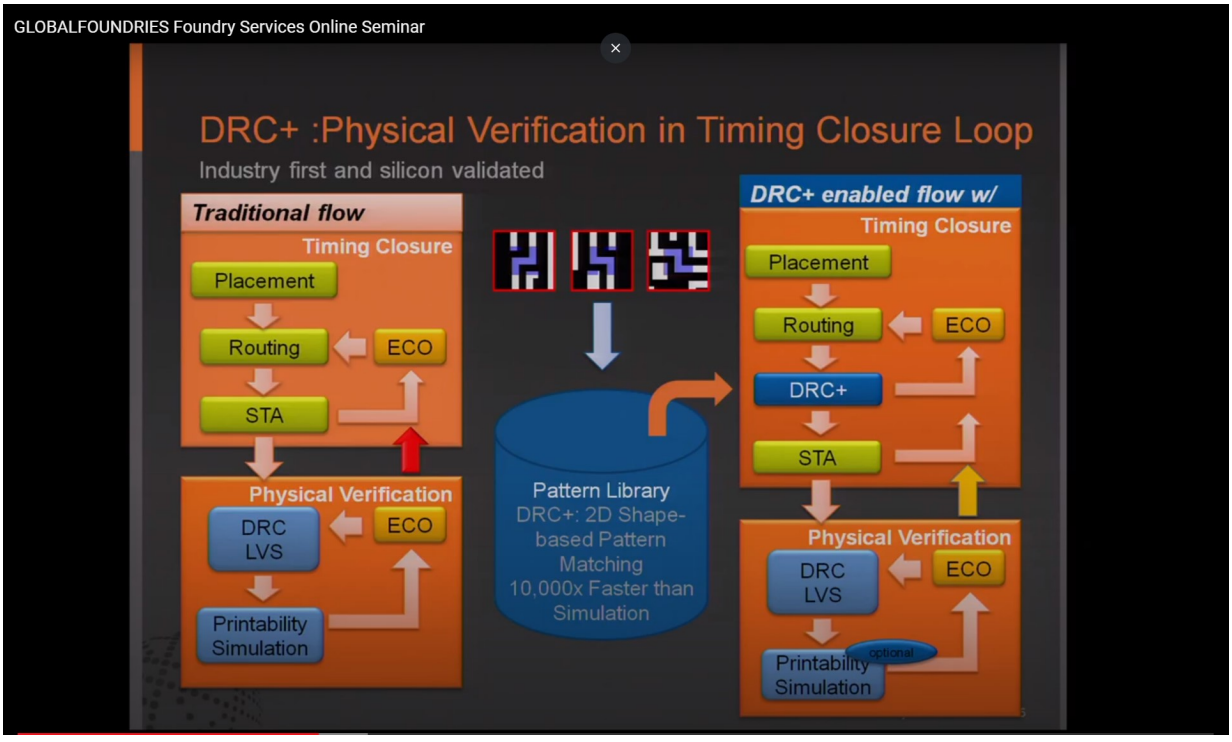
It will be a requirement for 28nm and below. "We are currently evaluating going back to 40 nm," Vito said.

Ex. 12 at 2; *see also* Ex. 13 at 1(customers gain access to "[GlobalFoundries] in-house assets along with a broad range of validated, platform/application-optimized partner services and solutions"); Ex. 14 at 4 (GlobalFoundries' Design Enablement organization's goal is to enable all the EDA tools used by clients).

102. The Accused Products are designed to be integrated with EDA tools where they enhance the pattern-matching capabilities of the EDA tools to identify similarities and differences in design files. The Accused Products provide EDA tools instructions stored in its system memory to conduct pattern matchings using printability rules for design purposes. Ex. 12 at 2 (stating that DRC+ needs a library of yield-detractor patterns and DFM rules to enforce); Ex. 14 at 4 ("As part of a reference flow, our team collaborates very closely with EDA vendors to ensure all key features enabling [GlobalFoundries'] differentiated technology are supported in the tools.").



https://www.youtube.com/watch?v=TFE5p3P74pg (Global Foundries Services Webinar), Slide 6, Screen capture at 06:53 (showing use of EDA tools for pattern matching).



Id. at Slide 5, Screen capture at 06:03.

103. GlobalFoundries' indirect infringement of the '571 Patent has injured and continues to injure Oasis in an amount to be proven at trial, but not less than a reasonable royalty. GlobalFoundries' actions are willful, blatant, and in egregious disregard for Oasis' patent rights.

104. GlobalFoundries' indirect infringement has caused and is continuing to cause damage and irreparable injury to Oasis, and Oasis will continue to suffer damage and irreparable injury unless and until that infringement is enjoined by this Court.

105. GlobalFoundries acted recklessly, willfully, wantonly, and deliberately engaged in acts of indirect infringement of the '571 Patent, justifying an award to Oasis of increased damages under 35 U.S.C. § 284, and attorney's fees and costs incurred under 35 U.S.C. § 285.

COUNT III
(Direct Infringement of the '545 Patent)

106. Oasis repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs, as set forth above.

107. GlobalFoundries has infringed and continues to infringe at least Claim 14 of the '545 Patent in violation of 35 U.S.C. § 271(a) by, among other things, making, using, importing, selling, and/or offering for sale in the United States the Accused Products.

108. GlobalFoundries' infringement is based upon literal infringement, infringement under the doctrine of equivalents, or both.

109. GlobalFoundries' acts of making, using, testing, importing, selling, and/or offering for sale infringing products and services have been without the permission, consent, authorization, or license of Oasis.

110. The Accused Products infringe at least Claim 14, as set forth above, because they are software with program code stored on non-transitory computer readable storage media for

evaluating similarities and differences between design data files for circuits using the techniques set forth in the Asserted Patents. Ex. 10 at 1 (describing DRC+ as an pattern based application to efficiently identify 2D pattern anomalies); Ex. 13 at 1 (the Design Enablement Network gives customers access to EDA software tools, design IP, design services and OSAT partners); Ex. 14 at 3 (PDKs have "[t]echnology files that describe the relevant design rules, along with design rule checking tools").

111. For example, DRC+ creates a design verification library, including LVS, used to evaluate the similarities and differences between design data for circuits in order to detect and correct design anomalies:

> Over the past few years GLOBALFOUNDRIES has developed a novel DFM capability called DRC+ that provides faster design rule verification, several orders of magnitude faster than industry-standard lithography printability simulations [5,6]. At the root of DRC+ is a library of "yield-critical" design patterns stored in a consolidated pattern database (PDB). The criticality metrics are derived based on both process simulations and early silicon learning from electrical/parametric test and advanced inline defect inspection techniques. The verification and update of the criticality of the patterns in the PDB is done during the process window qualification and process set up in the Fab. The critical patterns are provided to the GLOBALFOUNDRIES customers with the DRC+ library decks for layout verification prior to release of customer GDS to GLOBALFOUNDRIES.

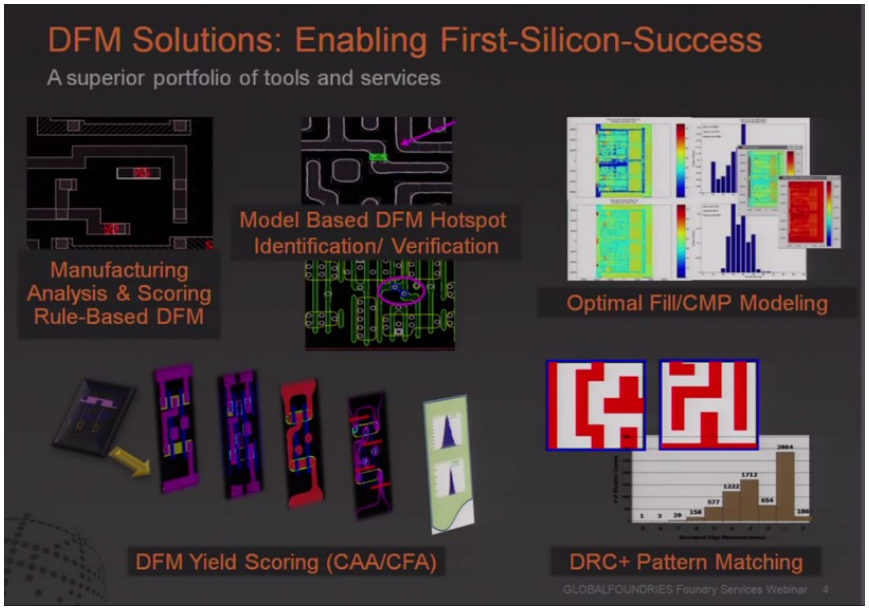
Ex. 15 at 1.

112. The Accused Products receive design files as an input and parse the design file according to the rule set for pattern matching to create one or more syntax trees and stores in memory. Because reliability checks include geometrical results, a complete waiver process of allowable designs that trigger a rule violation must apply waivers for reliability rules that combine "topological and geometrical information." Ex. 16 at 2. In doing so, the syntax tree based on the rule sets is set up to parse the design files into pre-defined formats for verification.

113. The Accused Products use checksums to represent graphical design layout data in canonical form by associating a unique numerical format with the design. *See Filippi* at 2:5-20,

2:53-3:31. An "identifier associated with a cell of the block" can have "one or more checksums corresponding to one or more DRC error" designs in the block. *Id.* at 3:8-12. By storing records of these checksums to a repository, the Accused Products can check if any design triggering an error may be waived via a violation waiver. *Id.* at 6:53-7:7.

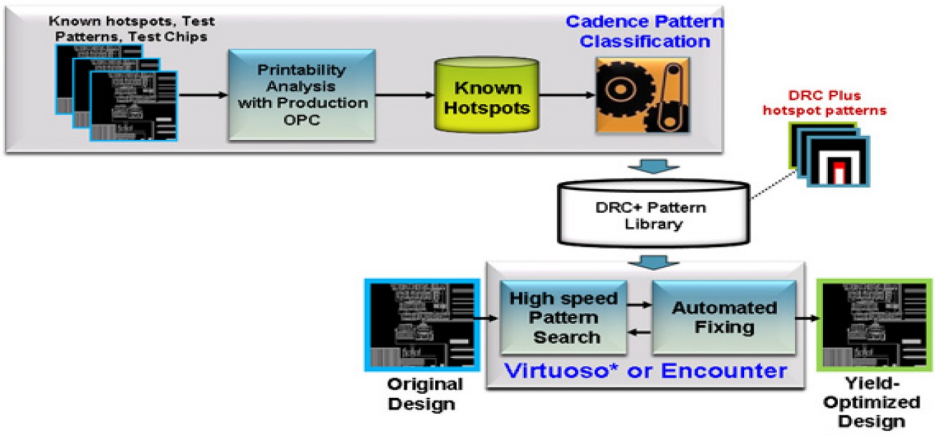
114. The Accused Products leverage pattern matching to identify the design of cells represented in checksums allows the EDA tools to represent the design rule definitions in data formats that are easy to analyze (header and cell partitions). Differentiating waivers for rules by a cell name associated with the rule generating the waived results allows designers to place all waived results within a single GDSII/OASIS layer. Ex. 18 at 2-3 (discussing the waiver process and auto-waiver implementation).



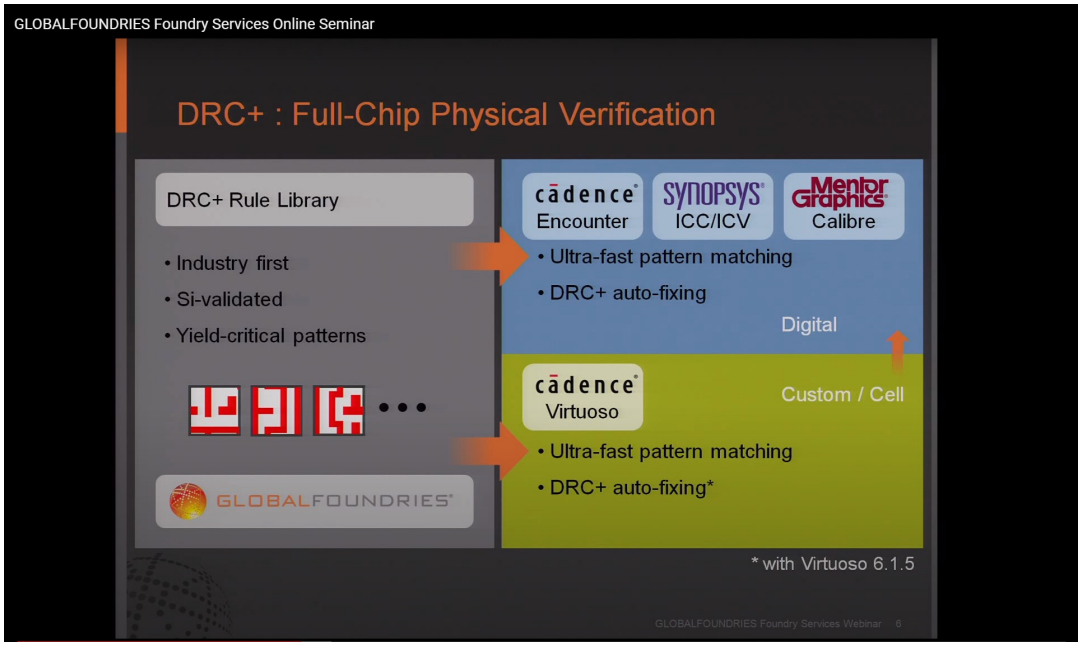
https://www.youtube.com/watch?v=TFE5p3P74pg (Global Foundries Services Webinar), Slide 4, Screen capture at 03:25.

115. The Accused Products' compatibility with various EDA tools allows for receipt of the canonical data to be calculated and stored in memory. The received data can then be compared to the known data of acceptable designs stored in the database(s) allowing the Accused

Products to provide designers with the design violation and either auto correct the violation or provide ways to fix the violation.



Ex. 12 at 2-3;

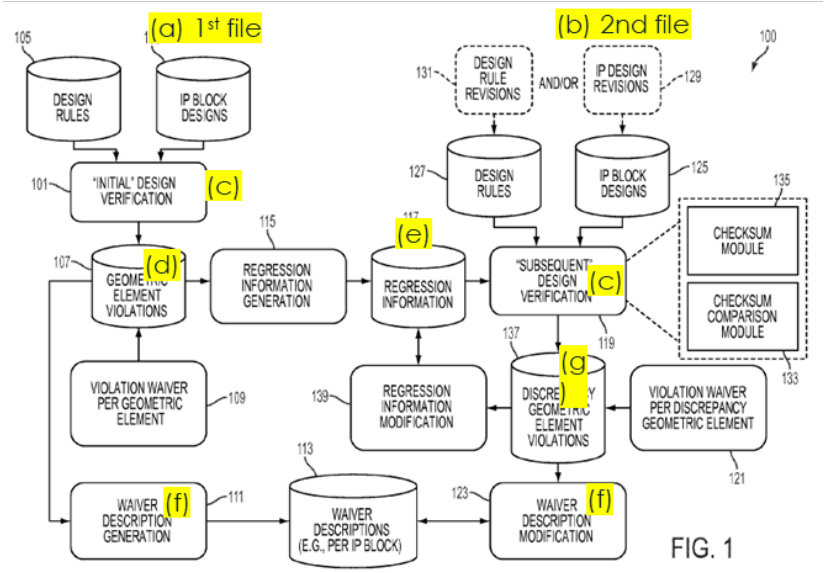


https://www.youtube.com/watch?v=TFE5p3P74pg (Global Foundries Services Webinar), Slide 4, Screen capture at 03:25.

116. The Accused Products manage design verification waivers by "analyzing, based on at least one design rule, layout data corresponding to an integrated circuit including a block of intellectual property having at least one geometric element, generating, if the at least one

geometric element violates the at least one design rule, at least one geometric element error, comparing the at least one geometric element error with waiver information stored in association with a version of the block, and disregarding the at least one geometric element error if the at least one geometric element error corresponds to at least some of the waiver information." *Filippi* at 5:48-58. Thus, DRC+ can compare rule violations against a database of approved waivers for circuit design.

117. As illustrated in *Fillipi* Figure 1, reproduced below, the Accused Products' waiver update process starts with two files stored in the computer memory, the first file (IP block design) (annotated as "a" in the figure below) and the second file (IP Design revisions) ("b"). The Accused Products initial and subsequent design verification ("c") will parse and normalize the design data in GDSII and OASIS formats while non-functional variations are ignored. The geometrics violations ("d") (digest) is calculated and the result is stored in regression information ("e") and waiver description ("f"). The Accused Products also compare and create geometric violations ("g"), generating reports of the result of the comparison.



Id., FIG. 1 (process for generating waivers, annotated)

118. GlobalFoundries provides a library of design data. Because the library of design data is unique to GlobalFoundries manufacturing constraints, GlobalFoundries has to repeatedly use, update, and test the Accused Products to ensure its design and manufacturing compatibility is current. Ex. 10 at 1 (DRC+ is a pattern based rule deck provided by GlobalFoundries); Ex. 12 at 2 (DRC+ needs a library of yield-detractor patterns and DFM rules to enforced that are provided by GlobalFoundries); *see also* Ex. 9 at 1 (a good DRC+ rule deck has all 2D patterns that pass DRC but have manufacturability issues).

119. GlobalFoundries' direct infringement of the '545 Patent has injured and continues to injure Oasis in an amount to be proven at trial, but not less than a reasonable royalty. GlobalFoundries' actions are willful, blatant, and in egregious disregard for Oasis' patent rights.

120. GlobalFoundries' infringement has caused and is continuing to cause damage and irreparable injury to Oasis, and Oasis will continue to suffer damage and irreparable injury unless and until that infringement is enjoined by this Court.

121. GlobalFoundries acted recklessly, willfully, wantonly, and deliberately engaged in acts of infringement of the '545 Patent, justifying an award to Oasis of increased damages under 35 U.S.C. § 284, and attorney's fees and costs incurred under 35 U.S.C. § 285.

COUNT IV
(Indirect Infringement of the '545 Patent)

122. Oasis repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs.

123. As discussed above, GlobalFoundries knew about Oasis' patented technology, including the '545 Patent, by no later than February 2010, and further knows about the '545 Patent from its receipt of this Complaint.

124. In addition to directly infringing the '545 Patent, as discussed above with respect to Count III, GlobalFoundries knew or was willfully blind to the fact that it was inducing infringement of at least Claim 1 of the '545 Patent under 35 U.S.C. § 271(b) by instructing, encouraging, directing, and requiring third parties in the United States to perform the method of Claim 1 by using and installing the Accused Products.

125. GlobalFoundries is also liable for contributory infringement of at least Claim 14 of the '545 Patent under 35 U.S.C. § 271(c) by knowing or being willfully blind to the fact that it was contributing to infringement by providing to its customers and offering to sell and selling in the United States the Accused Products.

126. The Accused Products are software that infringe at least Claim 14 when installed on a computer device having at least one processor and memory and are not a staple article or commodity of commerce suitable for substantial noninfringing use. Specifically, as described above, the Accused Products include the parser, normalizer logic, digester module, comparer module, and reporter module elements recited in Claim 14 and, therefore, necessarily infringe when they are installed on a compatible computer containing a processor and memory. Ex. 10 at 1 (describing DRC+ as an pattern based application to efficiently identify 2D pattern anomalies); Ex. 13 at 1 (the Design Enablement Network gives customers access to GlobalFoundries' optimized EDA software tools, design IP, design services and OSAT partners); Ex. 14 at 3 (PDKs have "[t]echnology files that describe the relevant design rules, along with design rule checking tools").

127. GlobalFoundries knowingly and actively encouraged, aided and abetted, and contributed to the direct infringement of the '545 Patent by instructing and encouraging its customers, developers, and partners to use and install the Accused Products, including through

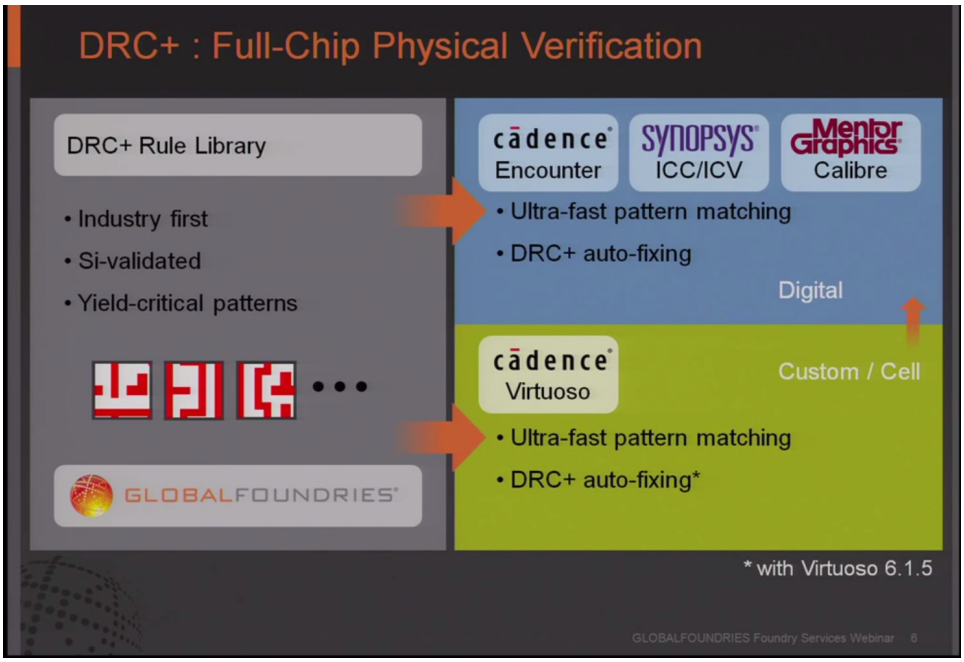
its Design Enablement Network and its offering of PDKs, requiring designers such as Mentor Graphics, Cadence, and others to integrate it into their EDA tools in order to use GlobalFoundries as a manufacturer.

Does GLOBALFOUNDRIES require DRC+?

It will be a requirement for 28nm and below. "We are currently evaluating going back to 40 nm," Vito said.

Ex. 12 at 2; *see also* Ex. 13 at 1(customers gain access to "[GlobalFoundries] in-house assets along with a broad range of validated, platform/application-optimized partner services and solutions"); Ex. 14 at 4 (GlobalFoundries' Design Enablement organization's goal is to enable all the EDA tools used by clients).

128. The Accused Products are designed to be integrated with EDA tools where they enhance the pattern-matching capabilities of the EDA tools to identify similarities and differences in design files. The Accused Products provide EDA tools instructions stored in its system memory to conduct pattern matchings using printability rules for design purposes. Ex. 12 at 2 (stating that DRC+ needs a library of yield-detractor patterns and DFM rules to enforce); Ex. 14 at 4 ("As part of a reference flow, our team collaborates very closely with EDA vendors to ensure all key features enabling [GlobalFoundries'] differentiated technology are supported in the tools.").



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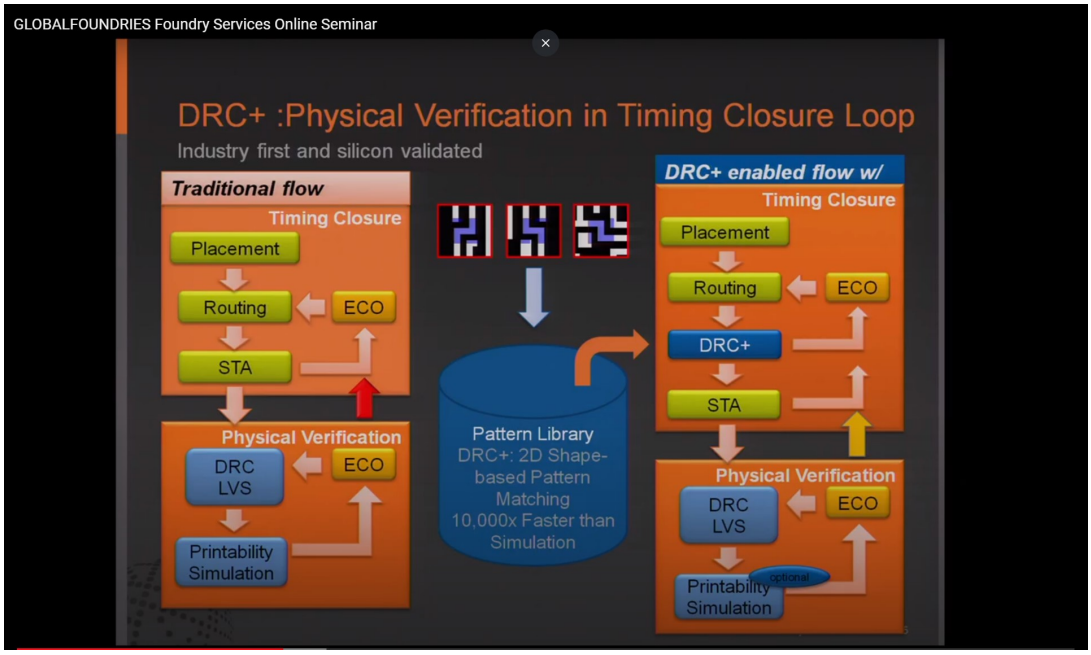

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129. GlobalFoundries' indirect infringement of the '545 Patent has injured and continues to injure Oasis in an amount to be proven at trial, but not less than a reasonable royalty. GlobalFoundries' actions are willful, blatant, and in egregious disregard for Oasis' patent rights. GlobalFoundries' indirect infringement has caused and is continuing to cause damage and irreparable injury to Oasis, and Oasis will continue to suffer damage and irreparable injury unless and until that infringement is enjoined by this Court.

130. GlobalFoundries acted recklessly, willfully, wantonly, and deliberately engaged in acts of indirect infringement of the '545 Patent, justifying an award to Oasis of increased damages under 35 U.S.C. § 284, and attorney's fees and costs incurred under 35 U.S.C. § 285.

PRAYER FOR RELIEF

WHEREFORE, Oasis prays for judgment and relief as follows:

A. an entry of judgment holding that GlobalFoundries has infringed and is infringing the '571 Patent and the '545 Patent; and has induced infringement and is inducing infringement of the '571 Patent and the '545 Patent; and/or has contributorily infringed and continues to contribute to infringement of the '571 Patent and the '545 Patent;

B. a preliminary and permanent injunction against GlobalFoundries and its officers, employees, agents, servants, attorneys, instrumentalities, and/or those in privity with them, from infringing, inducing, or contributing to the infringement of the '571 Patent and the '545 Patent and for all further and proper injunctive relief pursuant to 35 U.S.C. § 283;

C. an award to Oasis of such damages as it shall prove at trial against GlobalFoundries that is adequate to fully compensate Oasis for GlobalFoundries' infringement of the '571 Patent and the '545 Patent—said damages to be no less than a reasonable royalty;

D. a determination that GlobalFoundries' infringement has been willful, wanton, and deliberate, and that the damages against it be trebled on this basis or for any other basis in accordance with the law;

E. an award to Oasis of increased damages under 35 U.S.C. § 284, including because GlobalFoundries willfully infringed the '571 Patent and the '545 Patent;

F. a finding that this case is "exceptional" and an award to Oasis of its costs and reasonable attorneys' fees, as provided by 35 U.S.C. § 285;

G. an accounting of all infringing sales and revenues, together with post-judgment interest and prejudgment interest from the date of first infringement of the '571 Patent and the '545 Patent; and

H. such further and other relief as the Court may deem proper and just.

DEMAND FOR JURY TRIAL

Oasis demands a jury trial on all issues so triable.

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Dated: March 9, 2022
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