IN THE UNITED STATES DISTRICT COURT

DISTRICT OF DELAWARE

POLARIS INNOVATIONS LIMITED., an Ireland limited company, Plaintiff, v. XILINX, INC., a Delaware corporation Defendant.	No. **DEMAND FOR JURY TRIAL**

COMPLAINT FOR PATENT INFRINGEMENT

Polaris Innovations Limited ("Polaris") files this Complaint against Xilinx, Inc. ("Xilinx"), for patent infringement as follows:

PARTIES

1. Plaintiff Polaris Innovations Limited is a corporation organized and existing under the law of Ireland, with its principal place of business at 77 Lower Camden Street, Dublin D02 XE80, Ireland.

2. Upon information and belief, Xilinx is a corporation organized and existing under the law of Delaware with its principal place of business at 2100 Logic Drive, San Jose, CA 95124. Xilinx may be served with process through its registered agent, the Corporation Service Company, 251 Little Falls Drive, Wilmington, Delaware 19808.

JURISDICTION

3. This is an action for patent infringement arising under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

4. This Court has personal jurisdiction over Xilinx. Xilinx is a Delaware corporation. Upon information and belief, Xilinx has committed and continues to commit acts of

patent infringement, including making, selling, offering to sell, directly or through intermediaries, subsidiaries and/or agents, infringing products within this district, including to customers in this district.

VENUE

5. Venue is proper in this Court pursuant to 28 U.S.C. § 1400 (b). Xilinx is subject to personal jurisdiction in this district, and a substantial part of the events giving rise to Polaris's claims occurred in this district.

THE ASSERTED PATENTS

6. On December 5, 2000, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 6,157,589 ("the '589 patent"), entitled "Dynamic semiconductor memory device and method for initializing a dynamic semiconductor memory device." A copy of the '589 patent is attached hereto as Exhibit 1.

7. The '589 patent has been assigned to Polaris. Polaris holds all right, title, and interest in the '589 Patent, including the right to collect and receive damages for past, present and future infringement of the '589 Patent.

8. On December 5, 2006, the United States Patent and Trademark office duly and legally issued United States Patent No. 7,145,369 (the "'369 patent"), which is entitled "Output Driver For An Integrated Circuit And Method For Driving An Output Driver." A true and correct copy of the '369 patent is attached hereto as Exhibit 2.

9. The '369 patent has been assigned to Polaris. Polaris holds all right, title, and interest in the '369 patent, including the right to collect and receive damages for past, present, and future infringement of the '369 patent.

10. On May 12, 2009, the United States Patent and Trademark Office duly and legally issued United States Patent No. 7,532,523 ("the '523 patent"), which is entitled "Memory Chip With Settable Termination Resistance Circuit." A true and correct copy of the '523 Patent is attached hereto as Exhibit 3.

11. The ’523 Patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the ’523 Patent, including the right to collect and receive damages for past, present and future infringement of the ’523 Patent.

12. On March 2, 2004, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,702,473, entitled “Electrical Circuit And Method For Testing A Circuit Component Of The Electrical Circuit.” A true and correct copy of the ’473 patent is attached hereto as Exhibit 4.

13. The ’473 patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the ’473 Patent, including the right to collect and receive damages for past, present and future infringement of the ’473 Patent.

XILINX’S INFRINGING PRODUCTS

14. Polaris incorporates and realleges paragraphs 1-13 above as though fully set forth herein.

15. Xilinx is the industry leader in field-programmable gate arrays (“FPGA”).

16. According to Xilinx, “Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks.” https://www.xilinx.com/products/silicon-devices/fpga/what-is-an-fpga.html (Last accessed February 8, 2022).

17. Xilinx touts the wide applicability of its FPGAs, including aerospace & defense, ASIC prototyping, automotive, broadcast systems, consumer electronics, data center, high performance computing and data storage, industrial, medical, security, video and image processing, and wired and wireless communications applications.

18. Examples of Xilinx’s products include the Zynq Ultrascale+ MPSoC, Zynq-7000 SoC, the UltraScale product family, the 7-series product family, the 6-series product family,

Virtex-6 and Virtex-5 product families, and the Spartan-6 product family.

19. In addition to its FPGA devices, Xilinx also provides "advanced software" and "configurable, ready-to-use IP cores" for each such application of its FPGA devices. These tools allow the user to design, program, simulate, and test the desired configuration for the FPGA.

20. Xilinx's system on a chip ("SoC") products, such as the Zynq Ultrascale+ MPSoC, Zynq-7000 SoC, and the UltraScale product family incorporate memory controllers. Others, such as the 7-series product family, the 6-series product family, Virtex-6 and Virtex-5 product families, and the Spartan-6 product family, can be programmed to implement memory interface solutions between the FPGA and external DRAM, such as by using Xilinx's Memory Interface Generator tool, or other design tools provided by Xilinx.

COUNT I

(Infringement of U.S. Patent 6,157,589)

21. Polaris incorporates and realleges paragraphs 1-20 above as though fully set forth herein.

22. On information and belief, up until the expiration of the '589 patent, Xilinx willfully infringed one or more claims of the '589 patent, including, but not limited to, claims 11, 12, and 13 of the '589 patent literally, or under the doctrine of equivalents, by using in the United States without authority, products containing a Dynamic Memory Interface compatible with DDR3, DDR3L, and DDR4 memory, including but not limited to Zynq Ultrascale+ MPSoC, Zynq-7000 SoC, the UltraScale product family, and the 7-series product family (collectively, "'589 patent Infringing Products"). The '589 patent Infringing Products perform the claimed methods for initializing a dynamic semiconductor memory device.

23. On information and belief, when Xilinx, its customers, and other third parties turn on the '589 Patent Infringing Products, their memory controllers supply, via an initialization circuit, a supply voltage stable signal (for example, the ddr_reset_n or *RESET#* signal,) once a supply voltage has been stabilized (for example, at the time between Ta and the assertion of the RESET# signal) after the switching-on operation of the dynamic semiconductor memory device

(for example, in the "Reset Procedure" state which follows the "Power ON" state, and *RESET#* must be HIGH during normal operation). The controller chip also supplies, via an enable circuit of the initialization circuit, an enable signal (for example, the ddr_cke signal), the initialization circuit receiving the supply voltage stable signal (for example, the memory controller receives the *RESET#* signal) and further command signals (for example, the "MRS" signals) externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals (for example ZQ Calibration commands) the enable signal being generated and effecting an unlatching of a control circuit (for example, as indicated by the generation of the VALID signals generated on the CKE, COMMAND, CA, and ODT lines).

24. On information and belief, the controller provides at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals (for example, the MRS command, which acts both as a preparation command signal and as a loading configuration register command signal.)

25. On information and belief, the controller maintains a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit (for example, as seen in the state of the RTT line during the switching-on operation).

26. On information and belief, Xilinx induced infringement of one or more claims of the '589 Patent, including, but not limited to, Claims 11, 12, and 13, pursuant to 35 U.S.C. § 271(b), by encouraging its customers and other third parties to perform the claimed method for initializing a dynamic semiconductor memory device. This performance of the claimed method for initializing a dynamic semiconductor memory device, constitutes infringement, literally or under the doctrine of equivalents, of one or more claims of the '589 patent by such customers or

third parties. Xilinx's acts of inducement include: providing its customers with the '589 Patent Infringing Products and intending its customers to use the '589 Patent Infringing Products with hardware, software, and other infrastructure that enable and/or make use of these products; advertising these products through its own and third-party websites; and providing instructions on how to use these products.

27. Xilinx proceeded in this manner despite its actual knowledge of the '589 patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the '589 patent at least as of October 25, 2016 when Polaris placed Xilinx on notice of infringement of the '589 patent and identified Xilinx's infringing products. At the very least, because Xilinx was on notice of the '589 patent and the accused infringement, it was willfully blind regarding the infringement it induced.

28. On information and belief, Xilinx contributed to infringement of one or more claims of the '589 patent, including, but not limited to, Claims 11, 12, and 13, pursuant to 35 U.S.C. § 271(c) by, without authority, selling and/or offering to sell within the United States, importing, and/or supplying components of systems that perform the claimed methods for initializing a dynamic semiconductor memory device, including without limitation the 589 Patent Infringing Products. These components supplied by Xilinx are key components in automotive, defense, aerospace, and networking applications. When, for example, these products are installed in an embedded system and used, the claimed dynamic semiconductor memory device is used, and/or the claimed methods performed, thereby infringing, literally or under the doctrine of equivalents, one or more claims of the '589 patent. Xilinx supplied these components, including without limitation the '589 patent Infringing Products, with the knowledge of the '589 patent and with the knowledge that these components constitute material parts of the claimed inventions of

the ’589 patent. Xilinx knows that these components are especially made and/or especially adapted for use as claimed in the ’589 patent. Further, Xilinx knows that there is no substantial non-infringing use of these components.

29. Polaris has suffered damages as a result of Xilinx’s infringement of the ’589 patent.

30. Up until the expiration of the ’589 patent, Xilinx’s infringement of the ’589 patent was willful, deliberate, and in disregard of Polaris’s patent rights. At least as of October 25, 2016, when Polaris placed Xilinx on notice of infringement of the ’589 patent and identified Xilinx’s infringing products, Xilinx had actual knowledge of infringement of the ’589 patent and proceeded to infringe the ’589 patent with full and complete knowledge of that patent and its applicability to Xilinx’s products without taking a license under the ’589 patent. Despite knowledge of the ’589 patent, Xilinx acted despite an objectively high likelihood that its actions constituted patent infringement. This objective risk was known to Xilinx, and should have been known to Xilinx. Such willful and deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT II

(Infringement of U.S. Patent 7,145,369)

31. Polaris incorporates and realleges paragraphs 1-30 above as though fully set forth herein.

32. On information and belief, Xilinx has willfully infringed and continues to willfully infringe one or more claims of the ’369 patent, including, but not limited to, claim 2, literally, or under the doctrine of equivalents, by making, selling, using, offering for sale, and/or importing into the United States without authority, products containing a Dynamic Memory Interface compatible with DDR3, DDR3L memory, including but not limited to Zynq Ultrascale+ MPSoC, Zynq-7000 SoC, the UltraScale product family, and the 7-series product

family, and the Virtex-6 and Virtex-5 product families (collectively, "'369 Patent Infringing Products"). Each '369 Patent Infringing Product meets each and every limitation of at least claim 2 of the '369 patent.

33. On information and belief, each '369 Patent Infringing Product is an integrated circuit that contains an output driver for driving an integrated circuit. The output driver of each '369 Patent Infringing Product includes a driver circuit, for example, VRN, VRP, that drive an input signal of the output driver onto an output line, for example, the outputs from VRN and VRP.

34. On information and belief, each '369 Patent Infringing Product contains a measuring circuit, for example, VRN, VRP, for measuring at least one of an output line current and an output line potential, for example, the potential of the outputs from VRN and VRP.

35. On information and belief, each '369 Patent Infringing Product contains a control unit, for example, the DCI state machine, providing a control signal, for example, through the DCI state machine's control of the drive strength of the '369 Patent Infringing Products' DDR IOB, for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification- prescribed potential range and a specification-prescribed current range, for example, the power range and potential range as described in page 309 of the Xilinx Zynq-7000 All Programmable SoC Technical Reference Manual. The control unit includes a feedback control to affect the driver strength based on a measured value provided by the measuring circuit, for example, by adjusting VRN relative to VREF based on the measuring value provided by the measuring circuit.

36. On information and belief, the desired power range of the output driver of the '369 Patent Infringing Products is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value, for example, VREF, and a specification prescribed lower potential limit value adjusted with the tolerance magnitude, for example, VRN adjusted relative to VREF.

37. On information and belief, Xilinx has induced and continues to induce infringement of one or more claims of the ’369 patent, including, but not limited to, claim 2 pursuant to 35 U.S.C. § 271(b), by encouraging its customers and other third parties to install 369 Patent Infringing Products on their products in accordance with Xilinx’s specifications and instructions. This infringes, literally or under the doctrine of equivalents, of one or more claims of the ’369 patent by such customers or third parties. Xilinx’s acts of inducement include: providing its customers with the ’369 Patent Infringing Products and intending its customers to use the ’369 Patent Infringing Products with hardware, software, and other infrastructure that enable and/or make use of these products; advertising these products through its own and third-party websites; and providing instructions on how to use these products.

38. Xilinx proceeded in this manner despite its actual knowledge of the ’369 patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the ’369 patent at least as of October 25, 2016 when Polaris placed Xilinx on notice of infringement of the ’369 patent and identified Xilinx’s infringing products. At the very least, because Xilinx has been and remains on notice of the ’369 patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

39. On information and belief, Xilinx has contributed to and continues to contribute to infringement of one or more claims of the ’369 patent, including, but not limited to, claim 1, pursuant to 35 U.S.C. § 271(c) by, without authority, selling and/or offering to sell within the United States, importing, and/or supplying components of the claimed output driver for an integrated circuit, including without limitation the ’369 Patent Infringing Products. These components supplied by Xilinx are key components in automotive, defense, aerospace, and networking applications. When, for example, these products are installed in an embedded system with terminating resistors in accordance with Xilinx’s specification, the resulting system infringes, literally or under the doctrine of equivalents, one or more claims of the ’369 patent. Xilinx supplied and continues to supply these components, including without limitation the ’369

Patent Infringing Products, with the knowledge of the ’369 patent and with the knowledge that these components constitute material parts of the claimed inventions of the ’369 patent. Xilinx knows that these components are especially made and/or especially adapted for use as claimed in the ’369 patent. Further, Xilinx knows that there is no substantial non-infringing use of these components.

40. Polaris has suffered damages as a result of Xilinx’s infringement of the ’369 patent.

41. Xilinx’s infringement of the ’369 patent has been and continues to be willful, deliberate, and in disregard of Polaris’s patent rights. At least as of October 25, 2016, when Polaris placed Xilinx on notice of infringement of the ’369 patent and identified Xilinx’s infringing products, Xilinx has had actual knowledge of infringement of the ’369 patent and has proceeded to infringe the ’369 patent with full and complete knowledge of that patent and its applicability to Xilinx’s products without taking a license under the ’369 patent. Despite knowledge of the ’369 patent, Xilinx has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Xilinx, and is also so obvious that it should have been known to Xilinx. Such willful and deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT III

(Infringement of U.S. Patent 7,532,523)

42. Polaris incorporates and realleges paragraphs 1-41 above as though fully set forth herein.

43. On information and belief, Xilinx has willfully infringed and continues to willfully infringe one or more claims of the ’523 patent, including, but not limited to, claims 5 and 6, literally, or under the doctrine of equivalents, by making, selling, using, offering for sale, and/or importing into the United States without authority, products containing a Dynamic Memory Interface compatible with DDR3, DDR3L memory, including but not limited to Zynq

Ultrascale+ MPSoC, Zynq-7000 SoC, the UltraScale product family, and the 7-series product family, and the Virtex-6 and Spartan-6 product families (collectively, "523 Patent Infringing Products"). Each 523 Patent Infringing Product, when installed on a board with DDR3 SDRAM ("523 Patent Infringing System"), meets each and every limitation of at least claims 5 and 6 of the '523 patent.

44. On information and belief, each '523 Patent Infringing System contains a memory controller having a terminal, for example, the memory controllers of the 523 Patent Infringing Products.

45. On information and belief, each '523 Patent Infringing System contains a plurality of memory chips, for example, its DDR3 SDRAM.

46. On information and belief, each '523 Patent Infringing System contains a termination circuit, for example the RTT pullups and pulldowns of the on-die termination circuits, connectable with the terminal and configured to terminate the terminal according to a settable resistance value, for example, RZQ/4, RZQ/2, or RZQ/6.

47. On information and belief, each '523 Patent Infringing System contains a control command port for receiving a control command signal for affecting accessibility of the memory chip, for example, the RAS#, CAS#, and WE# command inputs and Mode Register MR1 values.

48. On information and belief, each 523 Patent Infringing System contains a control circuit connected to the termination circuit, for example the "other circuitry like RCV, …" in Fig. 101 of the JEDEC DDR3 SDRAM standard, July 2012, and configured to set the resistance value as a function of the received control command signal, for example by setting the resistance value to "Rtt_Nom disabled, RZQ/4, RZQ/2, RZQ/6 in Mode Register 1.

49. On information and belief, each '523 Patent Infringing System contains a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller, for example, the memory bus between the '523 Patent Infringing Product and the DDR3 SDRAM as depicted in Figure 1-51 of the Xilinx "Zynq-7000 AP SoC and 7 Series Device Memory Interface Solutions v.3.0 User Guide" on page 89.

50. On information and belief, each 523 Patent Infringing System contains a termination port to receive a termination signal, for example ddr_odt, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value, e.g., RTT_NOM, in response to the termination signal.

51. On information and belief, the control circuit, as a function of the termination signal ODT, (1) selectively terminates the terminal with the set resistance value RTT_NOM after a first time delay, for example, ODTLon = CWL + AL - 2, or (2) does not terminate the terminal in accordance with a second time delay, for example, ODTLoff = CWL + AL -2. On information and belief, the first time delay is sufficient to set the resistance value, for example, as indicated by the assertion of RTT_NOM after the first time delay ODTLon.

52. On information and belief, the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time. For example, as seen in the timing diagram below, the resistance value is set to a first resistance value (RTT_WR) after a first predetermined switchover time (ODTLon), and is set to a second resistance value (RTT_NOM) after a second predetermined switchover time (e.g., ODTLcwn4, ODTLcwn8).

53. On information and belief, Xilinx has induced and continues to induce infringement of one or more claims of the ’523 patent, including, but not limited to, claims 5 and 6 pursuant to 35 U.S.C. § 271(b), by encouraging its customers and other third parties to install ’523 Patent Infringing Products on their products, or to make, use, sell, offer for sale, or import ’523 Patent Infringing Systems using ’523 Patent Infringing Products in accordance with Xilinx’s specifications and instructions. This infringes, literally or under the doctrine of equivalents, of one or more claims of the ’523 patent by such customers or third parties. Xilinx’s acts of inducement include: providing its customers with the ’523 Patent Infringing Products and intending its customers to use the ’523 Patent Infringing Products with hardware, software, and other infrastructure that enable and/or make use of these products; advertising these products

through its own and third-party websites; and providing instructions on how to use these products.

54. Xilinx proceeded in this manner despite its actual knowledge of the ’523 patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the ’523 patent at least as of December 7, 2016 when Polaris placed Xilinx on notice of infringement of the ’523 patent and identified Xilinx’s infringing products. At the very least, because Xilinx has been and remains on notice of the ’523 patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

55. On information and belief, Xilinx has contributed to and continues to contribute to infringement of one or more claims of the ’523 patent, including, but not limited to, claims 5 and 6, pursuant to 35 U.S.C. § 271(c) by, without authority, selling and/or offering to sell within the United States, importing, and/or supplying components of 523 Patent Infringing Systems, including without limitation the ’523 Patent Infringing Products. These components supplied by Xilinx are key components in automotive, defense, aerospace, and networking applications. For example, as detailed above, the ’523 Patent Infringing Systems infringe, literally or under the doctrine of equivalents, one or more claims of the ’523 patent. Xilinx supplied and continues to supply these components, including without limitation the ’523 Patent Infringing Products, with the knowledge of the ’523 patent and with the knowledge that the 523 Patent Infringing Products constitute material parts of the claimed inventions of the ’523 patent. Xilinx knows that these components are especially made and/or especially adapted for use as claimed in the ’523 patent. Further, Xilinx knows that there is no substantial non-infringing use of these components.

56. Polaris has suffered damages as a result of Xilinx’s infringement of the ’523 patent.

57. Xilinx’s infringement of the ’523 patent has been and continues to be willful, deliberate, and in disregard of Polaris’s patent rights. At least as of December 7, 2016, when Polaris placed Xilinx on notice of infringement of the ’523 patent and identified Xilinx’s

infringing products, Xilinx has had actual knowledge of infringement of the '523 patent and has proceeded to infringe the '523 patent with full and complete knowledge of that patent and its applicability to Xilinx's products without taking a license under the '523 patent. Despite knowledge of the '523 patent, Xilinx has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Xilinx, and is also so obvious that it should have been known to Xilinx. Such willful and deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT IV

(Infringement of U.S. Patent No. 6,701,473)

58. Polaris incorporates and realleges paragraphs 1-57 as though fully set forth herein.

59. On information and belief, Xilinx has willfully infringed and continues to willfully infringe one or more claims of the '473 patent, including, but not limited to, claims 11, 12, and 13 of the '473 patent literally, or under the doctrine of equivalents, by using in the United States without authority, products containing a Dynamic Memory Interface compatible with DDR3, DDR3L, and DDR4 memory, including but not limited to Zynq Ultrascale+ MPSoC, Zynq-7000 SoC, the UltraScale product family, and the 7-series product family (collectively, "473 Patent Infringing Products"). The 473 Patent Infringing Products, when coupled with DDR3 SDRAM ("473 Patent Infringing Systems") perform the claimed methods for testing a circuit component which is connected to other circuit components via a bus.

60. On information and belief, when Xilinx, its customers, and other third parties turn on the 473 Patent Infringing Systems, provide a plurality of circuit components that are connected to a bus, for example, the 473 Patent Infringing Products connected to the DDR3 SDRAM via the memory bus of the physical interface.

61. On information and belief, the '473 Patent Infringing Systems configure at least one of the plurality of circuit components, for example, one of the DDR3 SDRAM, such that it can be tested independently, for example, using the write leveling feature of DDR3 SDRAM,

from all others of said plurality of circuit components, for example, the other DDR3 SDRAM of the ’473 Patent Infringing System, the at least one of the plurality of circuit components defining a circuit component to be tested, for example, the DDR3 SDRAM that is to be undergoing the write leveling procedure.

62. On information and belief, while the ’473 Patent Infringing Systems, while testing their DDR3 SDRAM, perform an operation, namely, write leveling, with the circuit component to be tested, the operation selected the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation, for example, outputting data through the DQ feedback line as depicted in Fig. 1-63 of the Xilinx Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solution v3.0 User Guide.

63. On information and belief, the ’473 Patent Infringing Systems signal a bus control device which controls the bus that the circuit component to be tested is undergoing a test, for example, the write_calib_n signal indicating the start of the write leveling mode.

64. On information and belief, the ’473 Patent Infringing Systems use the bus control device to ensure that, during testing of the circuit component to be tested, the bus is terminated, for example, after ODT is asserted, by a device selected from the group consisting of the bus control device and one of the others of the plurality of circuit components, for example, the other DDR3 SDRAMs of the ’473 Patent Infringing Systems.

65. On information and belief, the 473 Patent Infringing Systems, during write leveling mode, output data to the bus that is other than the data which would be output to the bus during normal operation, and outputs infrequently changing data, for example, outputting infrequently changing data on the DQ Feedback line as depicted in Fig. 1-63 of the Xilinx Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solution v3.0 User Guide.

66. On information and belief, Xilinx has induced and continues to induce infringement of one or more claims of the ’473 patent, including, but not limited to, claims 20, 26, 27, and 28 to 35 U.S.C. § 271(b), by encouraging its customers and other third parties to

perform the claimed method for testing a circuit component which is connected to other circuit components via a bus. This infringes, literally or under the doctrine of equivalents, of one or more claims of the ’473 patent by such customers or third parties. Xilinx’s acts of inducement include: providing its customers with the ’473 Patent Infringing Products and intending its customers to use the ’473 Patent Infringing Products with hardware, software, and other infrastructure that enable and/or make use of these products, such as the ’473 Patent Infringing Systems; advertising these products through its own and third-party websites; and providing instructions on how to use these products.

67. Xilinx proceeded in this manner despite its actual knowledge of the ’473 patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the ’473 patent at least as of December 7, 2016 when Polaris placed Xilinx on notice of infringement of the ’473 patent and identified Xilinx’s infringing products. At the very least, because Xilinx has been and remains on notice of the ’473 patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

68. On information and belief, Xilinx has contributed to and continues to contribute to infringement of one or more claims of the ’473 patent, including, but not limited to, claims 5 and 6, pursuant to 35 U.S.C. § 271(c) by, without authority, selling and/or offering to sell within the United States, importing, and/or supplying components, such as the ’473 Patent Infringing Products, of systems, such as the ’473 Patent Infringing Systems, that perform the claimed methods for testing a circuit component which is connected to other circuit components via bus. These components supplied by Xilinx are key components in automotive, defense, aerospace, and networking applications. For example, as detailed above, the ’473 Patent Infringing Systems perform the claimed methods and infringe, literally or under the doctrine of equivalents, one or more claims of the ’473 patent. Xilinx supplied and continues to supply these components, including without limitation the ’473 Patent Infringing Products, with the knowledge of the ’473 patent and with the knowledge that the ’473 Patent Infringing Products constitute material parts

of the claimed inventions of the ’473 patent. Xilinx knows that these components are especially made and/or especially adapted for use as claimed in the ’473 patent. Further, Xilinx knows that there is no substantial non-infringing use of these components.

69. Polaris has suffered damages as a result of Xilinx’s infringement of the ’473 patent.

70. Xilinx’s infringement of the ’473 patent has been and continues to be willful, deliberate, and in disregard of Polaris’s patent rights. At least as of December 7, 2016, when Polaris placed Xilinx on notice of infringement of the ’473 patent and identified Xilinx’s infringing products, Xilinx has had actual knowledge of infringement of the ’473 patent and has proceeded to infringe the ’473 patent with full and complete knowledge of that patent and its applicability to Xilinx’s products without taking a license under the ’473 patent. Despite knowledge of the ’473 patent, Xilinx has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Xilinx, and is also so obvious that it should have been known to Xilinx. Such willful and deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

PRAYER FOR RELIEF

Polaris respectfully prays for relief as follows:

a. A judgment that Xilinx has infringed and continues to infringe one or more claims of the Asserted Patents;

b. A judgment that Xilinx has willfully infringed one or more claims of the Asserted Patents;

c. A judgment awarding Polaris all damages adequate to compensate for Xilinx’s infringement, and in no event less than a reasonable royalty for its acts of infringement, including all pre-judgment and post-judgment interest at the

maximum rate allowed by law;

d. A judgment awarding Polaris treble damages pursuant to 35 U.S.C. § 284 as a result of Xilinx's willful conduct;

e. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding Polaris its reasonable attorneys fees and costs;

f. That an accounting be performed to determine the damages to be awarded to Polaris as a result of Xilinx's infringing activities, including an accounting for infringing conduct not presented at trial and an award of additional damages for any such infringing sales; and

g. A judgment awarding Polaris such other relief as the Court may deem just and equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Polaris demands a trial by jury on all issues so triable.

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