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IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF OREGON

PORTLAND DIVISION

BELL SEMICONDUCTOR, LLC Plaintiff, v. LATTICE SEMICONDUCTOR, INC. Defendant.	Case No. 3:22-cv-01282 **COMPLAINT FOR PATENT INFRINGEMENT** JURY TRIAL DEMANDED

ORIGINAL COMPLAINT

Plaintiff Bell Semiconductor, LLC ("Bell Semic" or "Plaintiff") brings this Complaint against Defendant Lattice Semiconductor, Inc. ("Lattice") for infringement of U.S. Patent Nos. 7,149,989 ("the '989 patent") and 7,260,803 ("the '803 patent") (collectively the "Lakshmanan patents"). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1. This is a patent infringement suit relating to Lattice's unauthorized and unlicensed use of the Lakshmanan patents. The metal design and insertion technologies claimed in the Lakshmanan patents are used by Lattice in the production of one or more of its devices, including its LCMX02-7000HC.

2. Semiconductor devices include different kinds of materials to function as intended. For example, these devices typically include both metal (i.e., conductor) and insulator materials, which are deposited or otherwise processed sequentially in layers to form the final device. These layers—and the interconnects and components formed within them—have gotten much smaller over time, increasing the performance of these devices dramatically. These devices have also become exceedingly more complex with increasing numbers of layers and increasingly smaller device features, all to enable increasingly faster devices operating at higher clock speeds. As a result, it has become more important to reduce the chance of short circuits and to keep the layers planar as the device is being built because defects and warpage can cause fabrication issues and malfunctioning of the device. Manufacturers use a process called Chemical Mechanical Planarization/Polishing ("CMP") to smooth out the surface of the device periodically between

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deposition and/or etching of each layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be "polished" away at different rates, leading to erosion or dishing on the surface. To reduce this problem "dummy" interconnect material, also known as "dummy fill," is typically inserted into low-density regions of the device to increase the overall uniformity of the structures on the surface of the layer and reduce the density variability across the surface of the device. Dummy fill is typically inserted by a dummy fill tool, which checks the metal density of the device and places dummy metal into regions that do not meet the metal density needed to minimize the likelihood that CMP processes causes the device to malfunction.

3. Prior to development of the methodology described in the '803 patent, if a designer requested even a small change to a semiconductor device, the dummy fill pattern must be thrown out. This is problematic because it can take up to 30 hours to run the dummy fill tool to create the dummy fill pattern. By starting over, the entire device design layout could be delayed by 30 hours or more. This issue is exacerbated with every subsequent change that again causes the dummy fill process to begin again from scratch. Such an iterative, time-consuming process negatively impacts the fabrication schedule and causes costs to go up.

4. Viswanathan Lakshmanan, Richard Blinne, Vikram Shrowty, and Lena Montecillio ("the '803 Inventors"), the inventors of the '803 patent, understood the drawbacks of this process and set out to develop a more efficient method for inserting dummy metal into a circuit design after portion(s) of it have changed. The '803 Inventors ultimately conceived of a dummy fill insertion procedure that did not require having to rerun the dummy fill tool whenever any change

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was made to the layout. The claimed invention, after a portion of the design data has changed, first performs a check to determining whether any dummy metal objects intersect with any other objects in the design data. Then any intersecting dummy metal objects are deleted from the design data, thereby avoiding having to rerun the dummy fill tool.

5. The inventions disclosed in the ’803 patent provide many advantages over the prior art. In particular, they provide a simple and efficient method for ensuring dummy metal does not intersect other components such that the dummy fill tool does not have to be rerun. *See* Ex. A at 2:6–22. As mentioned above, this is very beneficial as it substantially reduces the run time of the dummy fill tool, shortens the overall design timeline, and avoids cost overruns and delays, making it less costly to make changes later in the design process. *See* Ex. A at 1:51–65. Given the aforementioned increased complexity of circuit designs and the corresponding delays from ECOs and layout changes, these efficiency gains have become more and more important in completing the design process without affecting time-to-market. These significant advantages are achieved through the use of the patented inventions and thus the ’803 patent presents significant commercial value for companies like Lattice.

6. The ’989 patent addresses another way to minimize short circuits and malfunctioning devices. When creating a semiconductor device, designers typically create layout designs that contain the topological information used to identify structures within several layers of the semiconductor device. These layout designs are ultimately used as blueprints to create the physical semiconductor device. Prior to development of the methodology described in the ’989 patent, the designs would be validated at the very end of the design cycle, when all components have been placed and routed. However, if the validation process detects a design fault, like a short circuit, at the very end of the design cycle, then the timing of the entire integrated circuit design

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may have to be reset. In some cases, the design may have to be re-floorplanned and the entire design cycle may have to be reiterated, causing delays on of several weeks or months, depending on the overall complexity of the design and the process node. Similarly, it is not possible to simply run the validation check early in the process to avoid this issue. Doing so would cause the validation process to incorrectly identify a large number of errors because the circuit design is incomplete in early stages.

7. Viswanathan Lakshmanan, Alan Holesovsky, Lisa Miller, and Jonathan Kuppinger ("the '989 Inventors"), the inventors of the '989 patent, understood the drawbacks of both late stage and early stage validation processes and decided to create something better. The '989 Inventors ultimately conceived of a validation procedure that specifies validation checks on certain physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground. The claimed invention receives a representation of an integrated circuit design and a physical design rule deck that specifies rule checks to be performed on the integrated circuit design. The claimed invention generates a specific rule deck from the physical design rule deck, where the specific rule deck is a subset that includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design. A physical design validation is performed on the integrated circuit design from the specific rule deck to identify texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design.

8. The inventions disclosed in the '989 patent provide many advantages over the prior art. In particular, they provide the ability to perform an early validation process that does not falsely identify a number of unfounded errors in the early stage of the design. *See* Ex. B at 2:47–58. For instance, in early stages, the patented process can identify violations in floorplanning, texted metal

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shorts, and errors in power map structure. *See* Ex. B at 2:64–3:7. Early defect detection saves computer processing time, avoids severe voltage droop, and allows for correction in early stages, each of which would otherwise result in costly schedule delays and unacceptable turnaround time. *See* Ex. B at 3:7–20. Moreover, this allows high-level power and signal-routing such that individual blocks with defined pins can be finalized by the responsible members of design team in parallel, at substantial decrease in design time and overall gains in efficiency. These significant advantages are achieved through the use of the patented inventions and thus the '989 patent presents significant commercial value for companies like Lattice.

9. Bell Semic brings this action to put a stop to Lattice's unauthorized and unlicensed use of the inventions claimed in the Lakshmanan patents.

THE PARTIES

10. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

11. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America's greatest technology incubators. Bell Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

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12. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor–related inventions was developed over many years by some of the world's leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation ("LSI"). This portfolio reflects technology that underlies many important innovations in the development of semiconductors and integrated circuits for high–tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

13. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since those early days at Bell Labs. For example, Bell Semic's CTO was an LSI Fellow and Broadcom Fellow. He is known throughout the world as an innovator with more than 300 patents to his name, and he has a sterling reputation for helping semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from the semiconductor world to work with Nortel Networks in the telecom industry during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees and employees. In addition, several Bell Semic executives previously served as engineers at many of these companies and were personally involved in creating the ideas claimed throughout Bell Semic's extensive patent portfolio.

14. On information and belief, Lattice has its principal place of business and corporate headquarters at 5555 NE Moore Court, Hillsboro, OR 97124. On information and belief, Lattice develops, designs, and/or manufactures products in the United States, including in this District, according to the '803 and '989 patented processes/methodologies; and/or uses the '803 and '989

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patented processes/methodologies in the United States, including in this District, to make products; and/or distributes, markets, sells, or offers to sell in the United States and/or imports products into the United States, including in this District, that were manufactured or otherwise produced using the patented process. Additionally, Lattice introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

JURISDICTION AND VENUE

15. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

16. This Court has personal jurisdiction over Lattice under the laws of the State of Oregon, due at least to its substantial business in Oregon and in this District. Lattice has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of Oregon, and in this District by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of Oregon and in this District, Lattice, directly or through intermediaries: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the Lakshmanan patented process/methodology; (iii) distributes, markets, sells, or offers to sell products formed according to the Lakshmanan patented process/methodology; and/or (iv) imports products formed according to the Lakshmanan patented process/methodology.

17. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because Lattice has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, Lattice

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maintains its principal place of business and corporate headquarters at 5555 NE Moore Court, Hillsboro, OR 97124.

18. Currently, Lattice is advertising 18 jobs in the Portland area, including 6 product development and engineering positions. These positions include those that relate to the '803 and '989 patented technology, including Product Engineer, Product Test Engineering Manager, and Senior Reliability Engineer. *See Lattice Semiconductor Careers,* Lattice (https://recruiting2.ultipro.com/LAT1001LATT/JobBoard/e7f50c7c-43f9-46e9-86ed-b31eaa369842/?q=&o=postedDateDesc) (last visited August 10, 2022). Moreover, on information and belief, Lattice employs more than 150 employees, including over 80 engineers in the Portland area. *See* Search Results for Current Lattice Employees, LinkedIn (available at https://www.linkedin.com/search/results/people/?currentCompany=%5B%226994%22%5D&geoUrn=%5B%2290000079%22%5D&keywords=engineer&origin=GLOBAL_SEARCH_HEADER&sid=%2C3*).

19. Venue is also convenient in this District. This is at least true because of this District's close ties to this case—including the technology, relevant witnesses, and sources of proof noted above—and its ability to quickly and efficiently move this case to resolution. Further, Lattice has purposely availed itself of the court system in this District on multiple occasions.

20. On information and belief, Bell Semic's cause of action arises directly from Lattice's circuit design work and other activities in this District. Moreover, on information and belief, Lattice has derived substantial revenues from its infringing acts occurring within the State of Oregon and within this District.

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U.S. PATENT NO. 7,149,989

21. Bell Semic is the owner by assignment of the ’989 patent. The ’989 patent is titled “Method of Early Physical Design Validation and Identification of Texted Metal Short Circuits in an Integrated Circuit Design.” The ’989 patent issued on December 12, 2006. A true and correct copy of the ’989 patent is attached as Exhibit B.

22. The inventors of the ’989 patent are Viswanathan Lakshmanan, Alan Holesovsky, Lisa Miller, and Jonathan Kuppinger.

23. The application that resulted in the issuance of the ’989 patent was filed on September 22, 2004. The ’989 patent claims priority to September 22, 2004.

24. The ’989 patent generally relates to “methods of verifying an integrated circuit design to ensure adherence to process rules and overall manufacturability of the integrated circuit design for a specific technology.” Ex. B at 1:10–15.

25. The ’989 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior validation methodology was disadvantageous because “a design fault detected so late might reset the time schedule for the entire integrated circuit design.” Ex. B at 2:42–44. In some cases, this means the “design may have to be re-floorplanned, and the entire design cycle may have to be reiterated.” Ex. B at 2:44–46. Existing early design validation processes resulted in “substantial amount[s] of computer processing time that would severely impact the product turnaround time.” Ex. B at 2:50–54. In addition, it would “falsely report” a large number of design errors “due to the incomplete circuit design, making it difficult to sort out the design errors that need to be corrected before the circuit design is completed.” Ex. B at 2:54–58.

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26. In light of the drawbacks of the prior art, the Inventors recognized the need to "provide[] design rules that may be used in conjunction with a design rule check tool and/or a layout vs. schematic tool in an early stage of the physical design to detect design rule violations in floorplanning, including input/output cell placement and construction and power distribution and power map structure." Ex. B at 2:64–3:3. Moreover, "texted metal short circuits may be identified most advantageously in the early or evolutionary aspects of the design flow," which reduc[es] the computer processing time required to validate an integrated circuit design," such as once layout design is complete. Ex. B at 3: 3–11. The inventions claimed in the '989 patent address this need.

27. The '989 patent contains two independent claims and 12 total claims, covering a method and computer program product. Claim 1 reads:

> 1. A method comprising the steps of:
>
> (a) receiving as input a representation of an integrated circuit design;
>
> (b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design;
>
> (c) generating a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design; and
>
> (d) performing a physical design validation on the integrated circuit design from the specific rule deck to identify texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design.

28. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, minimizing the potential for design-based short circuits,

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ensuring overall manufacturability of devices, reducing probability of failure, and ultimately lessening the likelihood of defective devices. *See, e.g.*, Ex. B at 1:11–15; 3:3–19.

29. The claims of the ’989 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly validation processes. The claims of the ’989 patent disclose a new and novel solution to specific problems related to end-stage validation. As explained in detail above and in the ’989 patent specification, the claimed inventions improve upon the prior art processes by performing early-stage validation on texted metal short circuits. This has the advantage of ensuring manufacturability of devices, lessening the likelihood of short circuits and other defects, as well as substantially reducing the time needed to finalize a circuit design. This allows high-level power and signal-routing such that individual blocks with defined pins can be finalized by the responsible members of design team in parallel, at substantial decrease in design time and overall gains in efficiency.

U.S. PATENT NO. 7,260,803

30. Bell Semic is the owner by assignment of the ’803 patent. The ’803 patent is titled “Incremental Dummy Metal Insertions.” The ’803 patent issued on August 21, 2007. A true and correct copy of the ’803 patent is attached as Exhibit A.

31. The inventors of the ’803 patent are Viswanathan Lakshmanan, Richard Blinne, Vikram Shrowty, and Lena Montecillo.

32. The application that resulted in the issuance of the ’803 patent was filed on October 10, 2003. The ’803 patent claims priority to October 10, 2003.

33. The ’803 patent generally relates to “a method for performing dummy metal insertion that avoids having to rerun the dummy fill software tool after the integrated circuit design is changed.” Ex. A at 1:6–10.

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34. The ’803 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior dummy fill methodologies were disadvantageous because, when a customer requests a change, “the results of the dummy fill tool are thrown out, and the dummy fill tool is rerun in order to ensure that no dummy metal intersects with any of the design objects.” Ex. A at 1:51–59. Unfortunately, this “may delay completion of the design by another 30 hours” and may “significantly impact the design schedule and result in cost overruns. Ex. A at 1:60–65. This is especially true when multiple changes are requested.

35. In light of the drawbacks of the prior art, the Inventors recognized the need to “insert[] dummy metal into an integrated circuit design after an ECO [Engineering Change Order] without requiring reruns of the dummy fill tool.” Ex. A at 1:66–2:1. This “saves time on overall design execution” and helps manufacturers “meet aggressive design schedules.” Ex. B at 2:15–22; 4:52–57. The inventions claimed in the ’803 patent address this need.

36. The ’803 patent contains two independent claims and 22 total claims, covering a method and computer readable medium for performing dummy metal insertion. Claim 1 reads:

> 1. A method for performing dummy metal insertion in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool, comprising:
>
> (a) after a portion of the design data is changed, performing a check to determine whether any dummy metal objects intersect with any other objects in the design data; and
>
> (b) deleting the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool.

37. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, minimizing the potential for design-based short circuits, increasing the efficiency of the design process, and ensuring that devices meet their minimum

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density requirements, which reduces the probability of short circuits or other defects that render devices inoperable. *See, e.g.*, Ex. A at 1:24–42.

38. The claims of the ’803 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly dummy fill processes. The claims of the ’803 patent disclose a new and novel solution to specific problems related to rerunning dummy fill tools after a change order is received. As explained in detail above and in the ’803 patent specification, the claimed inventions improve upon the prior art processes by deleting dummy metal objects if a change order results in dummy metal objects that intersect with other objects in the design data. This has the advantage of maintaining minimum metal density without having to rerun the dummy fill tool, and results in substantially reducing the time needed to finalize a circuit design due to the ability to make late-stage ECOs and incremental changes in layout without needing to re-run the dummy fill tool for the entire layer.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,149,989

39. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

40. The ’989 patent is valid and enforceable under the United States Patent Laws.

41. Bell Semic owns, by assignment, all right, title, and interest in and to the ’989 patent, including the right to collect for past damages.

42. A copy of the ’989 patent is attached at Exhibit B.

43. On information and belief, Lattice has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’989 patent by using the patented methodology to design one or more devices, including as one example the LCMX02-7000HC, in the United States.

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44. On information and belief, Lattice employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to validate its circuit designs (the "Accused Processes") as recited in the '989 patent claims. As one example, Lattice's Accused Processes perform a method that receives as input a representation of an integrated circuit design as required by claim 1 of the '989 patent. Lattice does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, into which a circuit design for its LCMX02-7000HC is imported.

45. Lattice's Accused Processes also receive as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design. Lattice does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, that receives various in-design verification processes for concurrent physical design and verification of the LCMX02-7000HC's circuit designs.

46. Lattice's Accused Processes also generate a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design. Lattice does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, that includes a "short finder," "short locator," or similar functionality that identifies texted metal short circuits. For example, the Accused Processes allow designers to select texted metal short circuits, which are shown by cell, text, net, layer and position. The nets may include ground, power, and other signal nets. An exemplary infringement analysis showing infringement of one or more claims of the '989 patent is set forth in Exhibit D. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit E and further describes Lattice's infringement of the '989 patent.

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47. Lattice's Accused Processes infringe and continue to infringe one or more claims of the '989 patent during the pendency of the '989 patent.

48. On information and belief, Lattice has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the '989 patent. Lattice has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the '989 patent.

49. Lattice's infringement of the '989 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

50. Bell Semic has been damaged by Lattice's infringement of the '989 patent and will continue to be damaged unless Lattice is enjoined by this Court. Bell Semic has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

51. Bell Semic is entitled to recover from Lattice all damages that Bell Semic has sustained as a result of Lattice's infringement of the '989 patent, including without limitation and/or not less than a reasonable royalty.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 7,260,803

52. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

53. The '803 patent is valid and enforceable under the United States Patent Laws.

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54. Bell Semic owns, by assignment, all right, title, and interest in and to the ’803 patent, including the right to collect for past damages.

55. A copy of the ’803 patent is attached at Exhibit A.

56. On information and belief, Lattice has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’803 patent by using the patented methodology to design one or more devices, including as one example the LCMX02-7000HC, in the United States.

57. On information and belief, Lattice employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to delete intersecting dummy metal objects from its circuit designs (the “Accused Processes”) as recited in the ’803 patent claims. As one example, Lattice’s Accused Processes perform a method of dummy metal insertion in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool as required by claim 1 of the ’803 patent. Lattice does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, that performs this dummy metal process for its LCMX02-7000HC layout. The LCMX02-7000HC includes dummy metal objects inserted by a dummy fill tool, such as an “integrated” or “in-design” flow.

58. After a portion of the design data is changed, Lattice’s Accused Processes perform a check to determine whether any dummy metal objects intersect with any other objects in the design data. When Lattice receives an Engineering Change Order (“ECO”), it employs a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to perform a Design Rule Check (“DRC”) to determine whether there are any rule violations, including those related to metal fill geometries and layout changes, in the LCMX02-7000HC’s design data.

59. Lattice’s Accused Processes also delete the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool. Lattice does so by employing

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a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, that repairs DRC violations associated with shorts caused by dummy fill geometries intersecting with other objects in the design data. For example, the Accused Processes allow designers to trim metal fill geometries that cause the short or DRC violation. An exemplary infringement analysis showing infringement of one or more claims of the '803 patent is set forth in Exhibit C. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit E and further describes Lattice's infringement of the '803 patent.

60. Lattice's Accused Processes infringe and continue to infringe one or more claims of the '803 patent during the pendency of the '803 patent.

61. On information and belief, Lattice has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the '803 patent. Lattice has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the '803 patent.

62. Lattice's infringement of the '803 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

63. Bell Semic has been damaged by Lattice's infringement of the '803 patent and will continue to be damaged unless Lattice is enjoined by this Court. Bell Semic has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

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64. Bell Semic is entitled to recover from Lattice all damages that Bell Semic has sustained as a result of Lattice's infringement of the '803 patent, including without limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

(a) a judgment declaring that Lattice has infringed one or more claims of the Lakshmanan patents in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;

(b) an award of damages adequate to compensate Bell Semic for infringement of the Lakshmanan patents by Lattice, in an amount to be proven at trial, including supplemental post-verdict damages until such time as Lattice ceases its infringing conduct;

(c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting Lattice and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with Lattice, from committing further acts of infringement;

(d) a judgment requiring Lattice to make an accounting of damages resulting from Lattice's infringement of the Lakshmanan patents;

(e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;

(f) pre-judgment and post-judgment interest at the maximum amount permitted by law;

(g) all other relief, in law or equity, to which Bell Semic is entitled.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

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Dated: August 26, 2022

Respectfully submitted,

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EXHIBIT A

US007260803B2

(12) **United States Patent**
Lakshmanan et al.

(10) **Patent No.: US 7,260,803 B2**
(45) **Date of Patent: Aug. 21, 2007**

(54) **INCREMENTAL DUMMY METAL INSERTIONS**

(75) Inventors: **Viswanathan Lakshmanan**, Thorton, CO (US); **Richard Blinne**, Fort Collins, CO (US); **Vikram Shrowty**, Fremont, CA (US); **Lena Montecillo**, Los Gatos, CA (US)

(73) Assignee: **LSI Corporation**, Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 739 days.

(21) Appl. No.: **10/683,369**

(22) Filed: **Oct. 10, 2003**

(65) **Prior Publication Data**

US 2005/0080607 A1 Apr. 14, 2005

(51) **Int. Cl.**
G06F 17/50 (2006.01)
G06F 19/00 (2006.01)

(52) **U.S. Cl.** **716/10**; 716/21; 716/5; 700/97; 700/103; 700/105; 700/120; 700/121

(58) **Field of Classification Search** 716/10, 716/21, 5; 700/97, 98, 103, 105, 120, 121
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,597,668 A * 1/1997 Nowak et al. 430/5
5,970,238 A * 10/1999 Shibata et al. 716/8
6,516,457 B1 * 2/2003 Kondou 716/8
6,574,789 B1 * 6/2003 Yamauchi 716/21
6,718,527 B2 * 4/2004 Li 716/5
6,751,785 B1 6/2004 Oh
6,815,811 B2 11/2004 Ozawa et al.
6,892,363 B2 * 5/2005 Li 716/2
7,007,259 B2 * 2/2006 Shrowty et al. 716/10
7,137,092 B2 * 11/2006 Maeda 716/8
2001/0011362 A1 * 8/2001 Yoshinaga 716/8
2002/0066067 A1 * 5/2002 Wang et al. 716/11
2002/0138817 A1 * 9/2002 Lee et al. 716/12
2002/0185664 A1 * 12/2002 Dixit et al. 257/211
2003/0204832 A1 * 10/2003 Matumoto 716/19
2004/0025125 A1 * 2/2004 Li 716/5
2004/0031004 A1 * 2/2004 Yoshioka 716/7
2004/0063038 A1 * 4/2004 Shin et al. 430/311
2004/0139408 A1 * 7/2004 Boluki et al. 716/5
2005/0028121 A1 * 2/2005 Shrowty et al. 716/10
2005/0051809 A1 * 3/2005 Smith et al. 257/232
2005/0132306 A1 * 6/2005 Smith et al. 716/1
2006/0190920 A1 * 8/2006 Sakurai et al. 716/21

* cited by examiner

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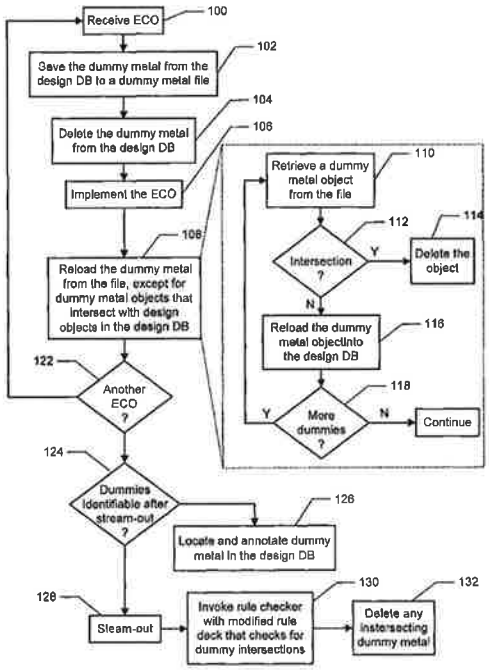
(74) *Attorney, Agent, or Firm*—Strategic Patent Group Inc.

(57) **ABSTRACT**

A method and system for performing dummy metal insertion in design data for an integrated circuit is disclosed, wherein the design data includes dummy metal objects inserted by a dummy fill tool. After a portion of the design data is changed, a check is performed to determine whether any dummy metal objects intersect with any other objects in the design data. If so, the intersecting dummy metal objects are deleted from the design data, thereby avoiding having to rerun the dummy fill tool.

22 Claims, 2 Drawing Sheets



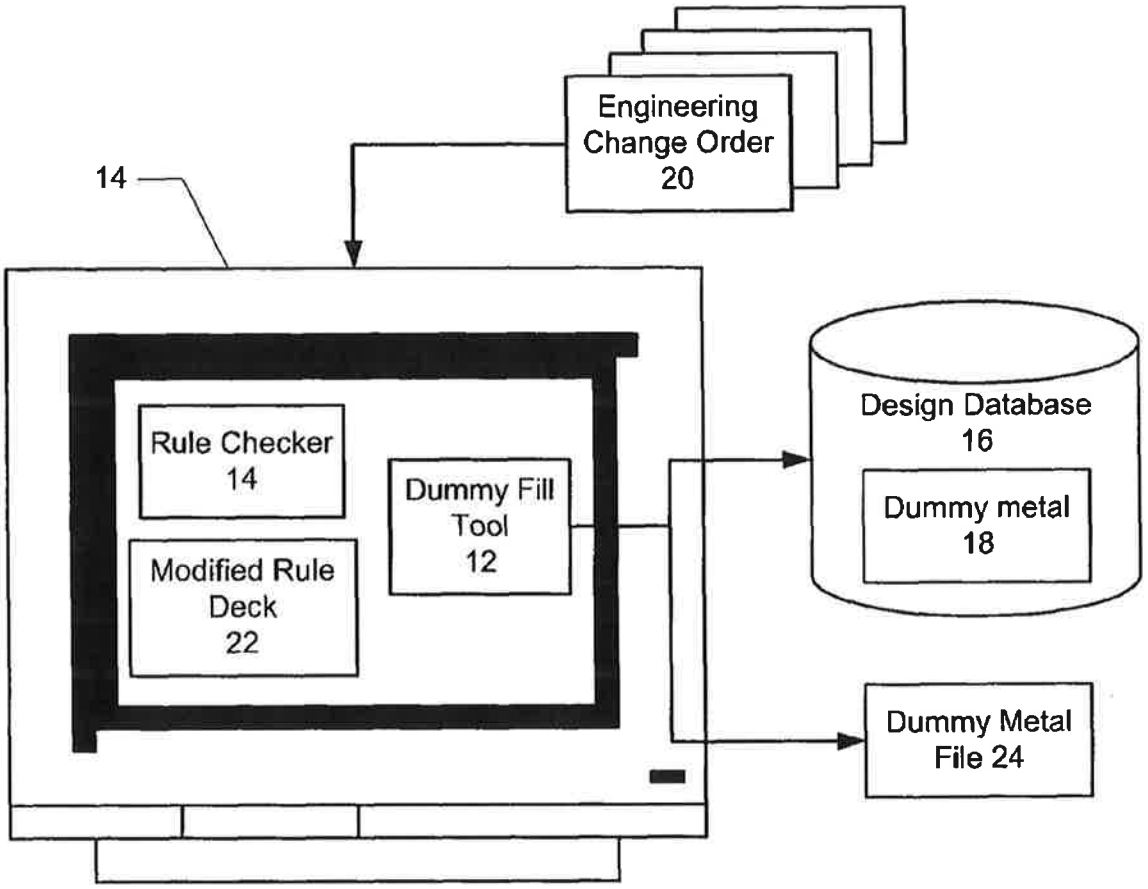

Engineering
Change Order
20
14
Rule Checker
14
Dummy Fill
Tool
12
Modified Rule
Deck
22
Design Database
16
Dummy metal
18
Dummy Metal
File 24

FIG. 1

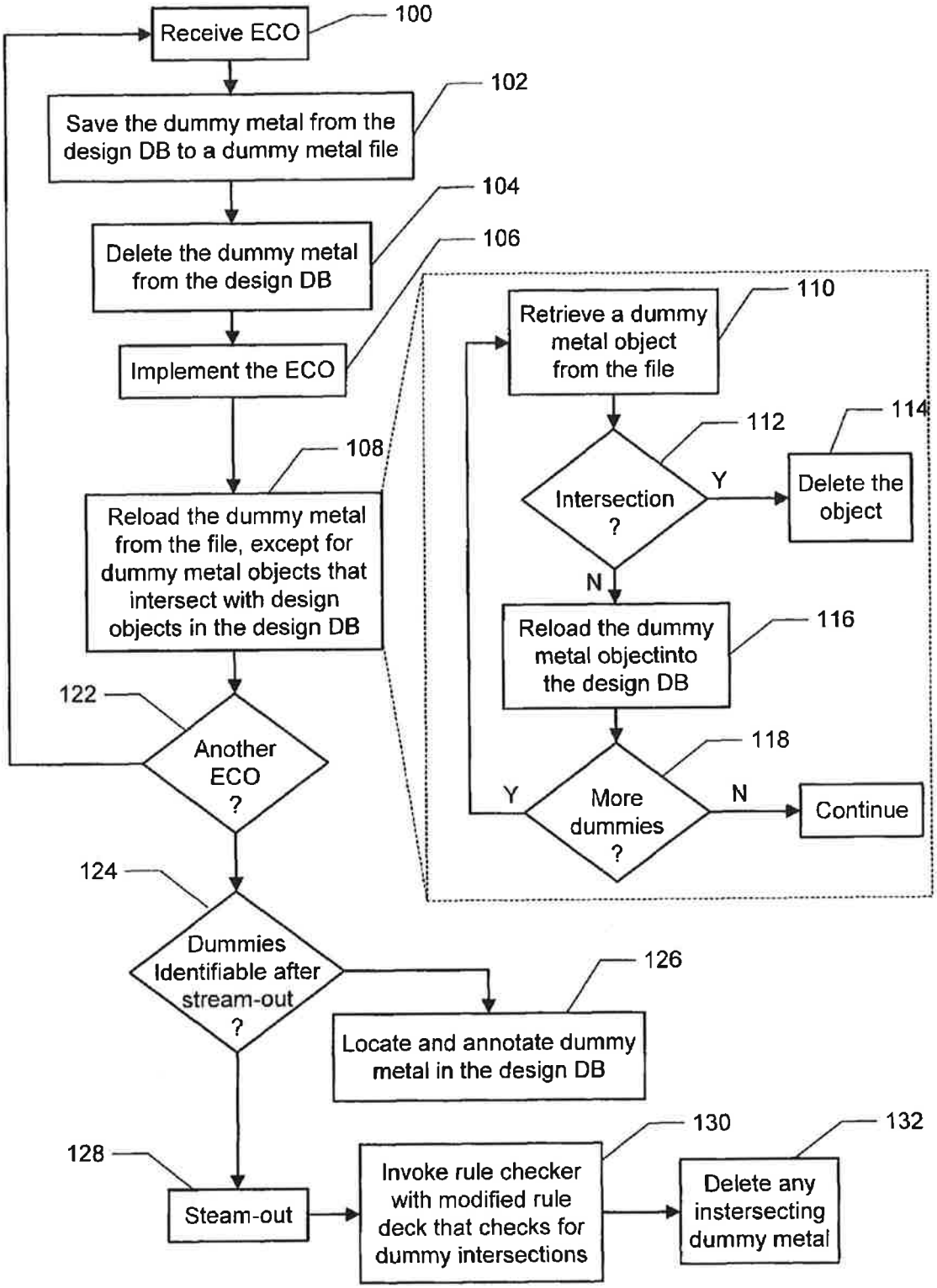

Receive ECO
100
Save the dummy metal from the design DB to a dummy metal file
102
Delete the dummy metal from the design DB
104
Implement the ECO
106
Reload the dummy metal from the file, except for dummy metal objects that intersect with design objects in the design DB
108
Retrieve a dummy metal object from the file
110
Intersection ?
112
Y
Delete the object
114
N
Reload the dummy metal objectinto the design DB
116
More dummies ?
118
Y
N
Continue
Another ECO ?
122
Dummies Identifiable after stream-out ?
124
Locate and annotate dummy metal in the design DB
126
Steam-out
128
Invoke rule checker with modified rule deck that checks for dummy intersections
130
Delete any instersecting dummy metal
132

FIG. 2

INCREMENTAL DUMMY METAL INSERTIONS

FIELD OF THE INVENTION

The present invention relates to a method inserting incremental dummy metal into an integrated circuit design, and more particularly to a method for performing dummy metal insertion that avoids having to rerun the dummy fill software tool after the integrated circuit design is changed.

BACKGROUND OF THE INVENTION

Chemical Mechanical Polishing (CMP) is a part of the chip fabrication process that requires a uniform distribution of metal and silicon over the surface of the chip. To achieve this distribution, pieces of interconnect (metal or silicon) must be inserted into available spaces in low-density regions of the chip. This interconnect insertion is called dummy metal filling or simply dummy filling, and the inserted interconnect is called dummy metal. Dummy metal is typically not allowed to touch or otherwise intersect with any objects in the design.

Most fabrication processes require a minimum density for the interconnects on each layer of a multi-layer chip design. The interconnect density for a region is the sum total of the area of all interconnects in that region divided by the area of the region. Fabrication processes typically partition each layer of the design into rectangular regions, called tiles, and specify that the interconnect density of each tile meet a minimum density requirement.

The process of determining the number and placement of dummy metal is typically preformed by a dummy fill software tool after routing and timing closure during chip design flow. The dummy fill tool operates on a design database that stores the design data for the integrated circuit, and determines whether each tile has an interconnect density equal to or greater than the specified minimum density. If the interconnect density does not meet the minimum density, then the dummy fill tool inserts pieces of dummy metal in free regions of the tile.

The time it takes the dummy fill tool to complete its task is dependent upon the complexity of the integrated circuit design, and correspondingly, the size of the design database. For a design of average complexity, the runtime for the dummy fill tool would be approximately 3-4 hours. With today's new process technologies and increasingly complex designs, the dummy fill tool may have a runtime of up to 30 hours.

The problem is that once a design has almost reached completion, a customer may request changes to the design in the form of engineering change orders (ECO). Once implemented, an ECO may change the locations of objects in the design. And even though most ECO make small incremental changes and 99.9 percent of the design may be left unchanged, the results of the dummy fill tool are thrown out, and the dummy fill tool is rerun in order to ensure that no dummy metal intersects with any of the design objects. Requiring another run of the dummy fill tool is problematic because it may delay completion of the design by another 30 hours. In addition, if more than one ECO is received, multiple runs will be required: one for each ECO. Such an iterative process can significantly impact the design schedule and result in cost overruns.

Accordingly what is needed is a method for inserting dummy metal into an integrated circuit design after an ECO without requiring reruns of the dummy fill tool. The present invention addresses such a need.

SUMMARY OF THE INVENTION

The present invention provides a method and system for performing dummy metal insertion in design data for an integrated circuit, wherein the design data includes dummy metal objects inserted by a dummy fill tool. After a portion of the design data is changed, a check is performed to determine whether any dummy metal objects intersect with any other objects in the design data. If so, the intersecting dummy metal objects are deleted from the design data, thereby avoiding having to rerun the dummy fill tool.

According to the method and system disclosed herein, dummy metal objects inserted into design data are preserved prior to implementing change orders that alter the design data, and then reloaded after implementation of the change order except for dummy metal found to intersect with design objects. This eliminates the need to rerun a dummy fill tool after each ECO, and therefore saves time on overall design execution.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram illustrating a software and hardware environment in which the present invention may be implemented.

FIG. **2** is a flow diagram illustrating the process for incremental dummy metal insertion performed by the dummy fill application in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to a method for adding dummy metal to an integrated circuit design. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiments and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

The present invention provides a method for performing incremental dummy metal insertion in design data for an integrated circuit design after the design has been changed. FIG. **1** is a block diagram illustrating a software and hardware environment in which the present invention may be implemented. During normal design flow of an integrated circuit, multiple design automation tools executing on one or more computers **14** populate a design database **16** with design data. The design database **16** includes information describing all objects of a fully routed integrated circuit design, such as cells, interconnects, and signal nets. An example of the design database is the Milkyway™ Database by Synopsys of Mountain View, Calif. The design automation tools include a dummy fill application **12** and a rule checker **14**. The dummy fill application **12** is typically invoked after routing and timing closure stages of the design flow to insert dummy metal objects **18** into the design database **16** as described above. The rule checker **14** is typically invoked after stream-out to ensure the finished design complies with design rules. In a preferred embodi-

ment, the rule checker tool **14** is an industry-standard DRC checker, such as Mentor Calibre™ and Synopsys Hercules™, for example.

In today's semiconductor industry, customers contract with chip manufacturers to design and produce highly customized integrated circuit designs. During the design flow of a custom integrated circuit design, it is not uncommon for the manufacturer to receive engineering change orders (ECO) **20** from the customer requesting changes to the design. ECOs **20** can be received all the way up to the stream-out phase, where the design database **16** is converted into a file format suitable for actual fabrication. A conventional design flow using a conventional dummy fill tool would require that the dummy fill tool be rerun after each change order was implemented to recompute the dummy metal **18** required for the design, severely impacting aggressive timing schedules.

The present invention provides an improved dummy fill tool **12** and a modified rule deck **22** that dispense with the need to rerun the dummy fill tool **12** after each ECO **20**. According to the present invention, the dummy fill tool **12** performs a check after the implementation of each ECO to determine whether any dummy metal objects **18** intersect with any other objects in the design data. Any dummy metal objects **18** determined to be intersecting another object are then deleted from the design database **16**, thereby avoiding having to rerun the dummy fill tool **12** after each ECO **20**.

FIG. **2** is a flow diagram illustrating the process for incremental dummy metal insertion performed by the dummy fill application **12** in accordance with a preferred embodiment of the present invention. Referring to both FIGS. **1** and **2**, the process begins in step **100** after a request to change the design data in the design database **16** is received. In a preferred embodiment, the request is in the form of an ECO **20**. Typically, the ECO **20** results in design objects (e.g., wires) being added and/or design object locations being changed. Thus, it is possible that the newly added or rearranged design objects may overlap with, and therefore intersect, previously inserted pieces of dummy metal **18**.

To ensure that the design database **16** does not include any such intersections, in step **102**, an operator instructs the dummy fill tool **12** to save the dummy metal **18** from the design database **16** to a dummy metal file **24**. In step **104**, the dummy fill tool **12** deletes all the dummy metal **18** from the design database **16**. In step **106**, the ECO **20** is implemented and the design database **16** updated.

According to the present invention, after the ECO **20** is implemented in step **108**, the dummy fill tool **12** reloads the dummy metal **18** from the dummy metal file **24**, except for dummy metal objects **18** that intersect with design objects in the design database **16**. The sub-processes performed in step **108** are also shown in FIG. **2**.

The process of reloading good dummy metal **18** into the design database **16** begins in step **110** by retrieving a dummy metal object **18** from the dummy metal file **24**. In step **112**, it is determined whether the dummy metal object **18** intersects with any of the design objects. In a preferred embodiment, each dummy metal object **18** is annotated in the design database **16** with an attribute that identifies it as dummy metal. The dummy metal fill tool intersection detection is accomplished by examining nets of the respective wires, and if a net identified as dummy metal **18** intersects with a net of a different name, then the dummy metal object **18** is deleted from the file **24** in step **114**. Otherwise, in step **116**, the dummy metal object **18** is reloaded into the design database **16**. This checking process is then repeated until there are no more dummy metal objects **18** in the dummy metal file **24**, as determined in step **118**.

In an alternative embodiment, rather than deleting a dummy metal object **18** identified as intersecting from the file **24**, the identified dummy metal **18** may be simply passed over and not reloaded during the reload process. In another alternative embodiment, all dummy metal objects **18** in the file **24** may be examined serially, and those found to be intersecting can be flagged as such in the file **24**. A batch reload can then be performed on the file **24** that reloads only the dummy metal objects **18** that are not flagged as intersecting.

As an optional step, after processing the ECO **20**, the operator may choose to fix all tiles in the design database **16** that fail the minimum density requirement by using the dummy fill tool **12** to add additional dummy metal at legal locations.

In step **122** is determined whether there is any more ECOs **20** to implement. If so, then, the process continues at step **100**. Once all of the ECOs **20** have been implemented, the stream-out process may be performed. However, prior to performing stream-out, in step **124** the dummy fill tool **12** determines whether the metal objects **18** are identifiable as such in the design database **16**. This would occur for example, where the dummy fill tool **12** is operating on a design database **16** that was populated with another dummy fill tool that did not identify dummy metal **18**, or if certain types of annotations in the design database **16** are not preserved after stream-out. If the dummy metal **18** are not identifiable in the design database **16**, then in step **126** the dummy fill tool **12** locates and annotates the dummy metal **18** in the design database **16**. According to the present invention, this ensures that all dummy metal **18** will be identifiable after stream-out.

In step **128**, a conventional stream-out process is performed in which the design database **16** is converted into a format suitable for the fabrication process. After stream-out, the rule checker tool **14** is invoked in step **130** using the modified rule deck **22** of the present invention to determine whether the output of the stream-out includes any dummy metal objects **18** that intersect with design objects. According to the present invention, the modified rule deck **22** uses the dummy metal annotations in the design database **16** to determine the existence of intersections between dummy metal **18** and other objects. If an intersecting dummy metal object **18** is found, then in step **132** the dummy metal object **18** is deleted.

According to the present invention, the dummy fill tool **12** preserves the dummy metal **18** inserted into design data when ECO's **20** are implemented, which eliminates the need to rerun the dummy fill tool **12** after each ECO **20**. The dummy fill tool **12** of the present invention helps integrated circuit manufacturers meet aggressive design schedules even though run-times for inserting dummy metal in large designs can be significant, and therefore saves time on overall design execution.

In an alternative embodiment, the method according to the present invention may be implemented as a script or other type of program that operates on the design database, rather than being implemented in the dummy fill tool **12**.

A method for incremental dummy metal insertion has been disclosed. The present invention has been described in accordance with the embodiments shown, and one of ordinary skill in the art will readily recognize that there could be variations to the embodiments, and any variations would be within the spirit and scope of the present invention. Accord-

ingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

We claim:

1. A method for performing dummy metal insertion in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool, comprising:

(a) after a portion of the design data is changed, performing a check to determine whether any dummy metal objects intersect with any other objects in the design data; and

(b) deleting the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool.

2. The method of claim **1** wherein step (a) further includes: prior to implementing the change, saving the dummy metal objects from the design data to a file.

3. The method of claim **2** wherein step (a) further includes: performing the check by accessing the dummy metal objects in the file.

4. The method of claim **3** further including:

reloading remaining dummy metal objects from the file to the design data.

5. The method of claim **4** wherein step (a) further includes:

performing the check by on the dummy metal objects in the file by,

(i) annotating each dummy metal object with an attribute that identifies it as dummy metal, and

(ii) examining nets of respective wires, and determining if a net identified as dummy metal intersects with a net of a different name.

6. The method of claim **5** wherein step (b) further includes:

(iii) deleting from the file any net identified as dummy metal that intersects with a net of a different name.

7. The method of claim **5** wherein step (b) further includes:

(iii) flagging in the file any net identified as dummy metal that intersects with a net of a different name.

8. The method of claim **5** wherein step (c) further includes: not reloading any flagged dummy metal from the file.

9. The method of claim **4** wherein step (a) further includes: changing the portion of the design data by implementing an engineering change order (ECO).

10. The method of claim **9** further including:

performing a stream-out process;

invoking a rule checker tool using a modified rule check to determine whether an output of the stream-out includes any dummy metal objects that intersect with design objects; and

deleting the dummy metal objects that intersect with design objects.

11. The method of claim **10** wherein the modified rule check uses the dummy metal identifications to determine existence of intersections between dummy metal and the design objects.

12. A computer readable medium containing program instructions for performing dummy metal insertion in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool, the program instructions comprising instructions for:

(a) after a portion of the design data is changed, performing a check to determine whether any dummy metal objects intersect with any other objects in the design data; and

(b) deleting the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool.

13. The computer-readable medium of claim **12** wherein instruction (a) further includes an instruction of: prior to implementing the change, saving the dummy metal objects from the design data to a file.

14. The computer-readable medium of claim **13** wherein instruction (a) further includes an instruction of: performing the check by accessing the dummy metal objects in the file.

15. The computer-readable medium of claim **14** further including an instruction of:

(c) reloading remaining dummy metal objects from the file to the design data.

16. The computer-readable medium of claim **15** wherein instruction (a) further includes an instruction of: performing the check by on the dummy metal objects in the file by,

(i) annotating each dummy metal object with an attribute that identifies it as dummy metal, and

(ii) examining nets of respective wires, and determining if a net identified as dummy metal intersects with a net of a different name.

17. The computer-readable medium of claim **16** wherein instruction (b) further includes an instruction of:

(iii) deleting from the file any net identified as dummy metal that intersects with a net of a different name.

18. The computer-readable medium of claim **16** wherein instruction (b) further includes an instruction of:

(iii) flagging in the file any net identified as dummy metal that intersects with a net of a different name.

19. The computer-readable medium of claim **16** wherein instruction (c) further includes an instruction of: not reloading any flagged dummy metal from the file.

20. The computer-readable medium of claim **15** wherein instruction (a) further includes an instruction of: changing the portion of the design data by implementing an engineering change order (ECO).

21. The computer-readable medium of claim **20** further including instructions of:

(d) performing a stream-out process;

(e) invoking a rule checker tool using a modified rule check to determine whether an output of the stream-out includes any dummy metal objects that intersect with design objects; and

(f) deleting the dummy model objects that intersect with design objects.

22. The computer-readable medium of claim **21** wherein the modified rule check uses the dummy metal identifications to determine existence of intersections between dummy metal and the design objects.

* * * * *

EXHIBIT B

US007149989B2

(12) **United States Patent**
Lakshmanan et al.

(10) **Patent No.: US 7,149,989 B2**
(45) **Date of Patent: Dec. 12, 2006**

(54) **METHOD OF EARLY PHYSICAL DESIGN VALIDATION AND IDENTIFICATION OF TEXTED METAL SHORT CIRCUITS IN AN INTEGRATED CIRCUIT DESIGN**

(75) Inventors: **Viswanathan Lakshmanan**, Thorton, CO (US); **Alan Holesovsky**, Loveland, CO (US); **Lisa M. Miller**, Ft. Collins, CO (US); **Jonathan P. Kuppinger**, Windsor, CO (US)

(73) Assignee: **LSI Logic Corporation**, Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 203 days.

(21) Appl. No.: **10/947,498**

(22) Filed: **Sep. 22, 2004**

(65) **Prior Publication Data**

US 2006/0064656 A1 Mar. 23, 2006

(51) **Int. Cl.**
G06F 17/50 (2006.01)

(52) **U.S. Cl.** **716/5**

(58) **Field of Classification Search** 716/5
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,009,251 A * 12/1999 Ho et al. 716/5
6,829,754 B1 * 12/2004 Yu et al. 716/5
2004/0025126 A1 * 2/2004 Culler et al. 716/5
2005/0055654 A1 * 3/2005 Lin et al. 716/5
2005/0097488 A1 * 5/2005 Lakshmanan et al. 716/7
2005/0108666 A1 * 5/2005 Chang et al. 716/2
2005/0125754 A1 * 6/2005 Schubert et al. 716/5

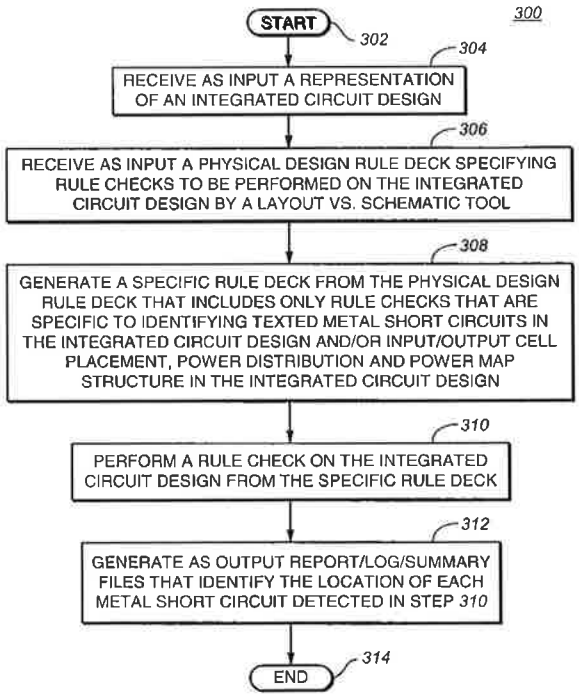
* cited by examiner

Primary Examiner—Stacy A. Whitmore
(74) *Attorney, Agent, or Firm*—Eric James Whitesell

(57) **ABSTRACT**

A method and computer program product for early physical design validation and identification of texted metal short circuits in an integrated circuit design includes steps of: (a) receiving as input a representation of an integrated circuit design; (b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design; (c) generating a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to one of identifying texted metal short circuits in the integrated circuit design and power distribution and input/output cell placement in the integrated circuit design; and (d) performing a physical design validation on the integrated circuit design from the specific rule deck.

12 Claims, 3 Drawing Sheets



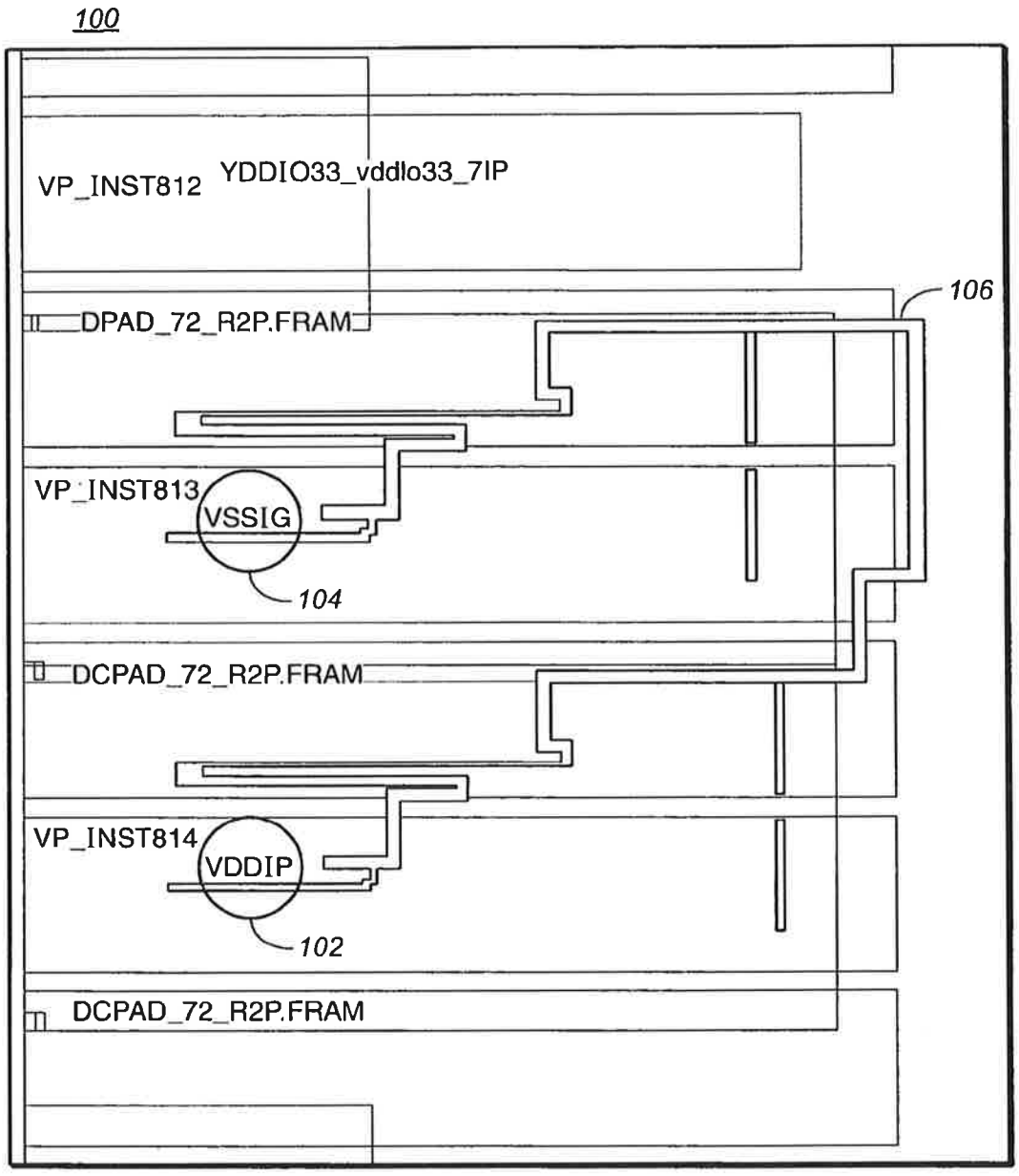

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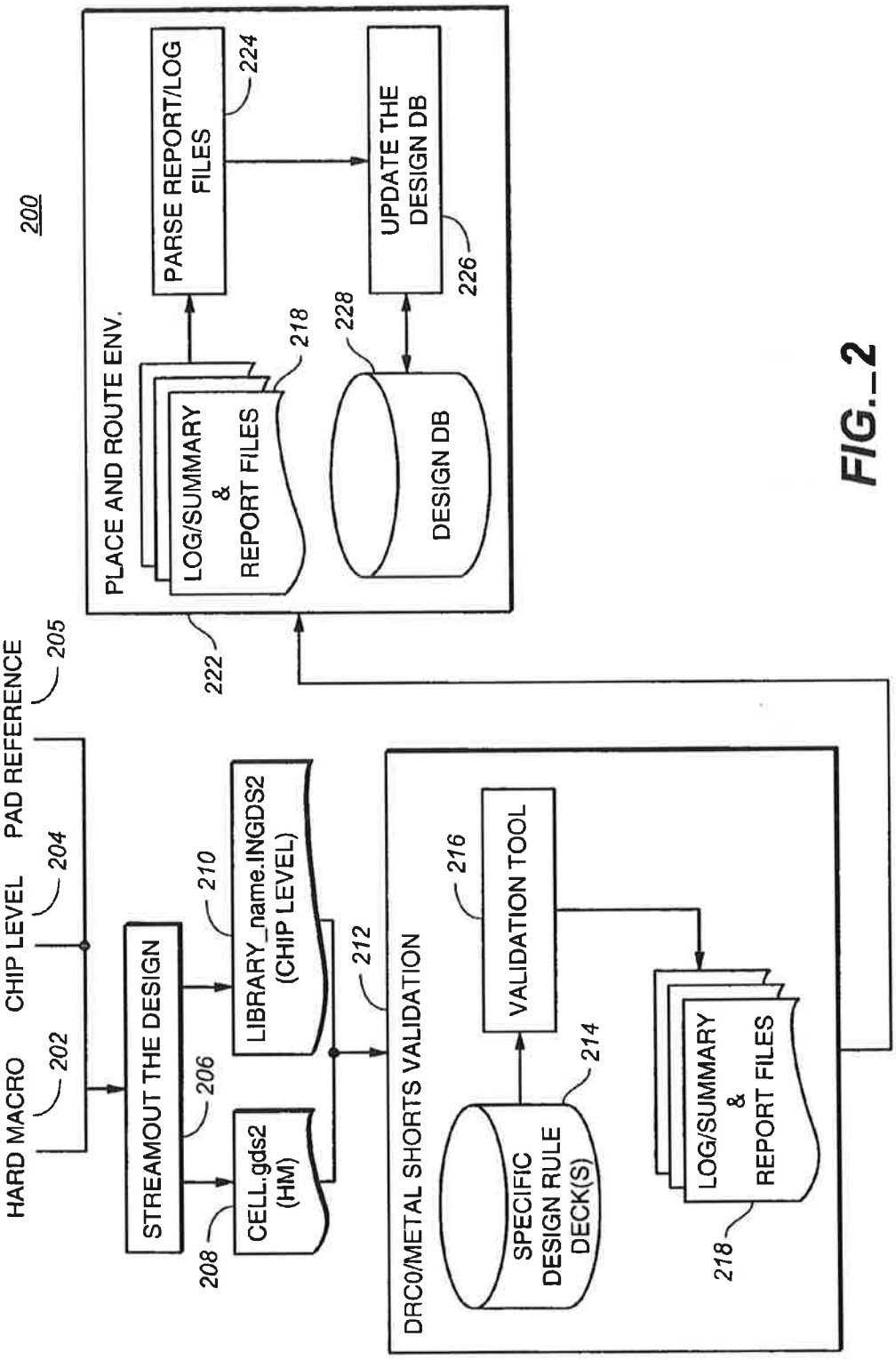
FIG._1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PLACE AND ROUTE ENV.
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LOG/SUMMARY & REPORT FILES
218
PARSE REPORT/LOG FILES
224
DESIGN DB
228
UPDATE THE DESIGN DB
226
DRC0/METAL SHORTS VALIDATION
VALIDATION TOOL
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SPECIFIC DESIGN RULE DECK(S)
214
LOG/SUMMARY & REPORT FILES
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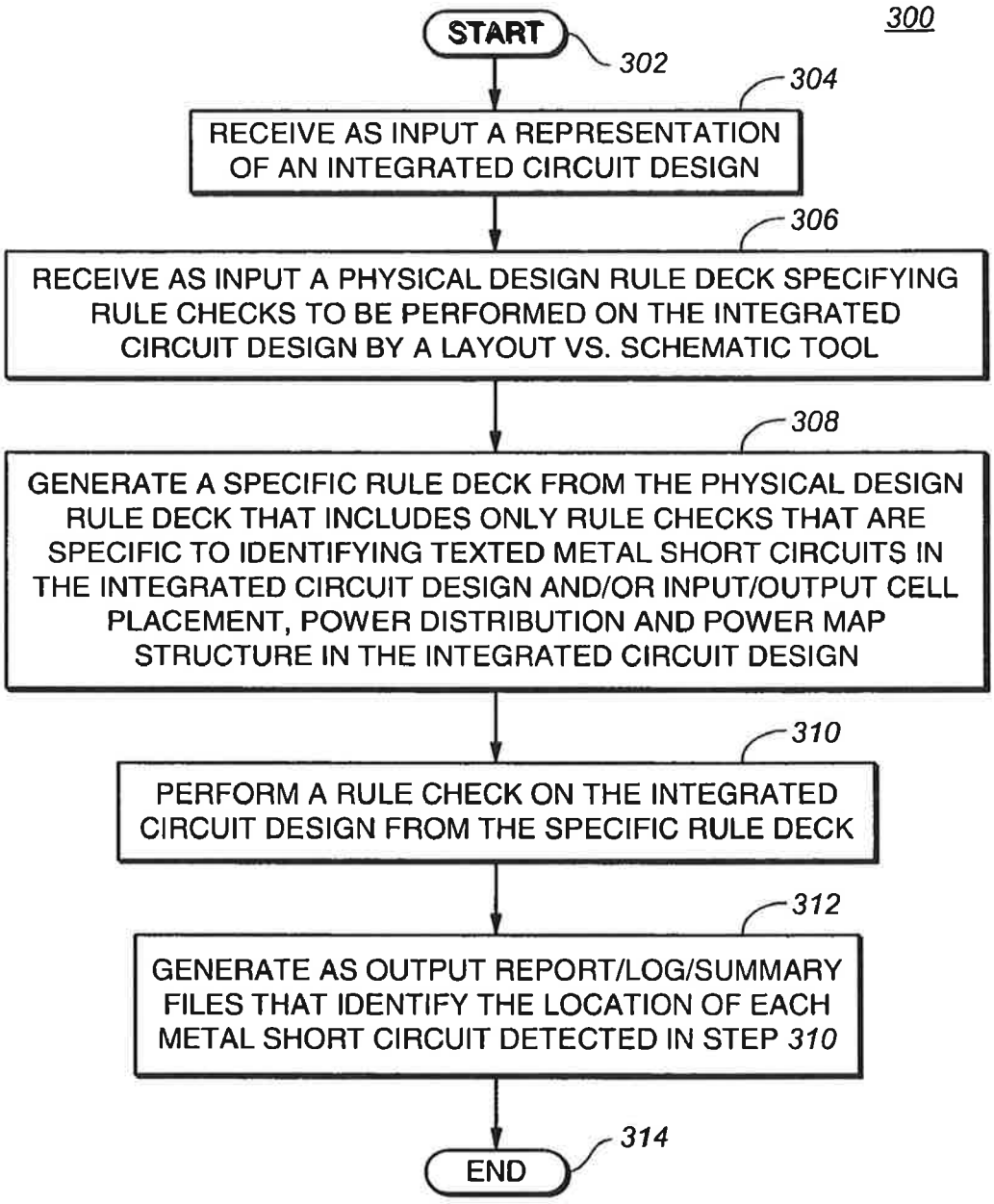
FIG._2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304
RECEIVE AS INPUT A REPRESENTATION OF AN INTEGRATED CIRCUIT DESIGN
306
RECEIVE AS INPUT A PHYSICAL DESIGN RULE DECK SPECIFYING RULE CHECKS TO BE PERFORMED ON THE INTEGRATED CIRCUIT DESIGN BY A LAYOUT VS. SCHEMATIC TOOL
308
GENERATE A SPECIFIC RULE DECK FROM THE PHYSICAL DESIGN RULE DECK THAT INCLUDES ONLY RULE CHECKS THAT ARE SPECIFIC TO IDENTIFYING TEXTED METAL SHORT CIRCUITS IN THE INTEGRATED CIRCUIT DESIGN AND/OR INPUT/OUTPUT CELL PLACEMENT, POWER DISTRIBUTION AND POWER MAP STRUCTURE IN THE INTEGRATED CIRCUIT DESIGN
310
PERFORM A RULE CHECK ON THE INTEGRATED CIRCUIT DESIGN FROM THE SPECIFIC RULE DECK
312
GENERATE AS OUTPUT REPORT/LOG/SUMMARY FILES THAT IDENTIFY THE LOCATION OF EACH METAL SHORT CIRCUIT DETECTED IN STEP 310
314
END

FIG._3

METHOD OF EARLY PHYSICAL DESIGN VALIDATION AND IDENTIFICATION OF TEXTED METAL SHORT CIRCUITS IN AN INTEGRATED CIRCUIT DESIGN

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the design of integrated circuits. More specifically, but without limitation thereto, the present invention relates to methods of verifying an integrated circuit design to ensure adherence to process rules and overall manufacturability of the integrated circuit design for a specific technology.

2. Description of Related Art

Physical design validation of an integrated circuit design is an important aspect of the overall design flow. The physical design verification step ensures that the design of the integrated circuit die complies to all process rules and that any additional required steps specific to manufacturability for a selected technology have been performed, for example, metal utilization.

SUMMARY OF THE INVENTION

In one aspect of the present invention, a method of early physical design validation and identification of texted metal short circuits in an integrated circuit design includes steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design;

(c) generating a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to one of identifying texted metal short circuits in the integrated circuit design and power distribution and input/output cell placement in the integrated circuit design; and

(d) performing a physical design validation on the integrated circuit design from the specific rule deck.

In another aspect of the present invention, a computer program product for early physical design validation and identification of texted metal short circuits in an integrated circuit design includes:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design;

(c) generating a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to one of identifying texted metal short circuits in the integrated circuit design and power distribution and input/output cell placement in the integrated circuit design; and

(d) performing a physical design validation on the integrated circuit design from the specific rule deck.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements throughout the several views of the drawings, and in which:

FIG. **1** illustrates a computer display of a texted metal short circuit identified by a layout vs. schematic tool according to the prior art;

FIG. **2** illustrates a computer software diagram of early physical design validation and identification of texted metal short circuits in an integrated circuit design according to an embodiment of the present invention; and

FIG. **3** illustrates a flow chart of a method of early physical design validation and identification of texted metal short circuits in an integrated circuit design according to an embodiment of the present invention.

Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some elements in the figures may be exaggerated relative to other elements to point out distinctive features in the illustrated embodiments of the present invention.

DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

The physical design validation of an integrated circuit design ensures that all spatial constraints are satisfied for the traces and devices formed in various layers of an integrated circuit die. The structures formed in the several layers of an integrated circuit die are typically represented in a GDS2 (Generic Data Stream) format file that contains the chip topological information for creating the masks used in manufacturing the integrated circuit dies. The GDS2 format is an industry standard used by commercially available physical verification tools to represent physical design data.

Physical design validation is typically performed at the very end of the design cycle, that is, when all components of the integrated circuit design have been placed and routed. A problem with placing the physical design validation step at the end of the design flow is that a design fault detected so late might reset the time schedule for the entire integrated circuit design, depending on the severity of the problem. The design may have to be re-floorplanned, and the entire design cycle may have to be reiterated.

To avoid the disadvantages of late detection of design defects, a physical validation tool may be run on the GDS2 file during the early evolution of the design instead of at the end of the design cycle. Unfortunately, performing an early physical design validation with an entire set of process design rules for a specific technology would require a substantial amount of computer processing time that would severely impact the product turnaround time. Also, a large number of design errors would be falsely reported as design rule violations due to the incomplete circuit design, making it difficult to sort out the design errors that need to be corrected before the circuit design is completed.

Examples of a physical validation tool are a design rule check (DRC) tool and a layout vs. schematic (LVS) tool. A commercially available physical validation tool that includes a design rule check tool and a layout vs. schematic tool is the Calibre tool, which is available from Mentor Graphics Corporation. The method of the present invention provides design rules that may be used in conjunction with a design rule check tool and/or a layout vs. schematic tool in an early stage of the physical design to detect design rule

violations in floorplanning, including input/output cell placement and construction and power distribution and power map structure. Also, texted metal short circuits may be identified most advantageously in the early or evolutionary aspects of the design flow, however, the identification of texted metal short circuits may be used at any point in the physical design validation flow. For example, texted metal short circuits may be identified in the power map in the early aspects of the design flow, advantageously reducing the computer processing time required to validate an integrated circuit design. The power map is created early in the design flow and should be consistent throughout the evolution of the design. Otherwise, there may be components in the integrated circuit design that are not connected to power and ground, or severe voltage droop may occur at some components in the integrated circuit design, and so on. If the power map is not validated early in the design flow, design defects may result in costly schedule delays and unacceptable turnaround time.

Previous methods of physical design validation do not check the physical design in the early stages of the design flow only from the perspective of metal short circuits or a limited subset of the process design rules for example, to ensure metal utilization compliance within the input/output cells and metal spacing and width constraints. However, a typical integrated circuit design may have a large amount of routing information created automatically and by manual entry, which greatly increases the likelihood of design rule violations such as a metal short circuit in the design. A metal short circuit is simply a metal connection between two different signal or power sources. An important example of a problematic metal short circuit is one between the supply voltage (VDD) and ground (VSS).

A typical layout vs. schematic tool uses several input files that are used in conjunction with a rule deck to detect design rule violations. One such file is the pad reference file. The pad reference file is used to associate a signal source location with a text name, for example:

TEXT "VDD: P"	−4663.23	1918.53	96
TEXT "VSS: G"	−4663.23	1836.53	96

The layout vs. schematic tool places the text signal names from the pad reference file, in this example, VDD and VSS, on the chip at the corresponding numerical XYZ coordinates associated with the text signal names. The coordinates are located on the bond site of each I/O pad cell in the chip. The layout vs. schematic tool traverses the GDS2 design file to ensure that there are no conflicting text entries on the net being traversed. For example, if a net has been texted, that is, named, with the text entry "CLK", then the rest of the net is traversed to ensure that there are no conflicting text entries on the net being traversed. A piece of metal in the chip that connects two different signal sources results in a "texted" metal short circuit.

Identifying texted metal short circuits in the physical design is a universal approach adopted in the industry to validate the physical design of an integrated circuit from a layout vs. schematic perspective. However, previous methods of physical design validation include design rules for detecting texted metal short circuits with all the other physical design rules used to validate the entire integrated circuit design, resulting in a less than optimum turnaround time for the integrated circuit design flow.

FIG. **1** illustrates a computer display **100** of a texted metal short circuit identified by a layout vs. schematic tool according to the prior art. Shown in the computer display **100** are text signal names **102** and **104** and a highlighted path **106**.

In FIG. **1**, the computer display **100** shows the text signal names **102** (VDD:P) and **104** (VSS:G) and the highlighted path **106** that connects them. The metal short circuit may be anywhere along the highlighted path **106**. The exact location of the metal short circuit is typically included in a report file generated by the layout vs. schematic tool. Because the layout vs. schematic tool is typically not employed until near the end of the design cycle, texted metal short circuits may not be detected until late in the design after a large amount of computer time has already been invested.

The method of the present invention exploits the capability of the layout vs. schematic tool to detect metal short circuits by reducing the standard design rule deck used for physical design validation to include only those design rules needed to detect texted metal short circuits. The physical design validation step is then performed on the reduced rule deck early in the integrated circuit design cycle.

In one aspect of the present invention, a method includes steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design;

(c) generating a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to one of identifying texted metal short circuits in the integrated circuit design and power distribution and input/output cell placement in the integrated circuit design; and

(d) performing a physical design validation on the integrated circuit design from the specific rule deck.

FIG. **2** illustrates a computer software diagram **200** of a method of early physical design validation and detection of texted metal short circuits according to an embodiment of the present invention. Shown in FIG. **2** are a hard macro file **202**, a chip level file **204**, a pad reference file **205**, a stream-out tool **206**, a hard macro cell GDS2 description file **208**, a chip level cell GDS2 description file **210**, an early design rule check and texted metal short circuit verification environment **212**, a specific rule deck **214**, a validation tool **216**, report/summary/log files **218**, a place and route environment **222**, a report file parser **224**, a design database update tool **226**, and a design database **228**.

The hard macro file **202**, the chip level file **204**, and the pad reference file **205** are generated by a circuit designer according to well known integrated circuit design techniques.

The stream-out tool **206** generates the hard macro cell GDS2 description file **208** and the chip level cell GDS2 description file **210** according to well known techniques from the hard macro file **202** and the chip level file **204**. The GDS2 description files **208** and **210** define the structures formed in the several layers of an integrated circuit die in a format that contains the chip topological information used for creating the masks used in manufacturing the integrated circuit dies.

The early design rule check and texted metal short circuit verification environment **212** includes the specific rule deck **214**, the validation tool **216**, and the report/summary/log files **218**. The specific deck **214** is an important feature of the present invention, because the specific rule deck **214** includes only rules that are specific to the detection of texted

metal short circuits and/or rules that are specific to, for example, metal utilization within the input/output cells, power map metal spacing and width constraints associated with the metal layers used in the power map, via structures in the integrated circuit design, and metal slots used in the integrated circuit design. The reduced number of design rules used in the specific rule deck **214** compared to a general design rule deck advantageously reduces the run time required to perform a physical design validation on the integrated circuit design, and can detect design errors that may be corrected before investing the time required to generate and validate the entire integrated circuit design. The specific rule deck may be a separate rule deck that only includes rules that are specific to the detection of texted metal short circuits, or the specific rule deck may be a separate rule deck that includes only rule violations that are specific to an early design rule check (DRC**0**), for example, metal utilization within the input/output cells, power map metal spacing and width constraints associated with the metal layers used in the power map, via structures in the integrated circuit design, and metal slots used in the integrated circuit design. The specific rule deck may also be a combination of the separate rule decks.

Examples of design rules for inclusion in the specific rule deck that are specific to the early detection of design rule violations for a selected integrated circuit manufacturing technology include but are not limited to:

(1) cells not connected to power (VDD);
(2) cells not connected to ground (VSS);
(3) power and ground paths closer to each other than a minimum allowed spacing;
(4) via/contact spacing less than a minimum allowed spacing;
(5) via/contact size less than a minimum metal size;
(6) wide power buses that do not have the correct number of slots;
(7) metal layer width, spacing and hole dimensions not within allowed range; and
(8) I/O and core regions of the chip exceed maximum allowed limits for the selected technology.

The specific rule deck **214** may be, for example, a text file that implements the various rule requirements in a rule format such as the Standard Verification Rule Format (SVRF) commonly used by commercially available physical design validation tools.

The validation tool **216** may be, for example, a design rule check (DRC) tool and/or a layout vs. schematic (LVS) tool. An exemplary validation tool is Calibre, a commercially available software program from Mentor Graphics Corporation that validates the adherence of the integrated circuit design to the rules specified in the design rule deck.

The report/summary/log files **218** are generated by the validation tool **216** and include a summary of the design rule checks performed on the integrated circuit design and the number of violations detected for each of the design rules. The report/summary/log files **218** also provide the precise locations of each of the texted metal short circuits detected in the integrated circuit design so that the circuit designer can readily correct design defects in an efficient manner.

The report file parser **224** parses the report/summary/log files **218** according to well known techniques to provide the circuit designer with the information needed to correct the rule violations.

The design database update tool **226** may be, for example, a commercially available software tool used to update the design database **228** with the corrections to the integrated design.

FIG. **3** illustrates a flow chart **300** of a method of early physical design validation and identification of texted metal short circuits in an integrated circuit design according to an embodiment of the present invention.

Step **302** is the entry point of the flow chart **600**.

In step **304**, a representation of an integrated circuit design is received as input. In this example, the representation is a GDS2 design database, however, other formats for representing a circuit design may also be used to practice the present invention within the scope of the appended claims.

In step **306**, a physical design rule deck is received as input specifying rule checks to be performed on the entire integrated circuit design by a layout vs. schematic tool.

In step **308**, a specific rule deck is generated from the physical design rule deck that includes only rule checks that are specific to identifying texted metal short circuits in the integrated circuit design and/or input/output cell placement, power distribution and power map structure in the integrated circuit design. Alternatively, the specific rule deck may be generated directly as described above in Standard Verification Rule Format (SVRF).

In step **310**, a physical design validation is performed on the integrated circuit design from the specific rule deck to identify rule violations in the integrated circuit design. The physical design validation may be performed according to well known techniques, for example, by a design rule check tool and/or a layout vs. schematic tool.

In step **312**, report/summary/log files are generated as output that include the precise location of each texted metal short circuit identified in step **310**. The circuit designer may then make the appropriate corrections to the integrated circuit design database.

Step **314** is the exit point of the flow chart **300**.

As may be appreciated from the above, the method of the present invention provides a flexible and robust architecture that can accommodate both in-house and third-party physical design validation tools and can work with a wide variety of computer resources.

Although the method of the present invention illustrated by the flowchart description above is described and shown with reference to specific steps performed in a specific order, these steps may be combined, sub-divided, or reordered without departing from the scope of the claims. Unless specifically indicated herein, the order and grouping of steps is not a limitation of the present invention.

The steps described above with regard to the flow chart described above may also be implemented by instructions performed on a computer according to well-known computer programming techniques.

In another aspect of the present invention, a computer program product includes:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design;

(c) generating a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to one of identifying texted metal short circuits in the integrated circuit design and power distribution and input/output cell placement in the integrated circuit design; and

(d) performing a physical design validation on the integrated circuit design from the specific rule deck.

While the invention herein disclosed has been described by means of specific embodiments and applications thereof, numerous modifications and variations could be made thereto by those skilled in the art without departing from the scope of the invention set forth in the following claims.

What is claimed is:

1. A method comprising steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design;

(c) generating a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design; and

(d) performing a physical design validation on the integrated circuit design from the specific rule deck to identify texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design.

2. The method of claim 1 further comprising performing step (d) prior to performing a physical design validation that includes a design rule that is not included in the specific rule deck.

3. The method of claim 1 further comprising a step of including in the specific rule deck a rule check for at least one of:

via/contact spacing less than a minimum allowed spacing;

via/contact size less than a minimum metal size;

wide power buses that do not have the correct number of slots;

metal layer width, spacing and hole dimensions not within allowed range; and

input/output cell and core cell regions of the chip exceed maximum allowed limits for a selected technology.

4. The method of claim 1 further comprising a step of generating as output a report file that includes a location of each texted metal short circuit identified in step (d).

5. The method of claim 1 wherein the representation of the integrated circuit design is a Generic Data Stream format file.

6. The method of claim 1 wherein the physical design validation is performed by one of a design rule check tool and a layout vs. schematic tool.

7. A computer program product comprising:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design;

(c) generating a specific rule deck from the physical design rule deck to include only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design; and

(d) performing a physical design validation on the integrated circuit design from the specific rule deck to identify texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design.

8. The computer program product of claim 7 further comprising performing step (d) prior to performing a physical design validation that includes a design rule that is not included in the specific rule deck.

9. The computer program product of claim 7 further comprising a step of including in the specific rule deck a rule check for at least one of:

via/contact spacing less than a minimum allowed spacing;

via/contact size less than a minimum metal size;

wide power buses that do not have the correct number of slots;

metal layer width, spacing and hole dimensions not within allowed range; and

input/output cell and core cell regions of the chip exceed maximum allowed limits for a selected technology.

10. The computer program product of claim 7 farther comprising a step of generating as output a report file that includes a location of each texted metal short circuit identified in step (d).

11. The computer program product of claim 7 wherein the representation of the integrated circuit design is a Generic Data Stream format file.

12. The computer program product of claim 7 wherein the physical design validation is performed by one of a design rule check tool and a layout vs. schematic tool.

* * * * *

EXHIBIT C

BELL SEMICONDUCTOR LLC'S ANALYSIS OF INFRINGEMENT

U.S. Patent No. 7,260,803

Claims 1–6 & 9–11

Bell Semiconductor ("Bell Semic") provides evidence of infringement of exemplary claims 1–6 & 9–11 of U.S. Patent No. 7,260,803 ("the '803 patent") by the LCMX02-7000HC produced by Lattice Semiconductor, Inc. ("Lattice"). In support thereof, Bell Semic provides the following claim charts.

"Accused Products" as used herein refers to at least devices produced or sold by Lattice that are or include semiconductor integrated circuit devices made using a design tool that, checks for dummy metal objects intersecting any other objects in the design data following a change to a portion of the design data, and if so, deletes any such intersecting dummy metal objects to avoid having to re-run the dummy fill tool, with the understanding that infringement has also taken place through the manufacture, importation, offer for sale, and/or sale of products including such Accused Products. These claim charts demonstrate infringement by comparing each element of the asserted claims to corresponding components, aspects, and/or features of the Accused Products. These claim charts are not intended to constitute an expert report on infringement. These claim charts include information provided by way of example, and not by way of limitation.

The analysis set forth below is based only upon information from available resources regarding the Accused Products, as Lattice has not yet provided any non-public information. An analysis of Cadence's, Lattice's and/or other third partiestechnical documentation may assist in fully identifying all infringing features and functionality. Accordingly, Bell Semic reserves the right to supplement this infringement analysis once such information is made available to Bell Semic. Furthermore, Bell Semic reserves the right to revise this infringement analysis, as appropriate, upon issuance of a court order construing any terms recited in the asserted claims.

Unless otherwise noted, Bell Semic contends that Lattice and customers of Lattice directly infringe under 35 U.S.C. § 271(a) the '803 patent by selling, offering to sell, making, using, and/or importing semiconductor products designed and/or produced at least in part by the Accused Products. Unless otherwise noted, Bell Semic further contends that the evidence below supports a finding of indirect infringement under 35 U.S.C. §§ 271(b) and/or (c), in conjunction with other evidence of liability under one or more of those subsections. Lattice and/or its customers make, use, sell, import, or offer for sale in the United States, or have done the same in the past, without authority, and/or induce or have induced others to make, use, sell, import, or offer for sale in the United States, without authority products, equipment, or services that infringe claims 1–6 & 9–11 of the '803 patent, including without limitation, the Accused Products or semiconductor products designed and/or produced at least in part using the Accused Products.

Unless otherwise noted, Bell Semic believes and contends that each element of each claim asserted herein is literally met through Lattice's provision of the Accused Products. However, to the extent that Lattice attempts to allege that any asserted claim element is not literally met, Bell Semic believes and contends that such elements are met under the doctrine of equivalents. More specifically, in its investigation and analysis of the Accused Products, Bell Semic did not identify any substantial differences between the elements of the patent claims and the corresponding features of the Accused Products, as set forth herein. In each instance, the identified feature of the Accused Products performs at least substantially the same function in substantially the same way to achieve substantially the same result as the corresponding claim element.

BELL SEMICONDUCTOR LLC'S ANALYSIS OF INFRINGEMENT

To the extent the chart of an asserted claim relies on evidence about certain specifically-identified Accused Products, Bell Semic asserts that, on information and belief, any similarly-functioning instrumentalities also infringes the charted claim. Bell Semic reserves the right to amend this infringement analysis based on other products made, used, sold, imported, or offered for sale by Lattice. Bell Semic also reserves the right to amend this infringement analysis by citing other claims of the '803 patent, not listed in the claim chart, that are infringed by the Accused Products. Bell Semic further reserves the right to amend this infringement analysis by adding, subtracting, or otherwise modifying content in the "Accused Products" column of each chart.

Lattice is a customer of at least Cadence, Synopsys, and Siemens, as demonstrated here: https://www.cadence.com/en_US/home/multimedia.html/content/dam/cadence-www/global/en_US/videos/tools/custom-_ic_analog_rf_design/maryam_shahbazi_lattice (Cadence); https://news.synopsys.com/index.php?s=20295&item=123188 (Synopsys); https://www.latticesemi.com/view_document?document_id=53646 (all).

Lattice is the producer and/or seller of the referenced above, as demonstrated by the following package image for the LCMX02-7000HC.

CLAIM CHARTS
CADENCE AND USERS
U.S. Patent No. 7,260,803

Claim 1	Accused Products
1. A method for performing dummy metal insertion in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool, comprising:	To the extent the preamble is limiting, the Accused Products are made, produced, or processed by performing a method for inserting dummy metal in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool. The Accused Products are made, produced, or processed by design tools from at least one of Cadence, Synopsys, and Siemens to insert dummy metal in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool. For example, Lattice creates design data for the LCMX02-7000HC,which was made, produced, or processed from that design data using one of the above-identified and described design tools to insert dummy metal in the design data, which includes dummy metal objects inserted by a dummy fill tool. To the extent the preamble is limiting, the Cadence Innovus tool is used to perform dummy metal insertion in design data for ainintegrated circuit, which includes dummy metal objects inserted by the dummy fill tool:

Recommendations for In-design Sign-off Metal Fill Flow

In the recommended flow, the software calls the Pegasus/PVS engine to insert sign-off metal fill in design. The metal fill near critical nets can be trimmed for timing closure.

Use the fill commands in the following order:

1. Insert sign-off metal fill in design.

   Before inserting sign-off metal fill, stream out a GDSII stream file of the current database. Specify the mapping file and units that match with the rule deck you specify while inserting metal fill. If necessary, include the detailed-cell Graphic Database System (GDS).

   Note: Prepare the mapping file to align with the rule deck layer definition. Use the same unit as the rule deck.

   If using Pegasus:

   ```
   streamOut -mapFile $gds_map -outputMacros -units $gds_unit pegasus.fill.gds
   ```

   `run_pegasus_metal_fill` calls the Pegasus engine to insert metal fill and then dump the metal fill in Innovus. The DEF mapping file is required to ensure that the metal fill is put in the correct layers. The top cell name is also required.

   ```
   run_pegasus_metal_fill -ruleFile $MF_RULE_DECK -defMapFile $def_out -gdsFile pegasus.fill.gds -cell $top_cell
   ```

   If using PVS:

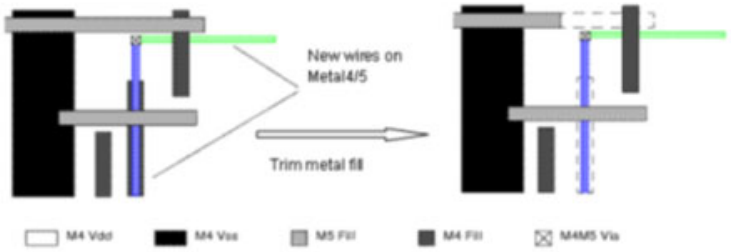
   ```
   streamOut -mapFile $gds_map -outputMacros -units $gds_unit pvs.fill.gds
   ```

   `run_pvs_metal_fill` calls the PVS engine to insert metal fill and then dump the metal fill in Innovus. The DEF mapping file is required to ensure that the metal fill is put in the correct layers. The top cell name is also required.

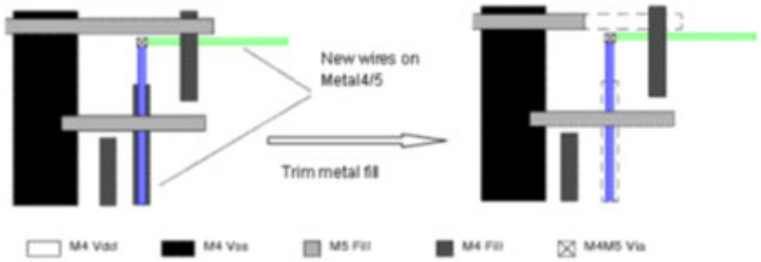
   ```
   run_pvs_metal_fill -ruleFile $MF_RULE_DECK -defMapFile $def_out -gdsFile pvs.fill.gds -cell $top_cell
   ```

See Innovus Manual at 717-18.

CLAIM CHARTS
CADENCE AND USERS
U.S. Patent No. 7,260,803

(a) after a portion of the design data is changed, performing a check to determine whether any dummy metal objects intersect with any other objects in the design data; and	The Accused Products are made, produced, or processed from design data that performs a check to determine whether any dummy metal objects intersect with any other objects in the design data after a portion of the design data is changed.
	
	Trimming Metal Fill
	
	The automatic routers, including the NanoRoute® router, ignore metal fill (`FILLWIRE` and `FILLWIREOPC`) shapes and might create routes that cause shorts or DRC violations.
	
	The following case illustrates the DRC violation after NanoRoute ECO. You can use `trimMetalFill` to clean the violations according to user setting, LEF setting, and default parameters.
	
	`trimMetalFill -deleteViol`
	
	 
	
	This command deletes metal fill shapes that cause DRC violations or shorts. After running the `trimMetalFill` command, the remaining shapes are still rectangles.
	
	This means you need not delete the metal fill before ECO and then add it again after ECO. Instead, you can trim metal fill in the window that has been impacted by ECO. `trimMetalFill` can minimize the impact caused by the ECO on the timing of other paths (due to cross-coupling changes) that were not involved in the ECO.
	
	To remove the shorts and violations, complete the following steps:
	
	◦ To remove floating metal fill that causes shorts or violations, run the following command:
	`trimMetalFill [-deleteViol] [-ignoreSpecialNet]`
	
	This command repairs violations caused by the metal fill shapes. If the metal density drops below the target after trimming the metal fill, re-run the `addMetalFill` command.
	
	The `trimMetalFill` command trims metal and via fill shapes based on the following spacing rules:
	
	◦ Between `FILLWIRE` and `FILLWIREOPC` shapes, the active spacing value or minimum spacing based on DRC rules, whichever is larger, is required.
	
	See Innovus Manual at 722-23.

	A POSITA would have understood that trimming metal fill that causes shorts or violations first requires determining whether any dummy metal objects intersect other objects in the design data.

(b) deleting the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool.	The Accused Products are made, produced, or processed from design data via deleting the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool.
	
	Trimming Metal Fill
	
	The automatic routers, including the NanoRoute® router, ignore metal fill (`FILLWIRE` and `FILLWIREOPC`) shapes and might create routes that cause shorts or DRC violations.
	
	The following case illustrates the DRC violation after NanoRoute ECO. You can use `trimMetalFill` to clean the violations according to user setting, LEF setting, and default parameters.
	
	`trimMetalFill -deleteViol`
	
	 
	
	This command deletes metal fill shapes that cause DRC violations or shorts. After running the `trimMetalFill` command, the remaining shapes are still rectangles.
	
	This means you need not delete the metal fill before ECO and then add it again after ECO. Instead, you can trim metal fill in the window that has been impacted by ECO. `trimMetalFill` can minimize the impact caused by the ECO on the timing of other paths (due to cross-coupling changes) that were not involved in the ECO.
	
	To remove the shorts and violations, complete the following steps:
	
	◦ To remove floating metal fill that causes shorts or violations, run the following command:
	`trimMetalFill [-deleteViol] [-ignoreSpecialNet]`
	
	This command repairs violations caused by the metal fill shapes. If the metal density drops below the target after trimming the metal fill, re-run the `addMetalFill` command.
	
	The `trimMetalFill` command trims metal and via fill shapes based on the following spacing rules:
	
	◦ Between `FILLWIRE` and `FILLWIREOPC` shapes, the active spacing value or minimum spacing based on DRC rules, whichever is larger, is required.
	
	See Innovus Manual at 722-23.

2. The method of claim 1 wherein step (a) further includes: prior to implementing the change, saving the dummy metal objects from the design data to a file.	The Accused Products are made, produced, or processed from design data via, prior to implementing the change, saving the dummy metal objects from the design data to a file. **Viewing DRC or Metal Density Violations** The Violation Browser updates violation markers generated by the `verify_drc` and `verifyMetalDensity` commands incrementally in an Innovus session--that is, it displays the markers generated the first time you run either of these commands and adds new markers, or deletes markers, from subsequent runs during the same session. If the software finds violations during a subsequent run that were already found previously, the browser display does not change, as there is no incremental update. The browser can make the incremental changes because `verify_drc` and `verifyMetalDensity` can check a small area of the design and update the database. As a result of this behavior, the Innovus software saves the information from the first verification run. See Innovus Manual at 1448. DRC violations caused by ECO are saved by the Innovus software.
3. The method of claim 2 wherein step (a) further includes: performing the check by accessing the dummy metal objects in the file.	The Accused Products are made, produced, or processed from design data via checking to determine whether any dummy metal objects intersect any other objects in the design data is performed by accessing the dummy metal objects in the file to which the dummy metal objects are saved from the design data. As shown in the Figure 6, the Innovus database contains the dummy fill data.

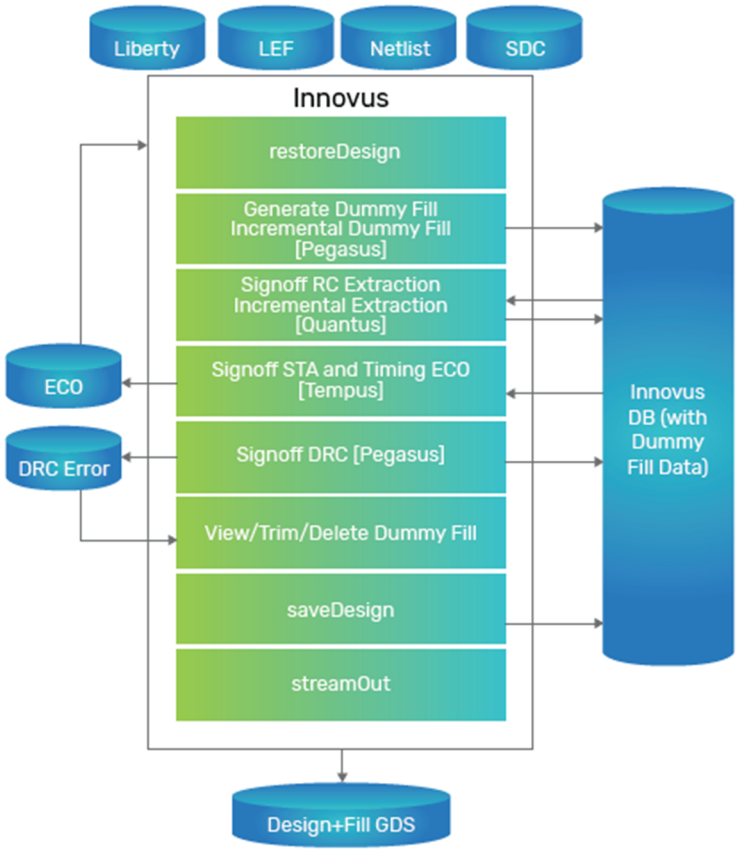


Figure 6: Hierarchical database flow

https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf, page 4

	Viewing DRC or Metal Density Violations The Violation Browser updates violation markers generated by the `verify_drc` and `verifyMetalDensity` commands incrementally in an Innovus session--that is, it displays the markers generated the first time you run either of these commands and adds new markers, or deletes markers, from subsequent runs during the same session. If the software finds violations during a subsequent run that were already found previously, the browser display does not change, as there is no incremental update. The browser can make the incremental changes because `verify_drc` and `verifyMetalDensity` can check a small area of the design and update the database. As a result of this behavior, the Innovus software saves the information from the first verification run. See Innovus Manual at 1448.
4. The method of claim 3 further including: reloading remaining dummy metal objects from the file to the design data.	The Accused Products were made, produced, or processed from design data via reloading remaining dummy metal objects from the file to the design data. A Person of Skill in the Art of Semiconductor design and layout would understand that after accessing the dummy metal objects in the file as part of the check, and then deleting intersecting dummy metal objects from the data, remaining dummy metal objects in the file would typically need to be reloaded to the design data in order to complete the process flow.

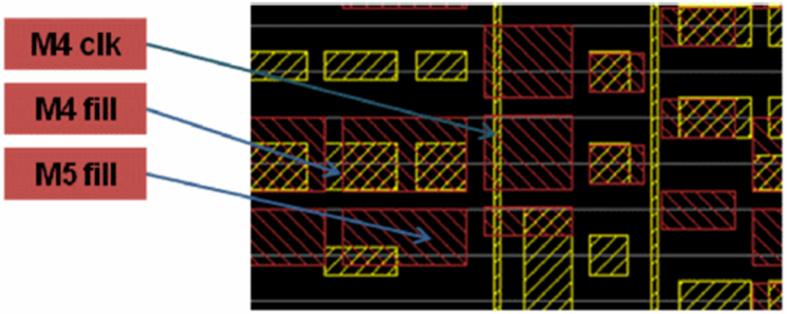
Viewing DRC or Metal Density Violations

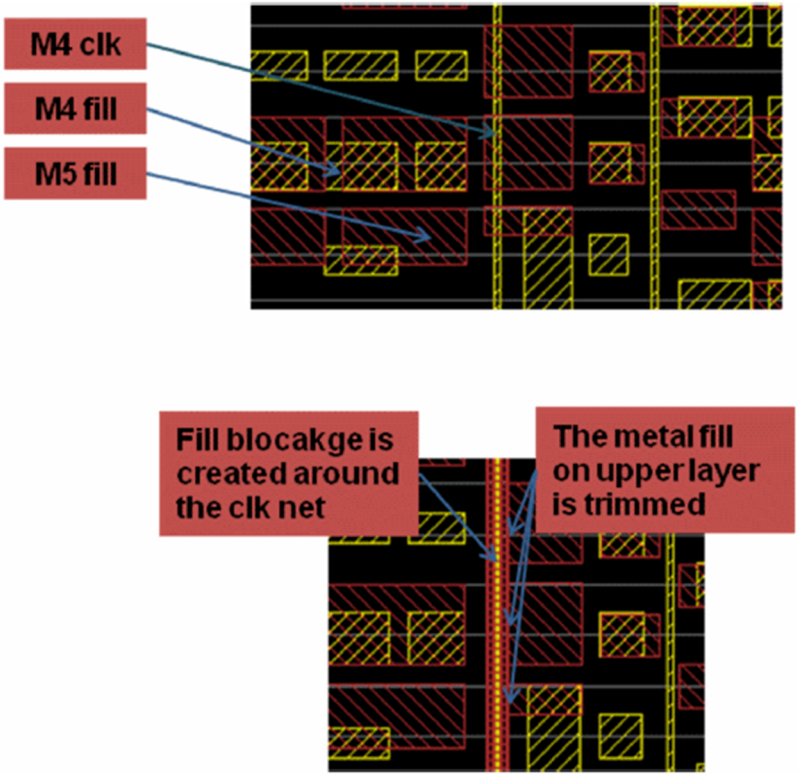
The Violation Browser updates violation markers generated by the `verify_drc` and `verifyMetalDensity` commands incrementally in an Innovus session--that is, it displays the markers generated the first time you run either of these commands and adds new markers, or deletes markers, from subsequent runs during the same session. If the software finds violations during a subsequent run that were already found previously, the browser display does not change, as there is no incremental update.

The browser can make the incremental changes because `verify_drc` and `verifyMetalDensity` can check a small area of the design and update the database. As a result of this behavior, the Innovus software saves the information from the first verification run.

See Innovus Manual at 1448.

	To remove the shorts and violations, complete the following steps: ◦ To remove floating metal fill that causes shorts or violations, run the following command: `trimMetalFill [-deleteViol] [-ignoreSpecialNet]` This command repairs violations caused by the metal fill shapes. If the metal density drops below the target after trimming the metal fill, re-run the `addMetalFill` command. See Innovus Manual at 723.
5. The method of claim 4 wherein step (a) further includes: performing the check by on the dummy metal objects in the file by,	The Accused Products were made, produced, or processed from design data via performing the check on the dummy metal objects in the file. **Viewing DRC or Metal Density Violations** The Violation Browser updates violation markers generated by the `verify_drc` and `verifyMetalDensity` commands incrementally in an Innovus session--that is, it displays the markers generated the first time you run either of these commands and adds new markers, or deletes markers, from subsequent runs during the same session. If the software finds violations during a subsequent run that were already found previously, the browser display does not change, as there is no incremental update. The browser can make the incremental changes because `verify_drc` and `verifyMetalDensity` can check a small area of the design and update the database. As a result of this behavior, the Innovus software saves the information from the first verification run. See Innovus Manual at 1448.
(i) annotating each dummy metal object with an attribute that	The Accused Products were made, produced, or processed from design data via performing the check on the dummy metal objects in the file by annotating each dummy metal object with an attribute identying it as dummy metal.

identifies it as dummy metal, and	 See Innovus Manual at 725. The Pegasus verification's HMF is generated in Innovus implementation by running the command add_metal_fill_ signoff -fill using the foundry-provided Pegasus rule deck. The properties of the generated metal fill, such as FILLWIRE and FILLWIREOPC are set appropriately, and the subse- quent flow can be handled in the same way as the normal metal fill pattern. For more details, see Figure 5. The Pegasus verification's HMF flow stores generated metal fill data in the Innovus implementation database as a metal fill database—which gives access to the Innovus, Quantus, and Pegasus solutions, as deemed necessary to process metal fill requirements. For more details, see Figure 6. *https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf, page 3*
(ii) examining nets of respective wires, and determining if a net identified as dummy metal	The Accused Products were also made, produced, or processed from design data via examination of nets of respective wires and dtermining if a net identified as dummy metal intersects with a net having a different name.

intersects with a net of a different name.	 See Innovus Manual at 725.
6. The method of claim 5 wherein step (b) further includes: (iii) deleting from the file any net identified as dummy metal that intersects with a net of a different name.	The Accused Products were made, produced, or processed, in the case of such intersections between dummy metal nets and nets having different names, by deleting from the file any net identified as dummy metal. When the initial signoff metal fill generation, RC extraction, timing analysis, and ECO are performed, some wiring patterns disappear, while some new patterns are generated. The newly added wiring pattern will cause a DRC violation between the initial metal fill and may be required to be removed. So, it is also essential to add metal fill to the empty spaces of the disappearing patterns of wires.

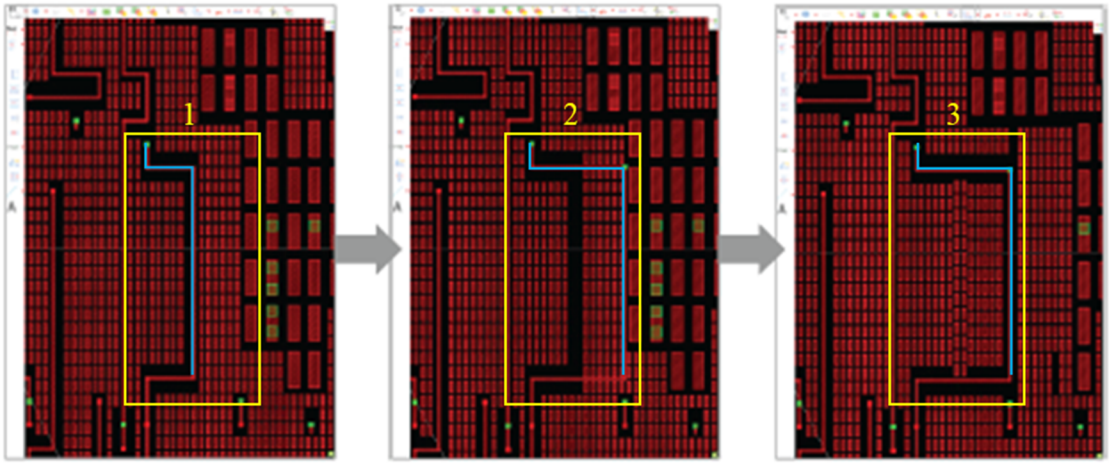
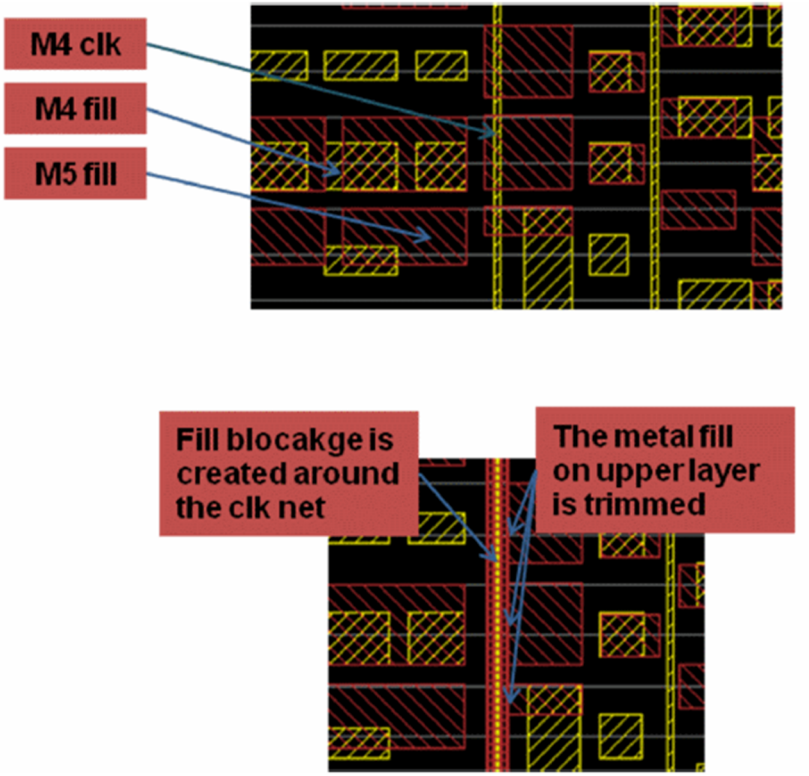


Figure 8: Pegasus incremental metal fill generation

https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf, pages 4 and 5

Note: For clarity, yellow boxes are added, and the ECO net is shown in light blue. Yellow Box 1: Original wiring pattern as depicted in light blue. Yellow Box 2: New wiring pattern per ECO as depicted in light blue. The newly added wiring pattern will cause a DRC violation between the initial metal fill. Yellow Box 3: Any dummy fill that intersects with the newly added wiring pattern is deleted.

	 See Innovus Manual at 725.
9. The method of claim 4 wherein step (a) further includes: changing the portion of the design data by implementing an engineering change order (ECO).	The Accused Products were made, produced, or processed from design data, of which, on information and belief, at least a portion of which was changed by implementation of an ECO.

	Viewing DRC or Metal Density Violations The Violation Browser updates violation markers generated by the `verify_drc` and `verifyMetalDensity` commands incrementally in an Innovus session--that is, it displays the markers generated the first time you run either of these commands and adds new markers, or deletes markers, from subsequent runs during the same session. If the software finds violations during a subsequent run that were already found previously, the browser display does not change, as there is no incremental update. The browser can make the incremental changes because `verify_drc` and `verifyMetalDensity` can check a small area of the design and update the database. As a result of this behavior, the Innovus software saves the information from the first verification run. See Innovus Manual at 1448.

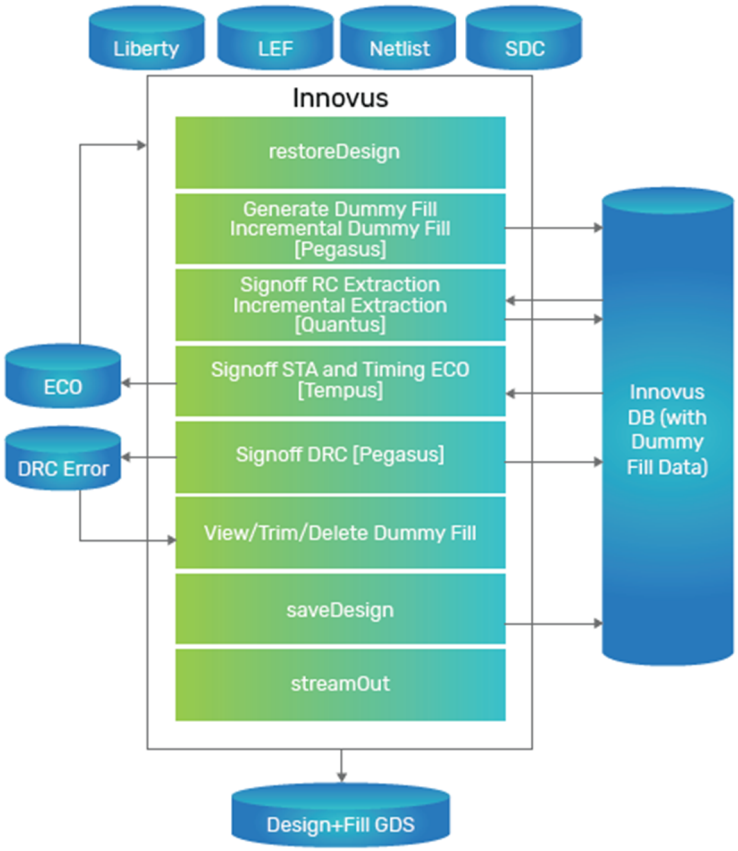
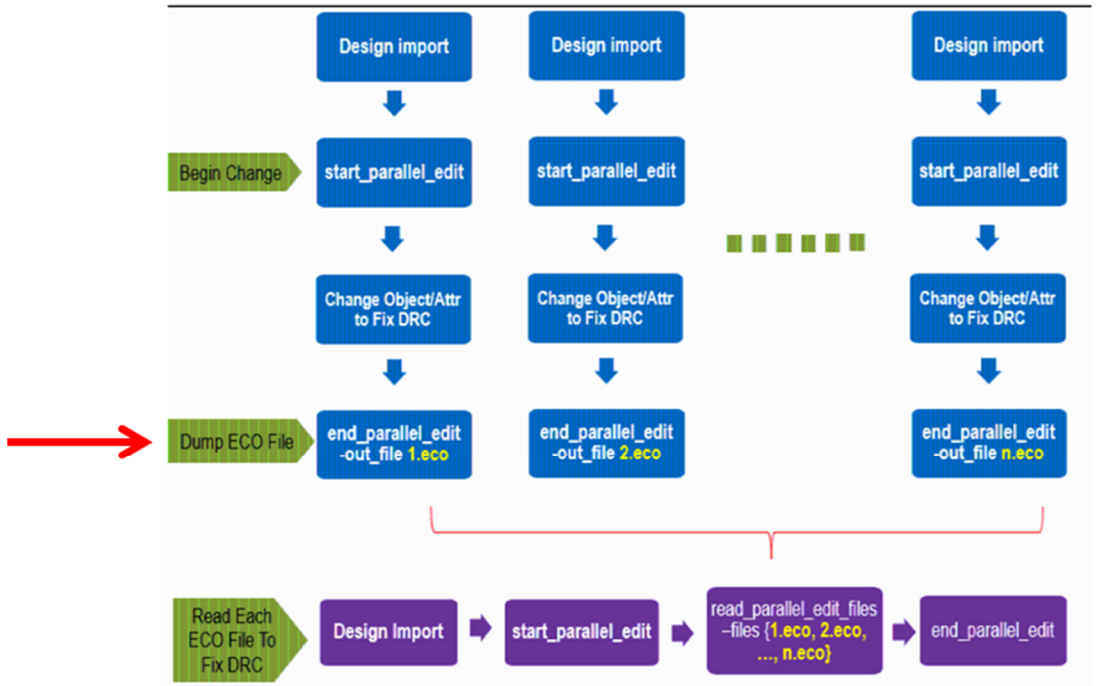


Figure 6: Hierarchical database flow

https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf, page 4

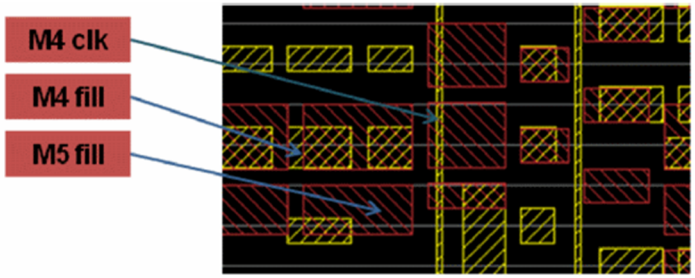
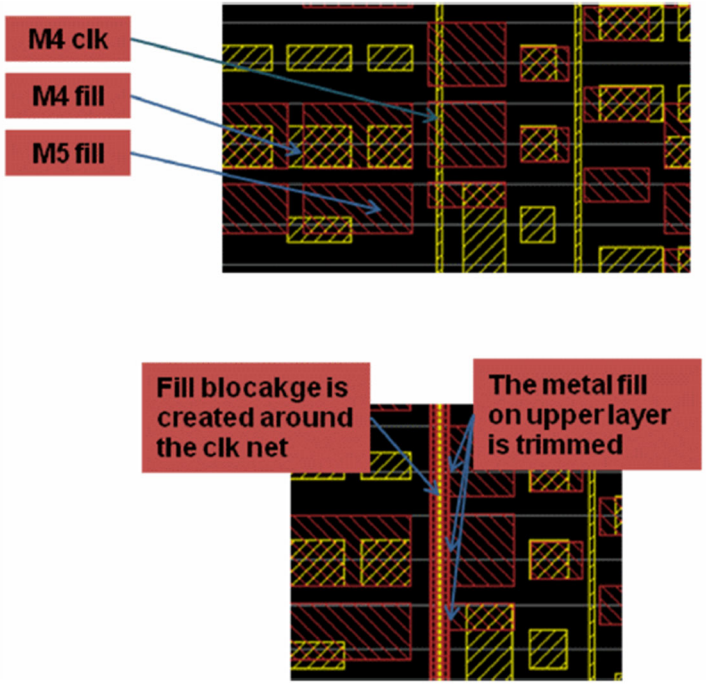
Parallel Edit Flow

The parallel editing flow can enable multiple users to make physical and logic ECO changes at the same time on different areas of a design. It can support a wide range of basic wire editing and ECO

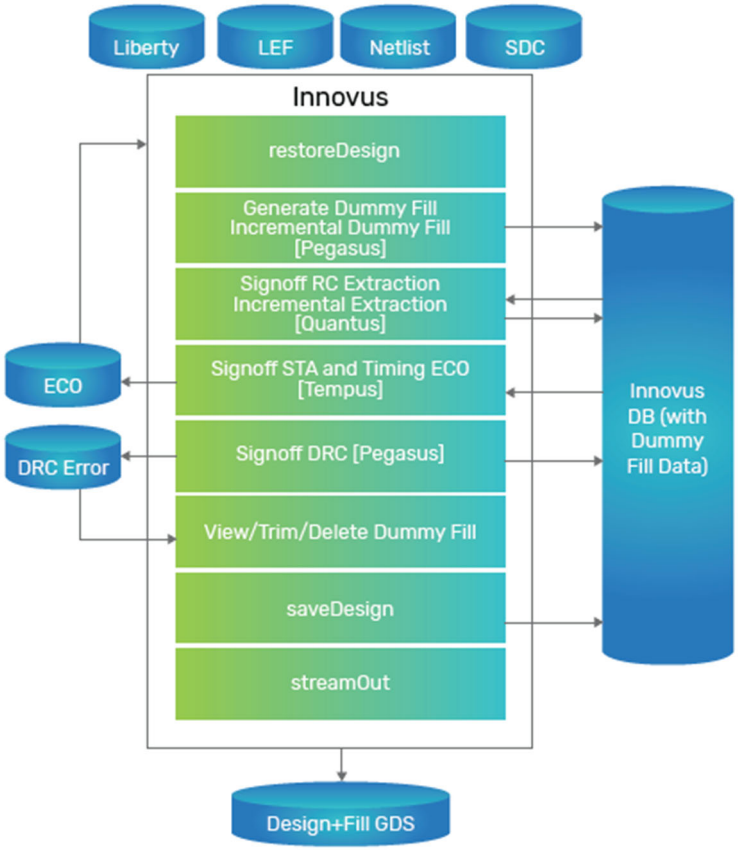
	operations, such as modifying or adding a wire or via or modifying logical connections.  See Innovus Manual at 1
10. The method of claim 9 further including: performing a stream-out process;	The Accused Products were made, produced, or processed from design data on which a stream-out process was performed.

	Use the commands listed below to insert sign-off metal fill in the design. This flow calls the Cadence Pegasus application or Cadence PVS application depending on which product you are using for sign-off metal-fill insertion. This is the recommended flow:
	If using Pegasus:
	`streamOut -mapFile gds_map -outputMacros -units unit`
	`run_pegasus_metal_fill -ruleFile PEGASUS_RULE_DECK -defMapFile -gdsFile -cell gds_top_cell`
	If using PVS:
	`streamOut -mapFile gds_map -outputMacros -units unit`
	`run_pvs_metal_fill -ruleFile PVS_RULE_DECK -defMapFile -gdsFile -cell gds_top_cell`
	See Innovus Manual at 124-125.

invoking a rule checker tool using a modified rule check to determine whether an output of the stream-out includes any dummy metal objects that intersect with design objects; and	The Accused Producs were made, produced, or processed from design data on which a rule check tool using a modified rule check was used to determine whether an output of the stream-out included any dummy metal objects intersecting other design objects.
	In Innovus, you can run the `timeDesign` command to check the timing. If the timing has degraded, you can trim the metal fill from critical nets for timing closure. Use the command below to trim the metal fill around critical nets:
	`setMetalFill -windowStep x_step y_step -windowSize x y`
	`trimMetalFillNearNet -slackThreshold $slack1 -spacing value -spacingAbove value -spacingBelow value -minTrimDensity value`
	See Innovus Manual at 124-125.

	 See Innovus Manual at 725.
deleting the dummy metal objects that intersect with design objects.	The Accused Products were made, produced, or processed from design data in which any such dummy metal objects that intersected design objects were deleted.  See Innovus Manual at 725.

CLAIM CHARTS
CADENCE AND USERS
U.S. Patent No. 7,260,803

11. The method of claim 10 wherein the modified rule check uses the dummy metal identifications to determine existence of intersections between dummy metal and the design objects.	The Accused Products were made, produced, or processed from design data where the modified rule check used the identification of dummy metal to determine whether it intersected other design objects.  *Figure 6: Hierarchical database flow* *https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf, page 4*

CLAIM CHARTS
CADENCE AND USERS
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Caveat: The notes and/or cited excerpts utilized herein are set forth for illustrative purposes only and are not meant to be limiting in any manner. For example, the notes and/or cited excerpts, may or may not be supplemented or substituted with different excerpt(s) of the relevant reference(s), as appropriate. Further, to the extent any error(s) and/or omission(s) exist herein, all rights are reserved to correct the same.

EXHIBIT D

BELL SEMICONDUCTOR LLC'S ANALYSIS OF INFRINGEMENT

U.S. Patent No. 7,149,989

Claims 1–2 & 4–6

Bell Semiconductor ("Bell Semic") provides evidence of infringement of exemplary claims 1–2 & 4–6 of U.S. Patent No. 7,149,989 ("the '989 patent") by the LCMX02-7000HC produced by Lattice Semiconductor, Inc. ("Lattice"). In support thereof, Bell Semic provides the following claim charts.

"Accused Products" as used herein refers to at least devices produced or sold by Lattice that are or include semiconductor integrated circuit devices that were made using a design tool, such as Synopsys IC Validator, to identify texted metal shorts between different signal sources (including, but not limited to, power and ground) using only a subset of physical design rules that are specific to texted metal shorts to validate the IC design as part of the manufacturing process flow, with the understanding that infringement has also taken place through the manufacture, importation, offer for sale, and/or sale of products including such Accused Products. These claim charts demonstrate infringement by comparing each element of the asserted claims to corresponding components, aspects, and/or features of the Accused Products. These claim charts are not intended to constitute an expert report on infringement. These claim charts include information provided by way of example, and not by way of limitation.

The analysis set forth below is based only upon information from available resources regarding the Accused Products, as Lattice has not yet provided any non-public information. An analysis of Synopsys's, Lattice's and/or other third parties' technical documentation may assist in fully identifying all infringing features and functionality. Accordingly, Bell Semic reserves the right to supplement this infringement analysis once such information is made available to Bell Semic. Furthermore, Bell Semic reserves the right to revise this infringement analysis, as appropriate, upon issuance of a court order construing any terms recited in the asserted claims.

Unless otherwise noted, Bell Semic contends that Lattice and customers of Lattice directly infringe under 35 U.S.C. § 271(a) the '989 patent by selling, offering to sell, making, using, and/or importing semiconductor products designed and/or produced at least in part by the Accused Products. Unless otherwise noted, Bell Semic further contends that the evidence below supports a finding of indirect infringement under 35 U.S.C. §§ 271(b) and/or (c), in conjunction with other evidence of liability under one or more of those subsections. Lattice and/or its customers make, use, sell, import, or offer for sale in the United States, or have done the same in the past, without authority, and/or induce or have induced others to make, use, sell, import, or offer for sale in the United States, without authority products, equipment, or services that infringe at least one or more of claims 1–2 & 4–6 of the '989 patent, including without limitation, the Accused Products or semiconductor products designed and/or produced at least in part using the Accused Products.

Unless otherwise noted, Bell Semic believes and contends that each element of each claim asserted herein is literally met through Lattice's provision of the Accused Products. However, to the extent that Lattice attempts to allege that any asserted claim element is not literally met, Bell Semic believes and contends that such elements are met under the doctrine of equivalents. More specifically, in its investigation and analysis of the Accused Products, Bell Semic did not identify any substantial differences between the elements of the patent claims and the corresponding features of the Accused Products, as set forth herein. In each instance, the identified feature of the Accused Products performs at least substantially the same function in substantially the same way to achieve substantially the same result as the corresponding claim element.

BELL SEMICONDUCTOR LLC'S ANALYSIS OF INFRINGEMENT

To the extent the chart of an asserted claim relies on evidence about certain specifically-identified Accused Products, Bell Semic asserts that, on information and belief, any similarly-functioning instrumentalities also infringes the charted claim. Bell Semic reserves the right to amend this infringement analysis based on other products made, used, sold, imported, or offered for sale by Lattice. Bell Semic also reserves the right to amend this infringement analysis by citing other claims of the '989 patent, not listed in the claim chart, that are infringed by the Accused Products. Bell Semic further reserves the right to amend this infringement analysis by adding, subtracting, or otherwise modifying content in the "Accused Products" column of each chart.

Lattice is a customer of at least Cadence, Synopsys, and Siemens, as demonstrated here: https://www.cadence.com/en_US/home/multimedia.html/content/dam/cadence-www/global/en_US/videos/tools/custom-_ic_analog_rf_design/maryam_shahbazi_lattice (Cadence); https://news.synopsys.com/index.php?s=20295&item=123188 (Synopsys); https://www.latticesemi.com/view_document?document_id=53646 (all).

Lattice is the producer and/or seller of the referenced above, as demonstrated by the following package images for the LCMX02-7000HC.

CLAIM CHARTS
SYNOPSYS IC VALIDATOR AND USERS
U.S. Patent No. 7,149,989

Claim 1	Accused Products
1. A method comprising steps of:	To the extent that the preamble is limiting, the Accused Products are made, produced, or processed by performing a method of physical verification. The Accused Products are made, produced, or processed by design tools from at least one of Cadence, Synopsys, and Siemens. For example, Lattice creates design data for the LCMX02-7000HC which was made, produced, or processed using one of the above-identified and described design tools, which include physical verification

CLAIM CHARTS
SYNOPSYS IC VALIDATOR AND USERS
U.S. Patent No. 7,149,989

(a) receiving as input a representation of an integrated circuit design;	The Accused Products are made, produced, or processed from design data by receiving a representation of an integrated circuit design as input. SYNOPSYS® Solutions Products Support Company Home ▼ / Silicon Engineering ▼ / Mask Synthesis ▼ / IC Validator WorkBench IC Validator WorkBench High Speed Layout Visualization **Overview** IC Validator WorkBench (ICVWB) is a powerful, high-performance, hierarchical layout visualization and analysis tool. It allows quick viewing and editing GDSII, OASIS®, and LEF/DEF layouts from small IP blocks to full-chip databases. In addition, ICVWB enables you to easily visualize and access the layout data being examined by the IC Validator (ICV) physical verification tool suite and review physical verification results. Building from the earlier IC WorkBench Edit/View Plus (ICWBEV) product, ICVWB refines the application for physical verification designers. **Benefits** • Quickly opens large GDSII, OASIS, and LEF/DEF files with low memory overhead. Additionally, cache files can drastically decrease the time for subsequent sessions • Opens Optimized OASIS files instantly • Provides easy debugging of the hierarchy and placement of cells and shapes • Quickly determines and displays shape connectivity interactively with cut layer capabilities • Provides improved support of the IC Validator (VUE) application to review and correct DRC and LVS errors • Provides various modes for merging layouts of mixed formats and DBUs • Compares layouts, cells, and generates difference reports/layouts • Defines TCAD simulation domains in hierarchical layouts for Sentaurus https://www.synopsys.com/silicon/mask-synthesis/icv-workbench.html

CLAIM CHARTS
SYNOPSYS IC VALIDATOR AND USERS
U.S. Patent No. 7,149,989

(b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design;	The Accused Products are made, produced, or processed from design data by also receiving, as input, a physical design rule deck that specifies rule checks to be performed on the IC design.

High-performance physical verification solution delivers up to 2X faster physical signoff

Overview

Synopsys' IC Validator physical verification is a comprehensive signoff solution improving productivity for customers at all process nodes from mature to advanced. The IC Validator tool offers the industry's best distributed processing scalability to over 2000 CPU cores. The tool's performance and scalability has enabled some of the industry's largest reticle limit chips with billions of transistors, same day design rule checking (DRC), layout versus schematic (LVS), and dummy fill turnaround time.

IC Validator physical verification is seamlessly integrated with Fusion Compiler™ RTL-to-GDSII solution and IC Compiler® II place and route system in the Fusion Design Platform. This integrated physical verification Fusion Technology™ accelerates design closure for manufacturing by enabling independent signoff-quality analysis and automatic repair within the implementation environment.

Benefits

- Industry leading physical verification performance enabled by distributed processing scalability past 2000 CPU cores
- Cloud-ready physical signoff, certified by TSMC
- Explorer technology for 5X faster DRC verification during SoC integration
- Elastic CPU management adds and removes CPUs dynamically
- Physical Verification Fusion within place and route enabling automatic DRC repair, timing aware FILL, and engineering change order (ECO) capabilities
- LVS-aware simulation based short-finder
- Integration with StarRC™ parasitic extraction, Custom Compiler™ full-custom design environment, and other third-party layout tools for increased designer productivity
- Live DRC for signoff quality on-the-fly DRC checking within full custom layout design tools

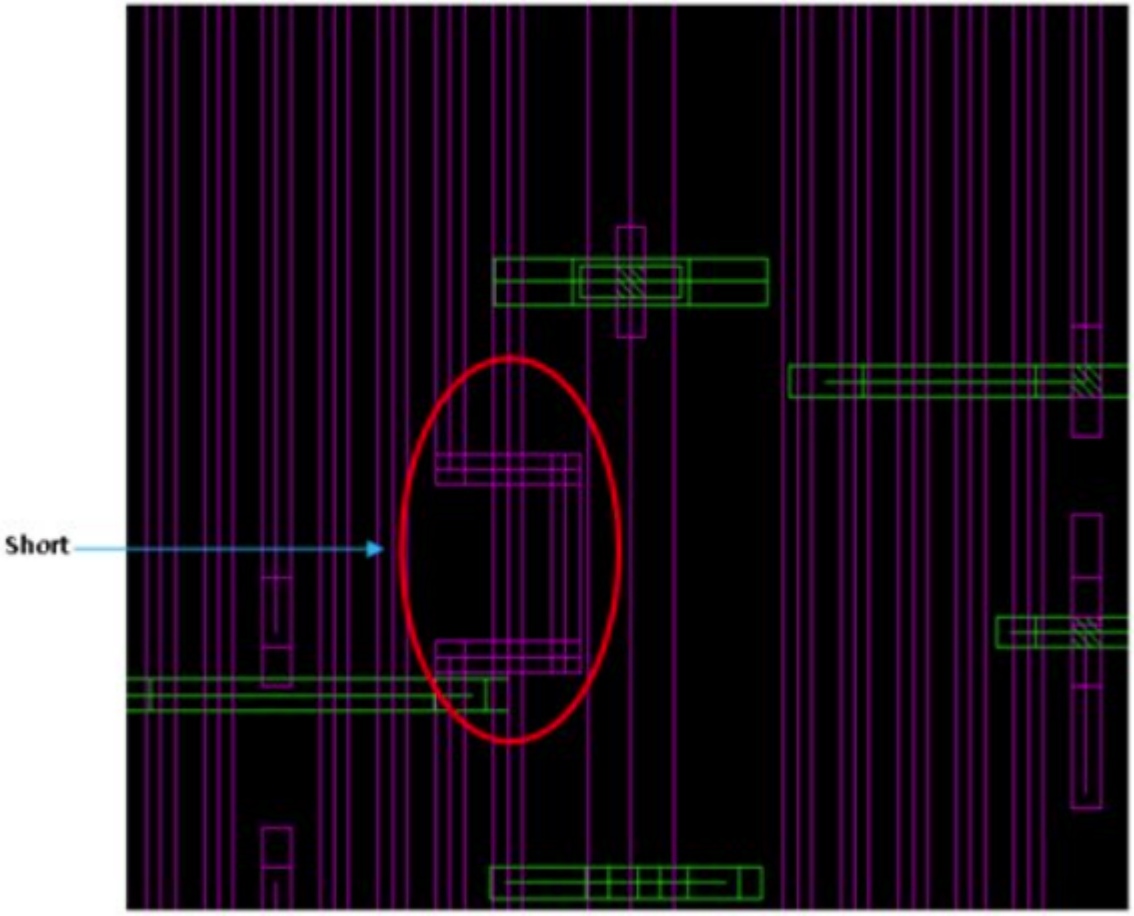
	Input files for LVS in ICV tool are listed below: • GDS (layout stream file): It is used by the LVS tool to generate layout netlist by extraction, which is used for LVS comparison. • Schematic netlist: It is used as a source netlist for LVS comparison. • Rule deck file: Rule deck file consists of required instructions and files to guide tool for performing LVS. This rule deck file also contains a layer definition, which is useful for extraction. • Equivalence file: It is used by the tool for ICV LVS comparison and it consists of cell pairs, which is made-up of one from the layout netlist and another from the schematic netlist. https://www.design-reuse.com/articles/47502/layout-versus-schematic-lvs-debug.html
(c) generating a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design; and	The Accused Products are made, produced, or processed from design data by generating, from the physical design rule deck, a specific rule deck that includes only physical design rules specific to texted metal short circuits between different signal sources (including but not limited to power and ground) in the IC design. IC Validator is specifically architected for In-Design physical verification, bringing the power of full signoff physical verification constraints into the design phase with IC Compiler II without imposing time-consuming stream-in and stream-out of layout data. Using In-Design physical verification, DRC and manufacturing issues are caught much earlier in the design cycle, reducing or eliminating late-stage surprises close to tapeout. With In-Design verification, specific layer, rules and selected areas of layout are targeted incrementally, providing a speed-up in overall **Incremental Layer-based, Rule-based and Area-based Verification** To accelerate physical verification design time, IC Validator and IC Compiler II integration enables intelligent incremental flows to eliminate unnecessary checking by restricting verification to the specific layer, rule or design area that needs validation. The tight integration provides a powerful tool dialog that allows the user to quickly select the rules, layers and region size for DRC checking, pattern matching, or adding metal fill. By automatically limiting the scope of the validation, more verification runs can be performed early in the design cycle, greatly reducing the number of full design verification runs, and shortening the time to results. (See Figure 3).

	Layout-vs-Schematic (LVS) IC Validator LVS is foundry certified and provides a comprehensive verification and debugging environment. The most important aspect of any LVS solution is the power and efficiency of its debug environment. IC Validator excels with its VUE and Shortfinder tools that quickly and easily identify errors, such as text-level shorts, for rapid repair and revalidation. VUE is a graphical environment to display and cross-probe between layout and schematics, together with a sophisticated error management system. IC Validator LVS device extraction supports leading edge technologies where device parameters are often affected by their proximity to neighboring devices through layout dependent effects (LDE). https://studylib.net/doc/18349317/ic-validator

Short: If layers in layout having different layout text on them are overlapping or intersecting, it will result in short in the design. Presence of the short in design will cause chip failure. It is important to find shorts present in design by running PnR shorts finding utility or by running LVS. The following example shows, how the short is reported by the tool after running the LVS.

```
Error summary:

          0 unmatched schematic device
          2 unmatched schematic nets
          0 unmatched layout device
          1 unmatched layout net



      Matched     Schematic    Layout          Instance types
                  unmatched    unmatched       [schematic, layout]
      ---------   ---------    ---------       -------------------
      ---------   ---------    ---------       -------------------
        9241555           0            0      Total instances

        4456857           2            1    * Total nets


DIAGNOSTIC: Shorted layout nets

    The following unmatched nets are highly suspected to indicate
    source of shorts in the layout netlist.

    Group 1 of 1:

        Schematic net : connections             Layout net : connections
        --------------------------              ------------------------
        y_pub_dfi2acx/n738 : 2                  N_11761399 : 5
        y_pub_dfi2acx/BUF_net_189972
```

When the short occurs in the design, the extractor will extract shorted nets as a single net, so there is only one layout corresponding net for two nets in the schematic, as mentioned in the report. N738 and BUF_net_189972 are shorted nets.

	Short can be resolved by properly rerouting the net.  https://www.design-reuse.com/articles/47502/layout-versus-schematic-lvs-debug.html
(d) performing a physical design validation on the integrated circuit	The Accused Products are made, produced, or processed from design data by performing a physical design validation from the specific rule deck to identify, on the IC design, any texted metal shorts between different signal sources (including but not limited to power and ground) in the IC design.

design from the specific rule deck to identify texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design.	**Layout-vs-Schematic (LVS)** IC Validator LVS is foundry certified and provides a comprehensive verification and debugging environment. The most important aspect of any LVS solution is the power and efficiency of its debug environment. IC Validator excels with its VUE and Shortfinder tools that quickly and easily identify errors, such as text-level shorts, for rapid repair and revalidation. VUE is a graphical environment to display and cross-probe between layout and schematics, together with a sophisticated error management system. IC Validator LVS device extraction supports leading edge technologies where device parameters are often affected by their proximity to neighboring devices through layout dependent effects (LDE). https://studylib.net/doc/18349317/ic-validator **Enhanced Productivity With In-Design Physical Verification** **Automatic DRC Repair (ADR)** IC Validator's seamless integration with IC Compiler II enables an innovative layout auto-correction interface, which identifies DRC violations, including DPT decomposition violations and initiates automatic repairs. The corrections are applied by IC Compiler II to alleviate DRC and DPT errors, and then validated within IC Validator. In-Design integration makes it possible to maintain hotspot-free designs throughout implementation, further eliminating iterations with downstream analysis tools. ADR's tight find-and repair loop enables rapid discovery and repair of errors, minimizing designer intervention and speeding time to tapeout. (See Figure 2). https://studylib.net/doc/18349317/ic-validator
2. The method of claim 1 further comprising performing step (d) prior to performing a physical design validation that includes a design rule that is not	The Accused Products are made, produced, or processed from design data that, after the physical design validation using the specific rule deck was performed, subsequently performs a physical design validation using at least one design rule that was not part of the specific rule deck, i.e., is not specific to identifying texted metal shorts.

included in the specific rule deck.	**Performing Layout-Versus-Schematic Checking** To perform layout-versus-schematic (LVS) checking, which checks for inconsistencies in the physical layout, use the `check_lvs` command. By default, the `check_lvs` command performs the following checks for all signal, clock, and PG nets: • Shorted nets A shorted net occurs when a net shapes from different nets touch or intersect. By default, the command ◦ Checks for shorts between net shapes in the top-level design, including shapes in top-level blockages To disable checking for shapes in top-level blockages, use the `-check_top_level_blockages false` option. ◦ Does not check for shorts between net shapes in the top-level design and net-shapes in child cells To enable this checking, use the `-check_child_cells true` option. To exclude certain types of child cells from checking, use the `-exclude_child_cell_types` option to specify one or more of the following cell types: `abstract`, `analog`, `black_box`, `corner`, `cover`, `diode`, `end_cap`, `fill`, `filler`, `flip_chip_driver`, `flip_chip_pad`, `lib_cell`, `macro`, `module`, `pad`, `pad_spacer`, `physical_only`, and `well_tap`. ◦ Does not check for shorts with zero-spacing blockages To enable this checking, use the `-check_zero_spacing_blockages true` option.

	Note: The `check_lvs` command supports only default routing blockages that apply to all net types and have a blockage group ID of 0. If the blockage applies only to specific net types or has a nonzero blockage group ID, the command ignores the blockage. In addition, the command ignores corridor routing blockages (which are created when you use the `-reserve_for_top_level_routing` option with the `create_routing_blockage` command) and boundary routing blockages (which are created when you use the `-boundary_internal` or `-boundary_external` options with the `create_routing_blockage` command).

- Open nets

  An open net occurs when the pins of a net are not connected by its net shapes.

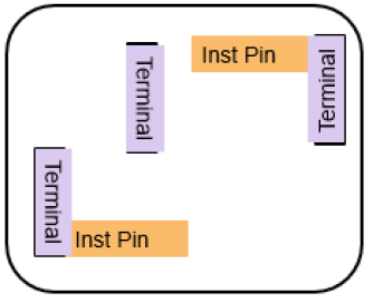
  By default, the command

  - Treats power and ground terminals as unconnected voltage sources

    To treat power and ground terminals as connected, use the `-treat_terminal_as_voltage_source true` option.

    For example, assume your block contains the layout shown in Figure 65. By default, the `check_lvs` command reports two opens for this layout. If you use the `-treat_terminal_as_voltage_source true` option, no opens are reported.

Figure 65 Layout With Power and Ground Terminals



  - Reports open nets as the bounding box of the open net and does not report floating pins

    To report detailed open locations, use the `-open_reporting detailed` option. Note that using this option might increase the runtime. To report the floating pins, use the `-report_floating_pins true` option.

- Floating net shapes

  A floating net shape occurs when a net shape is not physically connecting to a pin of its net.

To perform a subset of these checks, use the `-checks` option to specify one or more of the following checks: `short` (shorted nets), `open` (open nets), and `floating_routes` (floating net shapes). To check only specific nets, use the `-nets` option to specify the nets of interest.

By default, the `check_lvs` command reports a maximum of 20 violations for each type of error. To change this limit, use the `-max_errors` option. To report all violations, specify the maximum number of violations as zero (`-max_errors 0`). You can view the

	violations reported by the `check_lvs` command in the GUI by using the error browser. For information about using the error browser, see the *IC Compiler II Graphical User Interface User Guide*. To reduce the runtime required by the `check_lvs` command, enable multithreading by using the `set_host_options` command, as described in Enabling Multicore Processing.
4. The method of claim 1 further comprising a step of generating as output a report file that includes a location of each texted metal short circuit identified in step (d).	The Accused Products are made, produced, or processed from design data by generating, as an output, a report file that includes a location of each texted metal short identified in the specific rule check. *Key features include:* • Net tracing—ICVWB can trace touching shapes based on a user- defined connectivity list. This allows a quick check of opens/ shorts in a layout • Automated configurable HTML reporting of violation errors • Support automation with both Tcl and Python languages • Hierarchical folder representation of all objects including layouts, rulers, and other markups, such as SEM images • Browser-like forward and back view history • User and site-level customization: – Customizable hot keys for menus and commands – Customizable window and toolbar positions – Customizable menus and context-menus • Custom buttons to run user-created macros • Features to query layout databases instantly from a batch mode interface https://www.synopsys.com/content/dam/synopsys/silicon/datasheets/ic-validator-workbench-ds.pdf

Heatmap debugging with Explorer DRC allows designers to debug billions of DRC violations very quickly. Users are shown either in supported layout environments or directly in IC Validator - Visualization User Environment (VUE) heatmap details that enable designers to quickly pinpoint fundamental design flaws. DRC Heatmap provides designers with DRC error type, error density, error location, and error congestion.

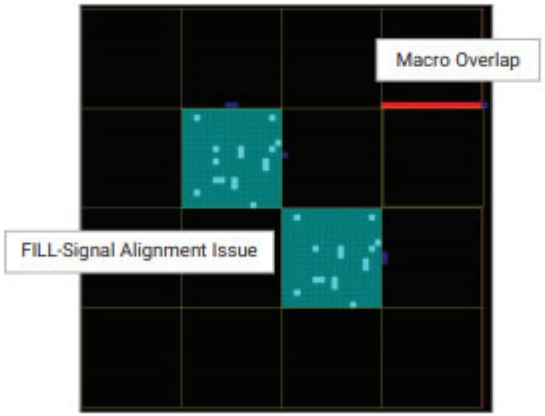


Figure 6: DRC heatmap highlighting error locations, density, and severity

https://www.synopsys.com/content/dam/synopsys/implementation&signoff/datasheets/ic-validator-ds.pdf at p. 4

CLAIM CHARTS
SYNOPSYS IC VALIDATOR AND USERS
U.S. Patent No. 7,149,989

5. The method of claim 1 wherein the representation of the integrated circuit design is a Generic Data Stream format file.	The Accused Products are made, produced, or processed from design data where the representation of the IC design is a GDSII file. SYNOPSYS® Solutions Products Support Company Home ▾ / Silicon Engineering ▾ / Mask Synthesis ▾ / IC Validator WorkBench IC Validator WorkBench High Speed Layout Visualization **Overview** IC Validator WorkBench (ICVWB) is a powerful, high-performance, hierarchical layout visualization and analysis tool. It allows quick viewing and editing GDSII, OASIS®, and LEF/DEF layouts from small IP blocks to full-chip databases. In addition, ICVWB enables you to easily visualize and access the layout data being examined by the IC Validator (ICV) physical verification tool suite and review physical verification results. Building from the earlier IC WorkBench Edit/View Plus (ICWBEV) product, ICVWB refines the application for physical verification designers. **Benefits** • Quickly opens large GDSII, OASIS, and LEF/DEF files with low memory overhead. Additionally, cache files can drastically decrease the time for subsequent sessions • Opens Optimized OASIS files instantly • Provides easy debugging of the hierarchy and placement of cells and shapes • Quickly determines and displays shape connectivity interactively with cut layer capabilities • Provides improved support of the IC Validator (VUE) application to review and correct DRC and LVS errors • Provides various modes for merging layouts of mixed formats and DBUs • Compares layouts, cells, and generates difference reports/layouts • Defines TCAD simulation domains in hierarchical layouts for Sentaurus

	https://www.synopsys.com/silicon/mask-synthesis/icv-workbench.html **Interfaces** • Inputs and Outputs – GDSII (including compressed GDSII) – LEF/DEF – OASIS (including compressed OASIS) – Optimized OASIS https://www.synopsys.com/content/dam/synopsys/silicon/datasheets/ic-validator-workbench-ds.pdf at 2

CLAIM CHARTS
SYNOPSYS IC VALIDATOR AND USERS
U.S. Patent No. 7,149,989

6. The method of claim 1 wherein the physical design validation is performed by one of a design rule check tool and a layout vs. schematic tool.	The Accused Products are made, produced, or processed from design data where the physical validation is performed by a DRC tool and/or an LVS tool. Synopsys' IC Validator is the proven high performance and comprehensive signoff physical verification solution. Trusted by leading semiconductor companies and used in hundreds of production designs, IC Validator offers a physical verification tool suite including DRC, LVS, Programmable Electrical Rule Checks (PERC), dummy fill, and Design For Manufacturing (DFM) capabilities. https://www.synopsys.com/content/dam/synopsys/implementation&signoff/datasheets/ic-validator-ds.pdf at p. 6

Caveat: The notes and/or cited excerpts utilized herein are set forth for illustrative purposes only and are not meant to be limiting in any manner. For example, the notes and/or cited excerpts, may or may not be supplemented or substituted with different excerpt(s) of the relevant reference(s), as appropriate. Further, to the extent any error(s) and/or omission(s) exist herein, all rights are reserved to correct the same.

EXHIBIT E

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON

BELL SEMICONDUCTOR, LLC, **Plaintiff,** **v.** **LATTICE SEMICONDUCTOR CORP.,** **Defendant.**	**Civil Action No.** **JURY TRIAL DEMANDED**

DECLARATION OF LLOYD F. LINDER

I make this declaration on behalf of Bell Semiconductor, LLC ("Bell Semic"). I understand that Bell Semic will offer my declaration as evidence in support of the above-captioned patent infringement lawsuit against Lattice Semiconductor Corp., ("Lattice").

1. My qualifications to testify concerning the relevant technology are set forth in my curriculum vitae, which is attached hereto as **Exhibit 1**.

2. I received my Bachelor of Science degree in Electrical Engineering (BSEE) from UCLA in 1985. I received my Master of Science degree in Electrical Engineering (MSEE), also from UCLA, in 1987. Thereafter, I continued studying Electrical Engineering at USC, where I received an Engineer's Degree in 1989 and researched and completed my thesis towards a doctoral degree in 2002. Following the completion of my BSEE, I began work at Hughes Aircraft, where I worked for 12 years.

3. When Hughes Aircraft was acquired by Raytheon in 1997, my title was "Senior Scientist." At Hughes Aircraft, I was the technical lead for RF/analog/mixed signal IC development and was a subject matter expert (SME) in integrated circuits, serving as a company-wide resource for review of integrated circuit designs and technical support of new business.

4. My next position was as an Engineering Fellow at Raytheon from 1997–2002, where I again was the technical lead for RF/analog/mixed signal IC development and was a subject matter expert (SME) in integrated circuits, serving as a company-wide resource for review of integrated circuit designs and technical support of new business.

5. In February 2002, I began a role as Director of Technology at TelASIC Communications, a company that I also founded. In this role, I served as the technical lead for the development of state-of-the-art ADC (analog-to-digital converter) and DAC (digital-to-analog converter) commercial products for the cellular base station market.

6. In 2006, I began working under "Lloyd Linder Consulting" as an Independent Integrated Circuit Design, Systems, Intellectual Property, and Wireless Consultant, a role that continues to this day. In this role, I have served as a consultant to over 100 companies in the commercial and military contractor semiconductor component market space and have served as an expert witness in semiconductor cases.

7. From 2008–2009, overlapping with my consulting, I took a position at Menara Networks for approximately 10 months, where I was involved with the development of an electronic dispersion compensation (EDC) IC and the development of quad transceiver for next-generation 10 Gb/s ASICs with integrated FEC / EFEC in CMOS.

8. I have received various honors over the course of my education and career. In 1985, I was named UCLA's most outstanding senior electrical engineering student, graduating Phi Beta Kappa and Summa Cum Laude. I am an IEEE Senior Member and served as a Judge for the San Fernando Valley Section Entrepreneurial Business Plan Competition in 2008. I am a named inventor on over 100 issued United States Patents (with several currently pending) and over 300 international patents, and have published over a dozen journal and conference papers focusing on

semiconductor design and layout. I am a two-time Hughes Aircraft Division Patent Award Winner, and was named by Hughes as a Masters Fellow, Engineers Fellow, and Doctoral Fellow.

9. I have reviewed U.S. Patent No. 7,260,803 to Lakshmanan et al. ("Lakshmanan '803"), which is also asserted in the Complaint, and its file history. I have also reviewed U.S. Patent No. 7,149,989 to Lakshmanan et al. ("Lakshmanan '989"), which is also asserted in the Complaint, and its file history. In addition, I have reviewed the claim charts accompanying the Amended Complaint supported by this Declaration.

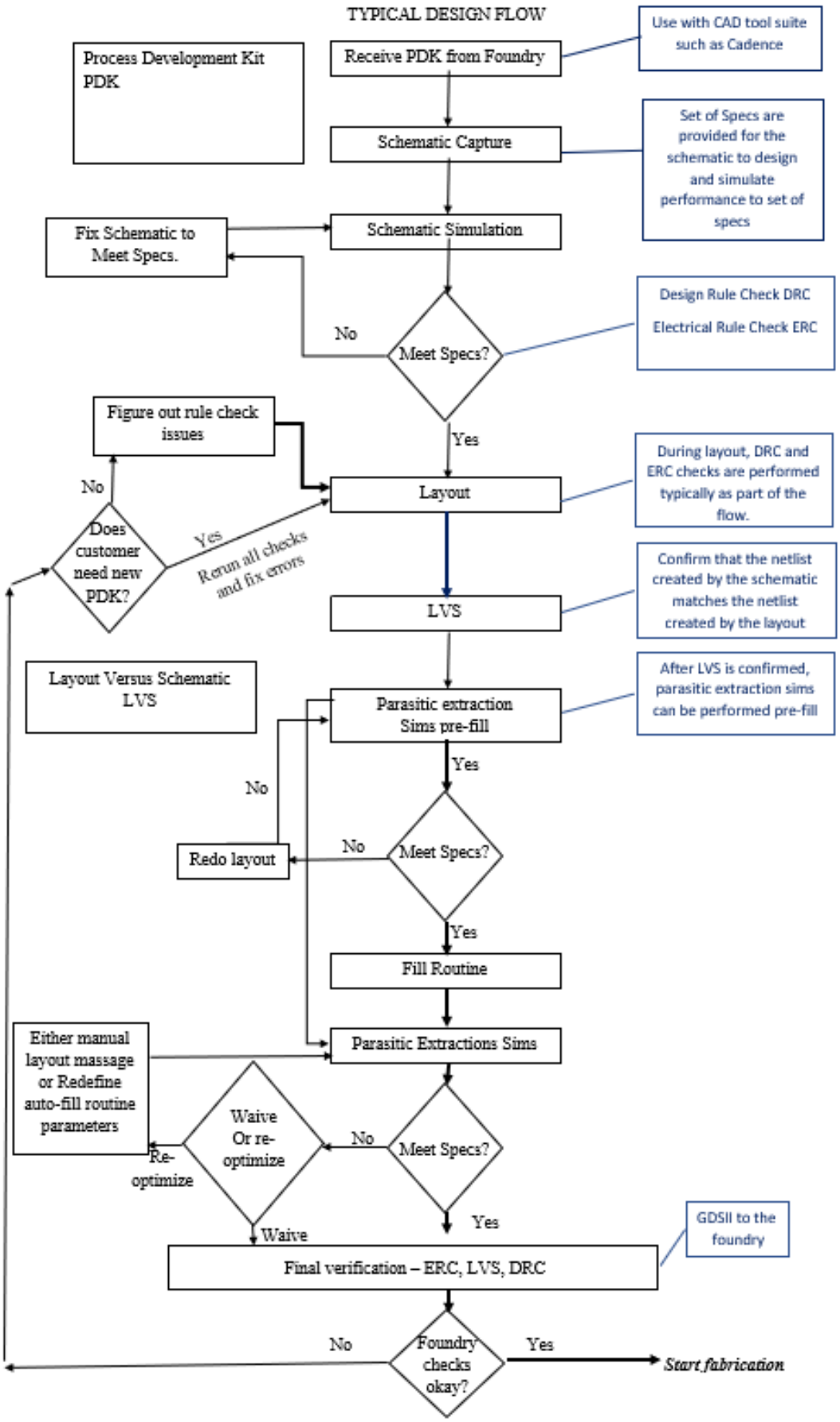
10. My college education over 15 years and 35 years of knowledge and experience in integrated circuit design, layout, and fabrication provides the necessary experience to support my stated conclusions set forth below.

Background on Integrated Circuit Manufacture, and Specifically the Layout Process Flow Segment of the Manufacturing Process

11. Semiconductor manufacture begins with the creation of a set of specialized electronic files that dictate the three-dimensional structure and features of the semiconductor device. These files, which are normally referred to as Graphic Design System (GDSII) files, are specifically formatted for and serve as necessary inputs for the devices that build the semiconductor device layer-by-layer according to the instructions contained in the GDSII files. Any changes to the structures in the GDSII files will result in changes to the structures in the fully fabricated device.[1] The manufacture process ends with the wafer containing the individual semiconductor devices is fully fabricated and sawed into individual semiconductor dies.

[1] The physical design validation of an integrated circuit design ensures that all spatial constraints are satisfied for the traces and devices formed in various layers of an integrated circuit die. The structures formed in the several layers of an integrated circuit die are represented in a GDSII format file that contains the chip topological information for creating the masks used in manufacturing the integrated circuit dies. This is also called the "layout," and which patents in this area typically call a "design". The GDSII format is an industry standard used by commercially available physical verification tools to represent physical design data. All structures affecting the performance of the circuit die must and will be present in the layout.

12. I have created the image below, which provides a simplified schematic showing, at a high level, a commonly-used integrated circuit design flow process that is representative of many (if not most) process flows in current use for creation of circuit layouts:


TYPICAL DESIGN FLOW
Process Development Kit PDK
Receive PDK from Foundry
Use with CAD tool suite such as Cadence
Schematic Capture
Set of Specs are provided for the schematic to design and simulate performance to set of specs
Fix Schematic to Meet Specs.
Schematic Simulation
No
Meet Specs?
Design Rule Check DRC
Electrical Rule Check ERC
Yes
Figure out rule check issues
No
Does customer need new PDK?
Yes
Rerun all checks and fix errors
Layout
During layout, DRC and ERC checks are performed typically as part of the flow.
LVS
Confirm that the netlist created by the schematic matches the netlist created by the layout
Layout Versus Schematic LVS
Parasitic extraction Sims pre-fill
After LVS is confirmed, parasitic extraction sims can be performed pre-fill
Yes
No
Redo layout
No
Meet Specs?
Yes
Fill Routine
Either manual layout massage or Redefine auto-fill routine parameters
Parasitic Extractions Sims
Waive Or re-optimize
No
Meet Specs?
Re-optimize
Yes
Waive
GDSII to the foundry
Final verification – ERC, LVS, DRC
No
Foundry checks okay?
Yes
Start fabrication

13. The integrated circuit design flow process includes a design engineer, using design tools, to create a design for an integrated circuit to be processed.

14. Design tools from vendors such as Cadence, Synopsys, or MentorGraphics (now Siemens) will then be used to design, simulate, and lay out integrated circuits. The typical design tool suite includes[2] schematic capture, simulation, layout, verification (layout versus schematic (LVS) and design rule check (DRC)), and fill generation routines. These fill routines can be automated or manual, and can be provided by the design tool company in whole or in part.

15. To be sure, the precise capabilities of each design tool available to a particular design engineer may differ within a company (based on what options in the design suite are available to a particular user or on a particular device), and between different design tool suites. However, based on my experience, at a high level, the design tools used by design engineers in the semiconductor industry, all operate in substantially similar fashion for schematic capture, simulation, layout, verification, design rule check, and fill-generation. In particular, based on my experience as a consultant, the design tools commonly used in the industry to place dummy fill operate in substantially similar fashion in providing incremental and timing-aware fill generation for integrated circuit layouts. This also applies to the design tools commonly used to identify texted metal shorts, which likewise operate in substantially similar fashion.

16. In the design process, the schematic is created first. The layout design tool is used to place and route all of the active (i.e., transistors) and passive components (i.e., resistors, capacitors, and inductors), and the interconnections between devices (represented as wires) in the schematic. It represents the circuit function that is to be physically implemented in the silicon. The schematic is created and simulated, using the CAD tools, to confirm that the circuit functions to a desired specification.

[2] Sometimes electrical rule check (ERC) is also included in design tool suite capabilities.

17. Once that performance specification is confirmed from the schematic simulation, the layout of the circuit is performed to physically place each of the individual elements necessary to implement the circuit functions set forth in the schematic in the GDSII file. During layout, layout rules for active and passive devices must be followed, but conformance is not checked until a DRC is run (typically at least as part of the final verification, though it can be run at any point or points in the layout process). Instead of only checking conformance at the end, it is possible to use a subset of the DRC deck to check for texted metal shorts in the layout of the schematic at an early or incremental point in the process flow. This allows the top-level routing to be completed in parallel with the block-level schematic and layout. Doing this will help accelerate the design timeline and avoid any delays occasioned by only finding such rule violations at the end of the design process flow for that particular schematic.

18. Once the layout is completed, it is compared to the schematic of the circuit using layout-versus-schematic (LVS) tool to confirm that the two are identical. From the schematic, a netlist (a list of devices and the associated nodes) is generated. From the netlist, the schematic could be re-generated by hand by drawing the devices and connecting the device nodes. From the layout of devices and associated nodes, a corresponding netlist is generated, from which a similar schematic could be generated by hand by drawing the devices and connecting the device nodes from the layout netlist. Then the schematic netlist is compared to the layout netlist using the LVS tool. The LVS tool compares the schematic netlist to the layout netlist to see if they match—i.e., whether they contain the same devices connected in the same fashion. If they do not match, the discrepancies between the two must be found and corrected, and LVS re-run. Any violations of layout rules must be corrected and DRC re-run for the layout.

19. After passing LVS, the process of performing parasitic extraction simulations before the fill has been placed (pre-fill) can be performed on an extracted netlist created from the

layout. If parasitic simulations are performed prior to the fill placement, the designer can get an idea of the impact on circuit performance from the basic layout parasitics pre-fill. From the layout, a netlist is extracted that includes any of parasitic resistance (R), parasitic inductance (L), parasitic capacitance (C), or any combination of the three. Additionally, the parasitic extraction can include what is termed "coupled" capacitance (parasitic capacitance between metal lines) as well as the parasitic capacitance to the substrate. The extracted netlist, with the selected added parasitics, can be used to run simulations on the baseline layout to determine if there is any performance degradation due to the baseline layout routing.

20. The simulated performance of the layout, which includes the parasitics, needs to be as close as possible to the specification that was already satisfied by the schematic. That is why parasitic extraction is performed, and why it is iterated pre-fill and post-fill. So if there is performance degradation due to the baseline layout, the layout is redone until its performance is at acceptable parameters. Ideally, the extracted simulation results match the schematic simulation results, which means that the layout parasitics had no impact on the circuit performance.

21. Once the layout passes pre-fill, the design tool is used to insert dummy fill at appropriate locations in the layout that do not contain devices or other features. As is well-known in the industry, the purpose of adding dummy fill is to achieve a higher and more uniform density of interconnect across the surface of each layer of the chip, to improve the outcomes of the chemical-mechanical polishing/planarization (CMP) step during fabrication. If individual pieces of fill are below a certain minimum size, they may not planarize properly during CMP, which will result in the dielectric material deposited on top of those too-small features not planarizing properly,[3] which will produce in dishing in the dielectric and result in a non-planarized surface.

[3] The effect on the dielectric from underlying interconnect is known as the deposition bias. A "positive bias" or "positive deposition" bias is when the width of the protrusion in the dielectric is

Thus, in practice, the fill pieces added cannot be below a certain minimum feature size. Adding dummy fill at or exceeding the minimum feature size and to achieve a higher and more uniform density of interconnect lowers the likelihood of defects caused by the CMP process step and thus improves the yield of modern integrated circuits.

22. Once all components of the integrated circuit design have been placed and routed, a physical design validation is typically performed at the very end of the design cycle. This ensures that all spatial constraints are satisfied for the traces and devices in each layer of an IC, that the die complies to all process rules, and that any additional required steps specific to manufacturability for a selected technology have been performed (e.g., metal utilization).

23. As the pre-fill step confirms that parasitics of the baseline layout, pre-fill, do not degrade the performance of the integrated circuit, it is desirable that the fill likewise does not degrade performance. However, depending on its placement, dummy fill can also degrade the performance of the integrated circuit, which is undesirable. To minimize this, the design suites include timing-aware fill tools that minimize, if not prevent, any degradation to circuit performance caused by dummy fill insertion. These tools also incorporate details on fill density, size, and position necessary to meet the requirements of the fabrication process and allow the user to specify the minimum and maximum dimensions of the dummy fill.

24. Based on my experience, use of such timing-aware fill tools has become standard practice in designing modern integrated circuits. In fact, modern integrated circuit designs are required to have fill included as part of the database submitted for fabrication. Due to the

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greater than that of the underlying active interconnect feature. Conversely, a "negative bias" or "negative deposition bias" is when the width of the protrusion in the dielectric is less than that of the underlying active interconnect feature. In either case, large density variations of the active interconnect features will typically result in interconnect that is insufficiently planarized during CMP, and thus, overpolishing of the dielectric that produces significant dishing. This is particularly detrimental in fabrication of multi-layer chips and packages.

complicated nature of these designs, such as SoCs and highly integrated circuits with many layers, the fill process cannot be manual at least for the practical reason of there being far too many locations and options for fill position and dimension to designate by hand for fill insertion. Moreover, the chip has many critical nets (i.e., important timing-sensitive signal lines), so there is a need for the fill-placement to be aware of any impact on the timing and resulting performance impact of the circuit. Timing-aware fill tools are used to attempt to simultaneously meet interconnect density (including feature size) and timing closure requirements, but they are not guaranteed to do so 100% of the time. When this occurs, a decision must be made to compromise performance at the expense of yield, or vice-versa.

25. Once the fill routine is completed, the fill checks are done, and final verification is performed again (LVS, DRC). The fill checks are performed based on percentage requirement on a specified area in the layout.

26. Once the layout database has been verified, it is sent for fabrication in the form of a GDSII database, which is the industry standard format for delivery of the chip database. As previously mentioned, fill is required to be included as part of the GDSII database.

27. The design resource is provided with a process design kit (PDK), which includes all of the information necessary to capture a schematic, run a simulation, do a layout, and perform all of the checks on the layout to make sure that the final GDSII is in an acceptable form to be ready for fabrication. It is the design resource / customer's responsibility to make sure that the designed chip meets all of the expected requirements for fabrication and bears the risk of failing to follow any steps in the design flow. For example, if the circuit does not work, that is the customer's responsibility. If the layout does not match the schematic, that is the customer's responsibility. The GDSII does have to meet all of the DRCs in order to be fabricated.

28. In order to develop an integrated chip product, tools are needed to develop the schematic, the layout, verification of the layout, and the final GDSII database for fabrication. Many companies use different tools (from different vendors) to accomplish this process either typically due to cost or preference of internal proprietary tools. Regardless of the process and specific tools that are used, the GDSII database goes through an internal DRC after it is received and before fabrication of the integrated chip:

a. The design resource receives a PDK that contains all of the information is included to create a GDS database to release for fabrication. This includes circuit symbols for the creation of the schematic, models for the circuit symbols to run simulation, and associated layout devices that have been created with all of the process layers needed.

b. Additionally, there are what are known as "rule decks" in the PDK that allow for LVS and DRC. A rule deck is typically a file that specifies all of the available rules (for example, minimum feature sizes such as line width and minimum fill dimensions), the layers to process on each rule, and the parameters of each rule. The LVS deck compares the schematic to the layout, and the DRC deck covers all of the design rules for placing and routing devices. For LVS, a netlist of the layout is created. This netlist is compared to a netlist created for the schematic. The LVS tool compares the two to determine if they match or not.

c. Additionally, there is a parasitic extraction deck that extracts all of the parasitics of the layout that is used to run simulations to close timing or to confirm that the layout still meets all of the chip requirements.

d. There can also be an electrical rule check (ERC) deck as well, depending on the fabrication involved.

29. If the DRC rules at pre-fabrication do not match those at the design resource, it is possible that there will be DRC errors. This could be due to a number of reasons, including the DRC in the provided process design kit (PDK) is not up to date, and so the PDK will be updated with the updated DRC and the design resource will have to redo everything and fix the DRC errors, providing a new GDSII database before fabrication can begin. These DRC checks at pre-fabrication will include checks for the fill on all layers to confirm that the fill requirement is met, on a granular level, for all tiles at the chip boundary level.

The Semiconductor Manufacturing Process includes a Textual Representation of the Integrated Circuit

30. Typically, every active element or device within a circuit[4] is connected between two (or more) other sources or components, such as power, ground, a clock, a signal, and/or another active element or device. During the design process, signal source locations are typically associated with and labeled by specific names. For example, supply voltage is typically labeled within the design database as "VDD" and ground as "VSS," with all signal sources typically receiving some name or textual label at some point in the design process in order to, among other things, assist with building the schematic and extracting a netlist.

31. The connections of each a device's particular inputs and outputs to other sources and/or devices, which indicates by the text label the particular signal sources for devices connected to such sources, are stored by the design tool as properties for each device. This enables a representation of a circuit design as defined by the map of its connections between devices and signals alone before determination of, and without needing to specify, any of the physical or topological details of their arrangement, such as their dimensions or location.

[4] This typically excludes dummy fill, which is usually (but not always) free-floating and not connected to any signal source or to ground.

32. As discussed above, part of the semiconductor circuit design process is physical validation (i.e., ensuring that all spatial constraints are satisfied with respect to all layers of the integrated circuit die). Examples of the kind of design rules that are included in a physical validation include checking for cells not connected to power or ground; power and ground paths being closer to each other than allowed; insufficient via/contact spacing or size; incorrect power bus slots; metal layer width, spacing, and hole dimensions; and I/O and core regions of the chip exceeding maximum limits. Typical physical validation tools include design rule check (DRC) and layout vs. schematic (LVS) tools.

33. As is well known, a "short" or "short circuit" is when a piece of metal or wire directly connects two (or more) different signal or power sources. But this is not limited to a physical, tangible circuit. Rather, a short can also exist in the textual representation of the circuit design such as, for example, when the textual representation of the circuit design indicates a wire connecting supply voltage (VDD) and ground (VSS). A piece of metal in the chip design that connects two different signal and/or power sources results in what is called a "texted" metal short or "texted" metal short circuit.

34. Identification of texted metal shorts in the physical design of the circuit (i.e., post layout and routing) is a universal part of validating the circuit design, and typically occurred for the first time at a late stage in the design cycle, most often at LVS and/or DRC. The use of design tools, which typically create a substantial amount of routing information automatically while also enabling manual entry and modification of routing, greatly increases the likelihood of design rule violations, such as texted metal shorts.

35. By that stage, however, a large amount of computer time and design time has typically been invested. Design rule violations discovered in foundational portions of the circuit

design, such as the power map, often require unacceptable turnaround time and costly schedule delays to address at the end of the design process.

36. While it is advantageous to identify texted metal shorts early in the design flow, doing so with a complete set of process design rules for a specific technology would require a substantial amount of computer processing time, which would in turn severely impact the time-to-market. In addition, a complete physical design validation at such an early stage would flag a large number of false positive design rule violations, making it difficult to sort out the design errors that actually need to be corrected before the circuit design is completed from those that just reflect the non-final nature of the design-in-progress.

37. Prior to Lakshmanan '989, the traditional approach for physical design validation was to perform a physical design validation at the end of the design cycle, after all components of the integrated circuit design (including dummy fill) have been placed and routed. Such performance of physical design validation at the end of the design flow meant that when a design fault is detected this late in the process, it may require substantial redesign—potentially requiring the design process to start over entirely, depending on the nature and severity of the design fault, and at least with significant delay to bringing the product to market.

38. Efforts to resolve the disadvantages associated with very late detection of design faults only offered the tradeoff of also using the physical validation tool—with the full set of process design rules that would apply during the end-of-design-flow verification—during the early stages of the design process. However, this approach yielded two disadvantages. First, it was slow: the computer processing time required severely impacted the turnaround time for the final product. Second, performing such a physical validation to detect errors early in the process yielded a large number of false positives resulting from the design being *incomplete* rather than *defective*.

39. The layers of semiconductor devices—and the interconnects and components formed within them—have gotten much smaller over time, increasing the performance of these devices dramatically. As the size of components and interconnects used in the manufacturing process have decreased, and the size of wavers have increased, the design requirements have become more difficult to meet.

Explanation of Lakshmanan '989

40. In place of these methodologies, Lakshmanan '989 teaches a novel process flow and software tool for physical validation that enables identification of texted metal short circuits early in the design cycle and without undue demands on computer processing time or incorrect identification of errors from a circuit design that remains in progress. At the time of the invention of Lakshmanan '989, this was a new and different process flow compared to the prior art that avoided costly schedule delays and unacceptable turnaround time that were likely to result from the use of traditional methods of physical validation that relied on end-of-design-flow verification or application of the full set of process design rules. The novel method and process flow of Lakshmanan '989 produces improvements in the IC design process flow as well as reducing the design time required to complete a design. This permits the top-level routing to be architected in an industry-standard manner to improve the overall performance of the resultant device.

41. Lakshmanan '989 explains that to solve this problem, early physical design validation is performed on a specific subset of the universe of design rules. Lakshmanan '989 exploits the capabilities of the LVS tool to detect metal short circuits by reducing the standard universe of rules to include only those needed to detect texted metal short circuits, then performing the physical design validation step on the reduced set of rules early in the integrated circuit design cycle.

42. Lakshmanan ’989 explains that the power map is created early in the design process and remains consistent throughout the design cycle. It teaches that defects in the power map such as texted metal short circuits can be detected well before the design cycle is complete. Moreover, any such defects are likely to create errors with other components, necessitating multiple design changes in response to such a defect.

43. Lakshmanan ’989 explains that the reduced number of design rules used in the early-stage physical validation reduces the time required to perform the physical design validation relative to performing a complete physical design validation on an incomplete (or complete) circuit design. Further, by detecting earlier in the process, those errors may be corrected before investing the time required to generate and validate the entire integrated circuit design (Lakshmanan ’989 at 5:6–13).

44. I have also reviewed the prosecution history of Lakshmanan ’989. The patent claims were allowed over prior art following an amendment to the independent claims to require that the subset of design rules search for short circuits between different signal sources in addition to power and ground. The examiner thus recognized that the prior art, whether alone or in combination, did not disclose or suggest creating a subset of design rules that searched for short circuits between different signal sources in addition to power and ground. Based on my experience in semiconductor layout and design, as set forth above, I agree with this characterization of the contents of the prior art.

45. Prior to Lakshmanan ’989, I am not aware of any product or method of physical design validation that checked the physical design in the early stages of the design flow process only from the perspective of metal shorts or a limited subset of process design rules. As far as I am aware, and based on my experience, to the extent that any such tools were able to validate the physical design in the early stages of the design flow process, such validation was not limited to

any particular subset of the physical design rules, let alone only those necessary to detect texted metal shorts.

46. Moreover, based on my experience in semiconductor layout and design, it was not well-understood, routine, or conventional at the time of Lakshmanan '989 to conduct physical design validation on a subset of the physical design rules for the purpose of identifying texted metal shorts or other issues identifiable from a power map. As Lakshmanan '989 recognized, the conventional methodology at the time was to perform an end-of-design-cycle physical design validation on the full deck of physical design rules. In circumstances where a design validation was performed early in the design cycle, it was likewise conventional to perform the validation using the full set of physical design rules.

47. Based on my experience in semiconductor layout and design, I agree that the claimed inventions of Lakshmanan '989 were not, to the best of my knowledge, well-understood routine, or conventional activity at the time of Lakshmanan '989. This is true not only in an ordered combination of the elements, but also as an individual claim element. In particular, generating a specific rule deck containing a subset of the physical design rule deck including only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground and performing a physical design validation to identify violations of that subset, as recited in elements (c) and (d) of claims 1 and 7, was not, to the best of my knowledge, well-understood, routine, or conventional activity at the time of Lakshmanan '989, either on its own or in an ordered combination with the other elements of the independent claims and the dependent claims that include those elements.

Dummy Fill is Required in Design and Layout of Multi-Layer Semiconductor Chips

48. To the best of my knowledge, adding dummy fill is a requirement for every integrated circuit using the latest technology nodes. Certain older nodes still in fabrication

(>350nm) may not require fill, but I believe that even some of these older technology nodes have incorporated fill requirement to enhance yield.

49. As mentioned above, it is required that the GDS database include fill within the database submitted for fabrication. In particular, most fabrication processes used in modern semiconductor chip designs require both a minimum density and a minimum feature size for the interconnects (i.e., pieces of metal or semiconductor) placed on each layer of a multi-layer chip design. This is the case both for the layer as a whole and for individual subunits of each layer, and is fundamental to the creation of consistent fabrication of multi-layer devices with minimal defects.

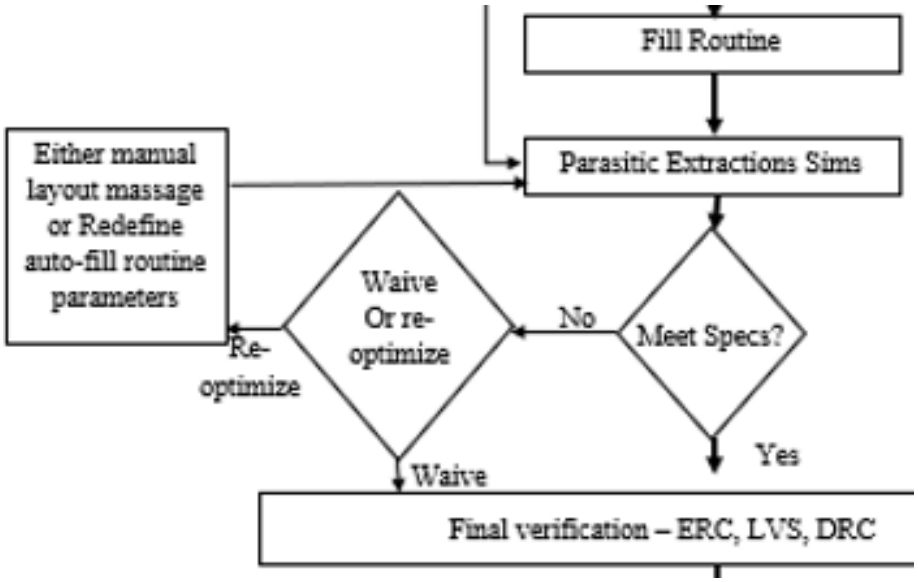
50. Fabrication processes typically partition each layer of the chip design into rectangular regions called tiles, each of which must also meet a minimum density requirement. For any given region of the chip, the interconnect density is the area of all of the interconnect in that region divided by the total area of that region.

51. Sufficient interconnect density and substantial uniformity of interconnect are required for the chemical mechanical polishing (CMP) portion of the chip fabrication process. CMP is crucial to achieve planarity, which allows for multi-layer chip designs and high yield of functional devices. Insufficient interconnect density and/or insufficient uniformity of interconnect between various regions will increase the likelihood of defects during the chip manufacturing process, which will resultantly degrade the yield.

52. Once the functional features of the chip design (such as power lines, signal nets, vias, and the like) have been laid out as needed in the first instance, there will usually be substantial portions of the chip design that have insufficient interconnect density to permit CMP without incurring substantial likelihood of defects.

53. To increase the interconnect density of the layer as a whole, and of regions within each layer, numerous individual pieces of interconnect are inserted into available space in low-

density regions of the chip until the minimum interconnect density specified for the particular fabrication process is achieved for each tile. Because these pieces of interconnect are not intended to carry signal or power, but instead are added to provide structural stability to the chip architecture, they are generally known as "dummy fill."



54. Placement of dummy fill is typically performed by a dummy fill software tool, and is one of the last steps in the chip design flow, with its extent and placement typically occurring after routing and timing closure. The time it takes the dummy fill tool to complete its task depends on the complexity of the circuit layout, and correspondingly, the size of the design database. If dummy fill must be run (or re-run) for the entire layer, even small changes in layout can result in significant delays while the dummy fill tool runs each time the layout changes.

55. In operation, the dummy fill software tool typically partitions each layer of the design into rectangles called tiles, which it examines in each layer of the design. If the interconnect density in each tile does not meet (or exceed) the specified minimum interconnect density for the fabrication process, the dummy fill tool inserts dummy fill into free regions of that tile where no interconnect is present.

56. The dummy fill software tool typically allows the user to specify the shape (rectangular or square) and dimensions (maximum and minimum) for the dummy fill to be inserted into open areas of the layout. In addition or alternatively, fill dimensions, shape, and position can be (and typically are) supplied separately from the fabricator in a format such as a LEF file, which the dummy fill software tool then incorporates and uses to place dummy fill in open areas of the layout

57. For large integrated circuits, commonly called system-on-a-chip (SoC) with either large analog content and small digital content ("big A, little D") or large digital content and small analog content ("big D, little A"), it is not practical to manually add dummy fill, so automated fill routines are almost always used. Because there are so many critical signals in a large SoC, the process cannot be done manually due to the time it would require. Thus, the design timelines and practical realities require that the automated fill routines are used instead.

58. However, placing the dummy fill that is too large in size, too extensive, and/or too close to signal nets increases capacitance between the signal wires and the dummy fill in the physical device if fabricated without taking additional measures. That increase in capacitance in the fabricated physical device would in turn slow the transmission speed of signals and degrades the overall performance of the integrated circuit. This effect is undesirable and is known as "parasitic capacitance."

59. The added parasitic capacitance will degrade parameters, such as operating frequency and rise/fall time, for a critical clock or signal, and this must be avoided in order for the circuitry to work properly.

60. The parasitic capacitance is inversely proportional to the distance between the dummy fill and the signal wire. Thus, parasitic capacitance from dummy fill will be minimized if the dummy fill is placed far from signal nets.

61. Conversely, the parasitic capacitance from dummy fill on signal lines is directly proportional to the lateral dimension of the dummy fill (i.e., the extent to which the dummy fill runs parallel to the signal line). Thus, parasitic capacitance from dummy fill will be minimized if the same area of dummy fill is placed in many narrow pieces oriented perpendicular to the signal line (which also places more of the dummy fill at a greater distance from the signal line) rather than one long strip oriented parallel to the signal line.

62. The result of using a constant (often very small) lateral fill dimension was that substantial dishing would occur during CMP due to variation in interconnect density in the lateral dimension, resulting in an unacceptably high rate of chip defects and unacceptably low yield. Since fixing fill dimension manually was a time-consuming process, with limited time available, the result would typically be that the interconnect density requirements could not be met, and a waiver would be requested before fabrication would begin, with any resulting yield degradation being accepted by the customer.

63. By minimizing the lateral dimension of dummy fill, its parasitic capacitance can be bounded below a particular value and its effect on circuit timing can be minimized. However, hard-coding a small dimension will create discontinuities in the dielectric that will only be exacerbated (rather than resolved) by CMP, thus limiting chip yield.

64. In other words, when using a one-size hard-coded dummy fill solution, the higher the required yield, the more constant the overall interconnect density must be within various portions of the layer, with increasingly higher parasitic capacitance and negative impact on timing and circuit performance because that interconnect will comprise dummy fill having a substantial lateral dimension paralleling signal lines. Conversely, the more sensitive the timing requirements for the circuit, the less the parasitic capacitance can be tolerated near crucial signal nets and the lower the lateral dimension of the dummy fill can be for tiles that include such signal nets, resulting

in a lower overall interconnect density, and greater variation across the layer, resulting in defects and lower yield. This tradeoff between performance and yield is further complicated when multiple metal layers are involved, which can be ten or even more.

65. The traditional solution to minimizing the parasitic capacitance effect of dummy fill near signal nets was the "simplistic approach" of hardcoding a large "stay-away" distance from crucial signal nets, essentially establishing a defined "exclusion zone" (or "keep-out area"), essentially a "moat" around those circuit elements that would be designated categorically unsuitable to receive dummy fill when the dummy fill software tool was utilized and the device fabricated. The distance was typically derived empirically for each design by studying the effect on timing from dummy fill inserted at various distances from clock nets in sample designs and was then manually hardcoded in the dummy fill libraries for each type of process technology.

66. The result of using these keep-out zones was that potentially the chip would have poor yield. Since this was a manual time-consuming process, with limited time available, the result would typically be that the fill requirements could possibly not be met, and a waiver would be requested before fabrication would begin, with any resulting yield degradation being accepted by the customer.

67. By excluding dummy fill from being placed within a certain distance of crucial signal nets, its parasitic capacitance can be bounded below a particular value and its effect on circuit timing can be minimized. However, hard-coding a large "stay-away" distance between dummy fill and signal nets, creating a region in which dummy fill cannot be placed, will also reduce the space available for dummy fill insertion and thus limit the overall interconnect density that can be achieved.

68. In other words, the higher the required interconnect density, the closer it must be placed to signal nets, with increasingly higher parasitic capacitance and negative impact on timing

and circuit performance. Conversely, the more sensitive the timing requirements for the circuit, the less the parasitic capacitance can be tolerated near crucial signal nets and the lower the interconnect density can be for tiles that include such signal nets. This tradeoff is further complicated when multiple metal layers are involved, which can be ten or even more.

69. It may be that the timing requirements cannot be met without a revision to the fill placement, density. and sizing, and re-extraction of the layout parasitics to determine if the timing requirements are met. If they are not, then a decision would have to be made to continue the iteration process or apply for a waiver and bear the risk of lower yield, or accept decreased performance.

70. Balancing these tradeoffs started to become particularly problematic by the early 2000s, as new processing technologies with smaller and smaller features demanded increasingly higher minimum interconnect density values at the same time that chip designs became much more aggressive in the circuit timing requirements. In such cases, it was often impossible to insert sufficient dummy fill into a tile such that the higher minimum density requirements could be met without also reducing the large "stay-away" distance, and thereby raising the timing impact of the dummy fill to levels that affected the performance of the chip. One potential solution was for the chip designer to waive the minimum interconnect density specified by a particular fabrication process. However, because invoking this waiver would not comply with the fabrication process requirements, the yield of the produced devices would not be guaranteed in such cases, which rendered this alternative not viable in practice.

71. Traditional dummy fill software tools of that time often completed their run through the tiles of each layer without reaching minimum interconnect density in some cases. In such cases, it would be necessary to re-run the dummy fill tool for those problematic tiles with a lowered "stay-away" distance and/or after adding, removing, or manually revising the size and positioning

of portions of the fill. If, as frequently occurred, more than one such tile lacked sufficient interconnect density and required (at least) a second run of the dummy fill tool with the revised "stay-away" distance parameters and/or dummy fill size and positioning, multiple runs could be needed if, as was typical, the dummy fill tool could only handle one tile at a time.

72. This iterative process, with manual adjustments of the "stay-away" distance, dummy fill size, and dummy fill positioning often required multiple runs for each such affected tile; it was an involved, time-consuming process that can and did significantly impact design schedules.

73. Prior to Lakshmanan '803, every layout change or other ECO required re-running the dummy fill tool, at a cost of approximately 30 hours per ECO on cutting-edge circuit designs at that time. (Lakshmanan'803 at 1:47–50.) The only way to guarantee that dummy fill would not intersect any design objects throughout the circuit design would be to re-run the dummy fill tool after each and every change. However, removing all of the original dummy metal fill geometries, doing the ECO, and then inserting new dummy metal fill could lead to different timing characteristics in areas of the device that were not affected by the original ECO itself, which cause additional iterations in the ECO process. Manual examination and alteration and/or removal of dummy fill intersecting design objects would be so time-consuming as to be commercially impractical even if it would not affect timing closure and interconnect density requirements (which it would). Even leaving dummy fill for the last possible moment could not be sure to avoid any subsequent ECOs, and there would also be no guarantee that sufficient interconnect density requirements and timing closure would be met on a single run of the dummy fill tool.

Explanation of Lakshmanan '803

74. Even when dummy fill could be placed in such a fashion that it would simultaneously satisfy interconnect density requirements for each tile and minimize any impact on

critical nets, prior to Lakshmanan '803, any change to layout or ECO would practically require rerunning the dummy fill tool for the entire layer, at a substantial time cost. That is because an ECO typically results in design objects (such as wires) being added and/or their locations being changed. (Lakshmanan '803 at 1:51–59.) In other words, while the routing has changed as a result of implementing the ECO, dummy fill insertion is typically not part of the routing portion of the process flow, but rather a separate step that is only done after the routing and timing closure stages of the design flow. (*See* 1:33–36; 2:62–65.) And that step must be redone for the entire layer to ensure that no dummy metal intersects with any of the design objects. (1:55–59.)

75. In place of having to deal with dummy fill in a batch process for the entire layer at a time whenever the layout changed, Lakshmanan '803 teaches a technique that permits layout changes without requiring that the entire dummy fill process be redone. Specifically, Lakshmanan '803 teaches that, following an ECO, the dummy fill tool performs a check to determine whether any dummy metal objects (which were inserted prior to the ECO) intersect with any other objects (such as signal nets) in the design data. (3:21–24.) Any such intersecting dummy metal objects are then deleted from the design database, which obviates the need to rerun the dummy fill tool after the ECO. (*Id.* at 3:24–27, 3:44–46.)

76. Because most ECO make only small incremental changes, most of the dummy fill is likely to be unaffected by the ECO. (*See* 1:55–57.) Accordingly, it is highly likely that even after deleting any dummy fill that intersects other design objects, the layout will still meet minimum density requirements for interconnect. If certain tiles fail to meet the minimum density requirement, the dummy fill tool may be used to add additional dummy metal at legal locations until the minimum interconnect density requirement is met, but it is not required to do so. (*See* 4:13–17.)

77. The significant efficiency gains from the ability to implement ECOs without having to rerun the dummy fill tool are repeatedly described within Lakshmanan '803. (*E.g.*, 1:46–50, 1:60–65, 2:20–22, 3:12–17.) This helps IC manufacturers "meet aggressive design schedules even though run-times for inserting dummy metal in large designs can be significant, and therefore saves time on overall design execution." (*Id.* at 4:52–57.) Based on my experience in semiconductor layout and design I agree that this new and improved process flow results in substantial efficiency gains in the design process for modern semiconductor devices. These gains are so substantial, and these incremental methods of dummy fill are so widely used today that it is hard to quantify just how important the inventions claimed by Lakshmanan '803 are to achieving current time-to-market for modern chip designs.

78. Based on my experience in semiconductor layout and design, it was not well-understood, routine, or conventional at the time of Lakshmanan '803 to perform dummy fill in an incremental fashion. In particular, it was not well-understood, routine, or conventional to identify dummy metal objects that, following an ECO, intersected other design objects and then delete such intersecting dummy metal objects from the design database. This feature, central to Lakshmanan '803, is required by every claim in the patent and recited explicitly in both independent claims. This is not only true in considering that element by itself, but also in an ordered combination with the other recited claim elements in creating a novel process flow that did not require a full-layer dummy metal fill simply to account for the relatively few objects that would intersect other design objects after an ECO.

79. Lakshmanan '803 explains, "A conventional design flow using a conventional dummy fill tool would require that the dummy fill tool be rerun after each change order was implemented to recompute the dummy metal 18 required for the design, severely impacting aggressive timing schedules." (3:12–17.) Rather, as I have explained, the typical process flows

and all the dummy fill tools of which I was aware lacked the capability to accommodate ECOs without a full-layer re-run of the dummy fill tool. Nor am I aware of any "unconventional" tools or process flows dating to the time of Lakshmanan '803 that had such capabilities.

80. During prosecution of the application that matured into Lakshmanan '803, the patent examiner expressly agreed in the Notice of Allowance that the claims as issued satisfied the requirements of 35 U.S.C. § 101. The examiner specifically agreed with Applicant's arguments that the practical benefits of the claimed invention, which resulted in substantial time-savings by avoiding having to re-run the design tool after a portion of the design data changed provided sufficient basis for patent eligibility. I agree with the examiner and the applicant.

Claim Charts

81. I have reviewed the Complaint supported by this Declaration, along with the Claim Charts showing infringement by Lattice of Lakshmanan '803 (Exhibit C) and Lakshmanan '989 (Exhibit D). For at least the reasons set forth below, I agree that the Claim Charts establish use of at least one of the methods recited by the respective claims of Lakshmanan '803 and Lakshmanan '989.

82. I have used design tools from different vendors in my career. As a consultant, I use the tools to review schematics and layouts, which has included industry-standard tools for detection of texted metal shorts. Based on the requirements for the latest process technology nodes, and the yield requirements for these technologies, the latest fill tools that are used by designers use timing-aware fill routines with minimum fill dimensions to meet timing as well as yield requirements simultaneously. These tools typically operate on an incremental basis; although they can and do insert dummy fill on a layer-by-layer basis, they typically operate in incremental fashion thereafter so that the impact of layout changes and ECOs to the overall design schedule is minimal and does not require rerunning the dummy fill tool for the entire layer for each and every

change. As I have done as a consultant, I can review either layouts post-fill or reverse engineering ("RE") of semiconductor die to confirm that these tools have been used to construct the layout or the die.

83. Lakshmanan '989 identifies that the invention operates on commercially available physical validation tools with DRC and LVS tools, such as the Calibre tool from Mentor Graphics Corporation (now Siemens). (Lakshmanan '989 at 2:59–3:3). As noted above, the typical design tool suite includes the DRC and LVS verification routines, as contemplated by the patent. Given the aggressive schedules for designing and bringing to market semiconductor devices and the ready availability of these routines in in common design tools like Cadence's Innovus product, it is unlikely (if not implausible) that most chip designers would not have access to design tools that practice the inventions claimed in Lakshmanan '989. It is even less likely that such designers would not use the features that allow for identification of texted metal shorts prior to the end of the design flow. Because failure to detect a texted metal short can require a restart of the entire design process and substantially delay the process of bringing chips to market, any entity who declined to use these features would be at a substantial competitive disadvantage in bringing its products to market in a timely fashion. As such, based on my experience in semiconductor layout and design, and my review of designs and supervision of designers that used such tools, I believe that it is highly unlikely that such functionality was not used in creating most modern semiconductor devices.

84. Given the aggressive schedules for bringing modern semiconductor devices to market, and the availability of incremental dummy fill in common design tools like Cadence's Innovus product, it is unlikely (if not implausible) that most chip designers would not have access to design tools that practice the inventions claimed in Lakshmanan '803. It is even less likely that such designers would not use the incremental dummy fill features that allow ECO without a time-

consuming (and design-freezing) repeat of the dummy fill insertion process for the entire layer whenever the layout changes or another ECO is implemented. Especially because these typically happen late in the design process, and often happen more than once, any entity who declined to use these features would be at a substantial competitive disadvantage in bringing its products to market in a timely fashion. As such, based on my experience in semiconductor layout and design, and my review of designs and supervision of designers that used such tools, I believe that it is highly unlikely that such functionality was not used in creating most modern semiconductor devices.

85. Even when the full history of the GDSII database for a particular integrated circuit is not available, my experience in semiconductor design and layout gives me sufficient basis to opine whether one or more of the methods claimed in Lakshmanan ’989 and/or Lakshmanan ’803 have likely been used in creating integrated circuits.

86. Because the power map is central to semiconductor processing design, and an error resulting from a texted metal short can cause substantial portions of the design process to be duplicated as components need to be relocated, I believe that it is highly unlikely that anyone using the Cadence Innovus tool (or another design tool with similar functionality for physical verification) to create a modern IC would not have used at least one of the inventions recited in Lakshmanan ’989 to minimize the delay from the late discovery of a texted metal short. The capability to perform physical verification according to the inventions recited in Lakshmanan ’989 is present in all commercially available design tools, and the failure to use these tools would result in a severe competitive disadvantage and substantial delays in bringing products to market.

87. Given the multiple dependencies in the semiconductor processing design flow and the reality of ECO after layout has been completed, I believe that it is highly unlikely that anyone using the Cadence Innovus tool (or another design tool with similar functionality for incremental

dummy metal fill) to create a modern IC would not have used at least one of the inventions recited in Lakshmanan '803 to minimize the delay from a post-routing ECO. The delays from having to manually re-run the dummy fill tool after each ECO or layout change so impactful that failure to use these now-commonly available tools would result in a severe competitive disadvantage and substantial delays in bringing products to market.

88. By contrast, based on my experience in semiconductor layout and design, I would only assume that relatively simple IC designs would have been made in recent years without employing at least one of the methods claimed in Lakshmanan '989 and Lakshmanan '803.

89. The Cadence paper "New Metal Fill Considerations for Nanometer Technologies" demonstrates several things. First, the use of the word "new" is justified in that it is a new approach, as documented here. Secondly, it reinforces the importance of formulating "a comprehensive methodology surrounding metal fill . . . in order to minimize impact on design timing as well as to cut down on design iterations." The paper explains that "sometimes the dummy metal fill geometries that were added to the original design must be deleted to make room for the ECO process to succeed," before identifying the solution as ignoring the effect of ECO on dummy fill in the first instance. The paper elaborates that allowing ECO "to cause shorts and/or DRC violations" from existing dummy fill following an ECO, and then repairing any violations will reduce the overall time to complete the ECO, including handling of the metal fill and its effects. Overall, this evidences that the Cadence tool suite is used for incremental dummy metal fill modification following ECO as claimed in Lakshmanan '803.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Dated: August 24, 2022

Lloyd Linder

EXHIBIT 1
to
EXHIBIT E

cell 818.632.9660
lflinder@yahoo.com
09/22/2021

Lloyd F. Linder

Skills summary

Extensive experience in high performance / high dynamic range analog mixed signal, custom digital, and RF integrated circuit design, layout, and test, from concept to production for commercial, military, and space IC products. Have knowledge of IC process development, characterization, and modeling. Have significant amount of experience in obtaining new military, space, and commercial IC business, as well as obtaining funding for start-up activities. Technical oversight for large IC design teams (20-40 people). Have ability to contribute creatively to the solution of difficult technical problems. Have 99 U.S. patents issued with twenty U.S. patents pending. Have 200-300 issued international patents. Have experience at the discrete analog / RF / mixed signal board level design and layout, system analysis, link budget analysis.

Specialties:

IP analysis / technical due diligence for M&A

IP portfolio management and creative contribution to new IP generation

Prior art searches and technical support for patent office action amendments

Perform simulations, review IP, and provide expertise in support of patent litigation

System Design/Architecture/Analysis/Block Specifications

New business development/capture

Winning proposals for small (SBIR Phase I and II) and large businesses

Product road maps

VC funding pursuits

Technical due diligence for VCs, angel investors, and M&A

IP creation and protection

Client deposition

Technical lead for IC design groups and product development

AMS/RFIC Design Chip/Circuit/System Architect

High speed, high performance ADC, Sample/Hold, ADC drvier amplifier, and DAC architectures

RF/AMS/SOC BIST/DFT architectures and methodologies

PLL and DDS

Digitally programmable RF transceivers/SDR/GPS/cellular/wireless transceiver architectures

RF TxRx, optical TxRx, modulator driver, LDD, TIA

Flash Ladar, active/passive imaging ROIC

regulators, high voltage/high current switches, ATE electronics

SiGe BiCMOS, CMOS, SOI, bipolar, Complementary bipolar, GaAs, InP

Digital beamforming

Cadence tools - schematic capture, SPECTRE, layout review

Solutions to production problems

Secret clearance

Objective

Looking for consulting opportunities to utilize my experience and provide technical leadership in all aspects of analog / mixed signal / RF integrated circuit and discrete circuit design: architectural conception, design, simulation, layout, test, and measurement / simulation correlation.

Experience

April 2006 – Present

Lloyd Linder Consulting

Consultant

Black Forest Engineering / Luminar Colorado Springs, CO.

- Architecture development for next generation automotive lidar ROIC

Strategic IP Initiatives Inc. Morgan Hill, CA.

- Review of patent portfolio for PIC applications in SFP optical modules

GreyB Service Pte Ltd Shaw Centre, Singapore.

- Provide expertise for many different invalidity cases for many different clients

Upwork Santa Clara, CA.

- Technical writer for application notes and VNA user's guide

Syrnatec Inc. Newington, CT.

- Consult on ROICs for SBIR proposals

Kenney&Sams, P.C. Boston, MA.

- Expert witness in software defined radio development case

Microchip Technology Inc. Burnaby, Canada

- Participated in ADC architecture study for 28 and 56 GBps SERDES products.
- Did webinar for world-wide IC design staff on ADC design issues.

ElevATE Semiconductor Carlsbad, CA.

- Write white paper on ATE products.

GoodIP GmbH Munich, Germany

- Review and analysis of GaN and LED patent portfolio for potential acquisition.
- Spoke as the GaN / LED IP expert at webinar to discuss IP auction.

Nevada Nanosystems Inc. Reno, NV.

- Review and analysis of ASIC architecture and requirements in support of MEMS control circuitry. Evaluate IC design houses in the down-select process.

Axzon Inc. Austin, TX.

- Contribute to the analysis and review of CMOS transceiver architecture for UHF RFID reader.

Microcosm Inc. Torrance, CA.

- Architect the discrete RF transceiver and analog base band signal processing solution for digital beamformer. Develop packaging concepts for the beamfomer and interface to the antenna elements.

Otava Inc. Moorestown, NJ.

- Contribute to the definition of overall transceiver and circuit architectures for 5G beam formimg solution for 28-40 GHz 5G applications.

Analog Circuit Works Boston, Mass.

- Review of specification for fiber optic SOC application. Contribute to system level analysis and architecture.

Second Sight Medical Sylmar, CA.

- Debug of current eyewear for blind people. Contribute to reduction of noise and coherent spurs in current product.

Linear Microsystems Irvine, CA.

- Architect for high volume SOC for VR headset application. System analysis for SOC proposal for fiber optic communications applications.

Teqnovations Colorado Springs, CO.

- System level architect for receiver for phased array radar applications.

Analog Devices Inc. Colorado Springs, CO.

- Work with design team on a DAC buffer IC to improve performance in the lab and remove oscillation. Review existing architecture for redesign and developed new architecture.

Facebook Woodland Hills, CA.

- Schematic and board layout reviews of electronics for flight system

GHB Intellect San Diego, CA.

- Review of Patent claims for client for multiple issued patents in the wireless communications area.

BINJ Labs Scituate, MA.

- Definition of top level Software Defined Radio architecture for wide band operation. Work with board development effort and SDR development company.

Sentinel Monitoring Systems Inc. Tucson, AZ.

- Schematic review of high speed data converter and timing board schematic.

FlexPowerControl Woodland Hills, CA.

- Consultation on system level requirements document in-home energy control product development. Develop IP for the company.

SpectraResearch Dayton, OH.

- Consultation on integration considerations for discrete X-band and Ka / Ku-band transponder architecture for SWAP-C improvements.

McKool Smith Dallas, TX.

- Perform simulations of IP for RFIC receiver, and provide expert opinion for patent litigation in a report for case :2:15-cv-00011-JRGRSP in the United States District Court for the Eastern District of Texas.

Quantum Semiconductor LLC San Jose, CA.

- Consultation on architecture and simulations for proprietary ADC architecture.

Maven Research San Francisco, CA.

- Consultation on use of design house by third party for products.

Faraday Technology Corporations Santa Clara, CA.

- Review of third party transceiver RFIC schematic design, layout, and testability.

Irunway Dallas, TX.

- Review of IP for legal firm in patent litigation. Simulation of IP for transceiver RFIC. Simulation results included in expert report.

Alphacore Inc. Phoenix, AZ.

- Architecture review and enhancements of high speed CMOS ADC and visible monolithic imaging chips. Develop DROIC architectures for SBIR proposal pursuits.

Brady Worldwide Inc. Milwaukee, WI.

- IP review of start-up for potential investment / acquisition. Develop sensitivity analysis for present products and future CMOS technology scaling.

InPhi Corporation Westlake Village, CA.

- Review and contribute to architecture refinements for single channel and multi-channel EAM drivers for 2 level and 4 level PAM. Perform architecture study for low power EAM driver.

DRS RSTA Inc. Cypress, CA.

- Help with EDA methodology for AMS design for ROICs.

Ridgetop Group Tuscon, AZ

- Architected wide band RF front end for multiple current SBIR proposals.

Space Micro San Diego, CA

- Review of 0.18 μm CMOS quadrature DAC design and layout.

Teradyne Agoura Hills, CA

- Analog DFT / BIST / testability architect for 40 nm CMOS SOC for next generation Teradyne tester. Architect transistor level circuit solutions for power supply IC for DUT testing. Investigate high voltage CMOS and complementary bipolar process technologies for internal design development with unique current clamping architecture. Define baseline circuit topology and perform simulations.

Lockheed Martin Moorestown, New Jersey
Littleton, Colorado
Deer Creek, Colorado

- Involved in high voltage driver IC development for GaN PA.
- Involved in architecture development and review of wide band band receiver integrated circuits from DC to Ka / Ku in SiGe.
- Involved in overall ADC architecture development and definition, and transistor level circuit architectures, for next generation RFIC transceivers and data converters. Architect of next generation transceiver architectures for SOC / heterogeneous applications. Involved in study for government customer of data converter architectures for next generation digital beam forming applications. Architecture review and development for high voltage analog driver array. Involved in architecture for multiple receiver RFIC developments for S, C, and Ka bands.

HRL Malibu, CA

- Perform market survey of component technologies for multi-mode, multi-mode commercial software defined radio applications. Summarize capability for data converters, front end modules, antennas, transceivers, and base band processors. Compare the available technology to an architecture based on custom chip development for the solution.

Micrel San Jose, CA

- Involved in the testing, debug, and redesign of a 65 nm CMOS 2.4 G / 5 G WiFi transceiver product. Provide technical guidance for redesign of RF front end and the 2.4 G / 5 G LO clock distribution.

Key2Mobile Westlake Village, CA

- Developed RF transceiver concepts for multi-band, multi-mode remote radio head system. This is included transceiver architectures based on digital beam-forming and direct RF sampling and direct RF synthesis data converters.

Hittite Microwave Colorado Springs, CO

- Consultant on the architecture for the high dynamic range, high speed IBM SiGe 8HP BiCMOS DAC and complementary bipolar ADC driver amplifier products for the cellular base station market.

Semtech Redondo Beach, CA

- Technical consultant on IBM SiGe 8HP BiCMOS interleaver IC and IBM 32 nm SOI monolithic coherent detection transceiver SOC for 100G coherent optical detection systems. Involved at the architectural level for the SOI interleaver, 8

bit, 64 GSPS ADC, and 8 bit 64 GSPS DAC circuits, and overall system calibration.

- Developed concepts for 10-12 bit, 4-8 GSPS ADC architectures for digital array radar and digital beam-forming applications, as well as high performance sample and hold architecture for military applications.

FBI Westwood, CA

- Technical consultant on matters of national security. Awarded medal for service to the country.

Nu-Trek Inc. San Diego, CA

- Developed an RF BIST architecture for characterization of a RF transceiver. Helped the company win Air Force Phase I and Phase II awards.
- Involved with test evaluation of pipeline ADC for cryogenic applications, L1 / L2 band GPS receiver, and Universal Reliability SOC development for lifetime testing of X-Band and L-Band transceivers.
- Responsible for the development of the company's product roadmaps.
- Contributed to SBIR and STTR proposals on nonlinear coupled oscillators for active array applications, active sonar signal processing, high dynamic range ADC, GPS, RFIC transceivers, RIICs, and ROICs. Involved in testing of ADCs for ROICs, and architecture development for RF BIST.

FLIR Electro-Optical Components Ventura, CA

- Technical lead for the development on ROIC architectures for NASA, Navy, Air Force, MDA, and Army SBIR Phase I and Phase II programs. Development of novel active and passive unit cell architectures.

SYS Technologies / Kratos Defense San Diego, CA

- Review of SiGe BiCMOS class E power amplifier design to improve reliability of operation. Reviewed circuit, simulation results, test results (dynamic and DC), and performed thermal analysis based on self-heating.
- Review of schematic and layout for small form factor PCB that contains GPS transceiver RFIC and companion digital ASIC. Review of schematic and layout for PLL, IF / baseband test chip evaluation boards. Suggestions for characterization / test debug**.**
- Review Transmitter and Receiver schematics and block layouts of GPS transceiver IC in IBM 7HP 0.18 µm SiGe BiCMOS for redesign effort. Review of improved receiver IC design.
- Review of test results for the evaluation board and suggestions for characterization and debug. Review of board design and layout revisions for improved electrical and thermal drift performance for successful demo. Help with board yield and manufacturing issues.

Aerius Photonics LLC Ventura, CA

- Technical lead for STTR Phase I ROIC circuit design partner.
- Developed ROIC architectures for laser vibrometer SBIR Phase I proposal.

LinearChip Inc. Aliso Viejo, CA

- Developed complete single chip CMOS 802.11 a/b/g/n/ac transceiver architecture, with on-chip T/R switch, for proposal to commercial test equipment house.
- Developed CMOS MSK transmitter for patient temperature monitor and medical equipment tracking ASIC. Developed overall quadrature transmitter architecture, circuit topologies for the DAC, active filter, quadrature mixer, power amplifier, and temperature stabilized reference oscillator. Performed noise / distortion budgets, duty-cycled power calculations for extended battery life, determined PLL phase noise requirements, and defined the circuit block specifications.

Technical lead for the circuit simulations in XFAB XH018 0.18µm CMOS RF process.

- Participating in pursuit of new IC design business. Development of PHEMT TIA gain block concept, satellite receiver / de-multiplexer architecture, CMOS and SiGe RF receiver architectures, and CMOS analog AFE for hand-held controller for telescope, including 16 bit audio DAC architecture. Involved with multiple RFIC proposals for military and commercial applications. Developed multi-channel AM/FM receiver for location positioning application.
- Developed unique TIA / AGC / output amp circuit concept for cable TV over fiber market based on JAZZ 0.18µm SBCH18XL SiGe BiCMOS process.
- Review of battery charger circuit architectures for XFAB XC06 0.6 µm CMOS IC. Architecture suggestions for capacitor charging loop and low battery indicator circuit.

Wistron Corporation Taipei, Taiwan

- Contributed to discrete quadrature receiver architecture for a new module business proposal to DirectTV.
- Involved with review of existing ODU L-Band module specifications, and application to new digital L-Band module. Contribute to the definition of ASIC requirements and discrete component requirements for new ODU architecture.

Arete Associates Sherman Oaks, CA

- Phase I and internal IRAD programs for advanced TIA architecture development for high speed laser pulse return processing.
- Review of schematics, simulation results, and layout floor plan, and layout for a 64 channel TIA / OTA wavelength converter in IBM 5HPE 0.5µm SiGe BiCMOS. Function is to receive 1 ns laser pulse and provide linear gain for retransmission. Made suggestions for additional simulations for design robustness and concerns, as well as improved performance based on layout changes. Also made layout suggestions for improved isolation and performance.
- Developing unique 3D FPA and digitally programmable ROIC pixel unit cell architectures for inclusion in STTR proposal.
- Review of 2 TIA input / 128 channel output VCSEL driver, 2 GHz pulsed sampling IC in IBM 7WL 0.18 µm SiGe BiCMOS.

Raytheon Corp. Dallas, Tx. / El Segundo, CA

- Involved in the development of 40 GSPS ADC architecture in 32 nm IBM SOI.
- Involved in development of on-chip mechanical stress measurement circuit for thermal imaging sensor IC in IBM 9SF 90 nm CMOS process. Submitted patent disclosure on stress sensor circuit. Reviewed the pixel circuit design and the overall ROIC circuitry and timing.
- Participated in winning MDREX proposal effort to AFRL to develop high performance 10 bit, 2.2 GSPS ADC, 14 bit, 3 GSPS DDS, and 1:4 DMUX ICs in IBM 8HP 0.12µm SiGe BiCMOS, and integrate these functions with 8HP receiver and transmitter circuits developed by AFRL, as well as 8HP bias and control circuits developed by Raytheon. Involved with Phase I kick-off meeting.
- Participate in SBIR proposals development with partners Nu-Trek and Crossfield. Developed design methodology for CMOS GPS SOC integration. Developed sub-threshold CMOS RF circuits for low power GPS receiver concept. Generated phase adjust circuit for RF clock distribution for antenna array electronics, and submitted patent disclosure. Contributed write-up on high speed, high performance DAC topologies for DDS proposals. 1 Phase I SBIR proposal awarded.

- Schematic and layout review of IBM 7HP 0.18µm SiGe BiCMOS digital control and bias regulation circuits for MMIC common leg circuit. Reviewed regulator loading problems, solutions, and simulation results. Made simulation recommendations for verification of design robustness. Reviewed metal mask fixes.
- Review of test data, process parameters, and circuit design for production HRL G1.5 2µm InP band-pass Σ-Δ IC for yield enhancement. Developed vendor RFQ for multi-phase IC redesign effort.
- Involved in metal mask effort for 14 bit, 3 GSPS DDS / DAC IC in IBM 7HP 0.18µm SiGe BiCMOS through the Trusted Foundry program. Contributed to design, layout changes in the high speed digital DLL section to improve performance for higher clock applications. Documented circuit design limitations for future redesign for clock rate enhancement.
- Analyzing test data, PCM data for the metal mask DDS chip. Correlate sensitivity of test results to process parameters, and simulation results, to improve yield on future fabrications. Investigate design improvements for possible new mask set. Provide suggestions for performance improvements at the board level. Involved in improvements of the DLL section for next all-layer mask release.
- Member of team analyzing radiation induced latch-up effects in commercially available data converter for space application. Involved in focused laser beam testing to create single events in the converter. Analyzing radiation data, reliability data, and design guides for end-of-life DC power estimates for ICs designed in NS 0.8µm ABIC-IV BiCMOS, MAXIM GST-1 bipolar, IBM 5SF CMOS, and Honeywell HX3000 SOI.
- Review of link budget and block performance for IF and base-band ICs implementing high dynamic range receiver, including IF amp, mixer, VGA / attenuator, and ADC driver amp in IBM 5HPE 0.5µm SiGe BiCMOS. Made architectural suggestions for improved performance. Reviewed test results, and made suggestions for debug.
- Design review of IBM 5HPE 0.5µm SiGe BiCMOS IF receiver ASIC including mixer, gain control amp, and ADC buffer amplifier. Review of measurements for test circuits.
- Jitter analysis for ADC module clock path using divider circuits.
- Design reviews of IBM 5DM 0.5µm SiGe BiCMOS L1 / L2 GPS dual channel receiver IC: LNA1, LNA2, RF amp, RF mixer, IF mixer / AGC, gain calibration loop, baseband amp, PLL, and ADC. Defined layout floor plan, channel layout isolation techniques, and package requirements to meet isolation requirements. Reviewed final GPS receiver layout and developed plan for simulation of layout, package, and external component parasitics. Contributed to correlation of test results. Review of socketed test board layout.
- Review of quad channel IQ detector hybrid design and layout. Made suggestions for debugging of existing hybrid oscillation and improved performance. Review of TI BiCOM-2 0.7µm CBiCMOS IQ IC performance and correlation to hybrid measurement.
- Review of simulations and test results for IBM 8HP 0.12µm SiGe BiCMOS millimeter wave transceiver chipset module performance from outside vendor.
- Review of M/N PLL hybrid design. Review of TI BiCOM-2 0.7 µm CBiCMOS M/N PLL IC performance and correlation to hybrid measurement.
- Performed BOL and EOL noise analysis to estimate the jitter of on-chip clock receiver circuits for the SPT7760 ADC IC based on the MAXIM GST-1 process parameters, and off-chip COTS components for satellite application.

Menara Networks Irvine, CA

- Reviewed schematics and simulation results for high frequency, multi-GHz active RF low pass filter in JAZZ SBC18HXL 0.18µm SiGe BiCMOS. Involved in top level layout review of first generation EDC IC.
- Contributing to the development of Nyquist 10 GSPS sample / hold circuit, for hold mode feed-through reduction, low distortion, and low power. Contributed to the DC AGC circuit to generate coefficients for Gilbert multiplier as well as developed a new summing circuit for the sampled signals in the analog sampled FIR filter. Involved in solving layout-induced performance problems.
- Involved in the clock distribution architecture and feedback loop to reduce DC offset effects on zero crossing. Review of regulator circuit power-up issues. Created new ADC-based residue architecture to generate the appropriate transfer function for a phase detector circuit for consideration on a higher performance, lower power version of the existing Fiber Optic Receiver IC in JAZZ SBC18HXL 0.18µm SiGe BiCMOS.
- Preliminary review of third party design of 10 Gb/sec CDR PLL schematic blocks for SOC application in STM 0.13µm SiGe BiCMOS. Reviewed metal mask circuit design changes.

MOSIS / ISI Marina del Rey, CA

- Review of MOSIS website. Provide report consisting of ways to improve technical and business information on the website, as well as customer support. Used client questionnaire to provide additional insight into website, technical information, customer service and support.

Tangea Semiconductor Manhattan Beach, CA

- Participated in business plan development, facility requirements, engineering manpower requirements, technical concepts, and potential investor meetings.

Technoconcepts Inc. / Terocelo Van Nuys, CA

- Involved in the design, development, and review of RF receiver and transmitter ICs for multi-band, multi-mode applications using JAZZ SBC18HXL 0.18 µm SiGe BiCMOS. Versions of the Receiver IC include RF VGA, mixer, RZ (Return-to-Zero) and NRZ (non-Return-to-Zero) 6 GSPS 1 bit Σ-Δ ADC, with 2 feedback DAC and 3 feedback DAC versions, PLL, 1:16 DMUX, and base band decimation and filtering. Activities include circuit-level architectures to improve existing performance, schematic and simulation reviews, top level layout floor-planning, layout review, and evaluation board review.
- Involved in testing and correlation of packaged part performance, to simulation, for noise density, harmonic distortion, and intermodulation distortion products. Involved in architecture improvements and enhancements, based on test results, for a metal mask effort. Improvements include extension of VGA architecture to extend the input 1 dB compression point, IIP3, and bandwidth. Added provision to sample very low input frequencies. Improved the dynamic range of the transconductance amplifiers in the modulator. Added dither DAC at the comparator input to improve idle tone performance. Extended the dynamic range of the present RZ Σ-Δ design. Improved the DAC settling and noise response. Added an LNA, and a single-ended to differential converter to interface to the existing VGA.
- Development and layout of test chips for the TSMC 90nm CRN90LP CMOS RF process. Designs include single-ended, wideband and tuned versions of high IIP3 LNA architectures using novel distortion cancellation techniques for operation in the 1- 6 GHz frequency bands. Also developing versions of a 1.8V bidirectional, tri-stated CMOS / LVDS I/O driver with resistive and active back terminations,

and a single input, multi-band, multiple output, switched / tuned RF front end. Involved with CASCADE probing, and correlation to simulation results.

- Development of a wide-band, software defined, multi-band, multi-mode, receiver chip for the TSMC 65nm CRN65GP mixed signal / RF process. Architected the circuits for the wideband LNA with novel AGC and attenuator, the RF DMUX / on-chip RF filter bank, the RF MUX / single-ended-to-differential converter, the quadrature mixer with AGC, RSSI log amp, and the programmable base-band filters. All the RF blocks utilize IM3 cancellation. Target services include AM, FM, DTR, DTV, WiFi, and WiMAX for automotive application for Japanese customer. Involved in the link budget analysis, block specifications, and the requirements for the associated base band ADC and PLLs for the high band LO, low band LO, and ADC LO ICs. Also proposed this architecture for NSF proposal in order to obtain additional development funding.
- Involved in the design, layout, and review of customer demonstration board, based on existing transceiver chipset, for WiMAX applications, using Picochip base-band processor.
- Developing transceiver architecture concepts for multi-service / simultaneous /switched reception off of single multi-band antenna, diversity, and MIMO with self-calibration. Developed low power architecture for multi-service receiver summing into single ADC. Developed transmit / receive architecture for multi-band, multi-mode military radio. Architectures are baseline for new business opportunities.
- Developed IBM 0.12µm 8HP SiGe BiCMOS low power LNA topologies for 10-20 GHz for SBIR proposal. Developed RF interference cancellation architecture for SBIR proposal.

Red Dot Wireless Milpitas, CA

- Performed transceiver architecture study for TD-SCDMA / EVDO / WiFi / MIMO WiMAX application. Involved in presentations to investors.

Ubidyne Ulm, Germany

- Schematic, simulation, and layout review of IHP SG25H1 SiGe BiCMOS S1.0 Receiver RFIC. Review of characterization test results.
- Schematic, simulation, and layout review of JAZZ SBCH18XL SiGe BiCMOS S2.0 receiver, transmitter, and PA driver IC designs. Schematic and layout review of Toshiba 90nm CMOS high speed custom digital IC design.
- Review of test data and circuit design for S2.0 receiver to determine yield issues.

Dynamic Research Corporation San Diego, CA

- Review of existing top level IC issues and proposed packaging approach for GPS transceiver in IBM 7HP 0.18 µm SiGe BiCMOS.

Q3Web Wideband Wireless Inc. Harbor City, CA

- Constructed white paper on the development of IP libraries in the IBM CMOS and SiGe BiCMOS technologies for use by military contractors. Being submitted to government for funding consideration.

August 2009 – May 2011 Aerius Photonics Ventura, CA.

Senior Systems Engineer

- Directly responsible for winning new SBIR business for ROIC development. Captured $2.6M of ROIC development money. Have written multiple winning proposals for Army, Navy, MDA, NASA, Air Force, and NSF SBIR Phase I efforts. Have won Navy and ARMY Phase II efforts. Additionally, supported other proposal wins for other technology developments.

- Responsible for the development of new and novel circuit concepts for CMOS and SiGe BiCMOS passive and active imaging ROICs. Have found and engaged ROIC design partnerships. Involved in new business development.
- Have defined ROIC specifications and system requirements in conjunction with BALL Aerospace, Sensor Creations, Raytheon, BAE Systems, Arete and Associates, Tetravue, IDEO, Microvision, Velodyne, and other military and commercial contract partners.
- Technical lead for the conceptual phases of the following ROIC developments: JAZZ SBC35 ROIC for laser vibrometry, ON Semiconductor C5 0.5µm ROIC for 3-D FLASH LADAR for beach zone / surf zone applications, ON Semiconductor C5 0.5µm CMOS ROIC for dual well application (patent pending), JAZZ SBC18 CMOS monolithic imaging ROIC with integrated SiGe APD, and ON Semiconductor 0.18µm CMOS 1920 X 1080 SWIR ROIC.
- Contributed to the development of new laser range finder receiver architecture with unique time programmable gain.
- Developed digitally programmable pixel architecture and specifications for linear direct / coherent detect ROIC for STTR Phase I effort.
- Technical lead in development of single pixel discrete board level customer demo for STTR Phase I LADAR application, and board developments for: 10 Gb/second hexagonal InGaAs detector array, custom ROSA and CDR, 4 X 4 array with fan-out electronics in support of sub-ns laser returns, and new laser range finder receiver.

April 2008- January 2009 Menara Networks Irvine, CA

Director of ASIC Development

- Involved in simulations of existing Electronic Dispersion Compensation (EDC) IC to correlate to measured performance to define metal mask effort for JAZZ SBC18HXL 0.18µm SiGe BiCMOS IC. Helped define testing for chip characterization.
- Patent application on interleaved FIR with unique sample / hold for extended high dynamic range over previous implementations.
- Contributed to architectural improvements for low power version of EDC IC in IBM 8HP 0.13 µm SiGe BiCMOS.
- Performed simulation trade-off study to compare circuit performance for transmitter application in TSMC CMN65LP 65 nm CMOS, IBM 10LPE 65 nm CMOS, and IBM 8HP 0.12µm SiGe BiCMOS.
- Simulation and design of transmitter pre-driver and output driver for quad 10 Gb/s transceiver with integrated EFEC in IBM 10LPE 65 nm CMOS.
- Simulated low power EML driver concept in IBM 8HP 0.12µm SiGe BiCMOS.
- Involved in the investigation and development of new architectures in support of 100 Gbit/s optical links.
- Review of board schematics and layouts for EDC IC evaluation board, OTN XFP module, and OTN 300 pin module.

February 2002- April 2006 TelASIC Communications El Segundo, CA

Director of Technology / Founder

- Technical lead for next generation single supply (+5V) data converter ICs in IBM 0.5 µm 5AM SiGe BiCMOS: RF sampling 10 bit, 1 GSPS ADC, on-chip sample / hold, and up-converter IC with integrated 14 bit, 1 GSPS DAC, IF amplifier / mixer. Developed self-heating error correction for quantizer preamp.

- Technical lead for new business pursuits in military and commercial integrated circuits. These included RF handset transceivers, spot BTS, fiber optics, analog transmit cancellation receiver for Gigabit Ethernet, automotive radar, data converters, sample / hold, FPA imaging sensor readout, and arbitrary waveform generators. Technical lead in new business pursuits in board-level DPD-based transceivers based on COTS components. Involved in proposals with Raytheon for DARPA programs, including RHBD (Rad Hard by Design) and Team Phase II.
- Technical advisor for the conception, development, and commercial production of the TC2412 14 bit, 737 MSPS DAC IC and TC1412 14 bit, 250 MSPS ADC IC in IBM 5AM (data sheets available at www.telasic.com/website/products). Architectural contributor to base station transceiver chipset concept. Data converter IC products are being sold to PMC for the NTT DoCoMo base station market. Involved in development of IBIS models of DAC and ADC IC for customer board level simulations.
- Technical contributions to various IC designs including IBM 5AM ADC driver amps, Re-sampler, IBM 7HP test chips, including sample / hold, amplifier, mixer, ring oscillator, and 14 bit, 3 GSPS DDS. IBM 8T chips including re-sampler and 3 bit / 40 GSPS sample / hold / Quantizer / DAC.
- First version of the ADC IC developed, TC1411, received analogZone 2003 Product of the Year Award.
- Involved in business plan development, process to obtain first round of funding.
- Performed technical due diligence on potential new investments for venture fund.

1999– February 2002 Raytheon Advanced Products El Segundo, CA

Engineering Fellow

- Technical lead for new business pursuits in military / commercial ICs, working with organizations across the company. Programs won include: SIMBAW, TEAM, ADRT, ULTRACOMM, ACN, 3D Flash Ladar image sensor, and APLA.
- Involved in FPA multi-sampling ROIC developments in AMI 0.5µm CMOS: 10 X 10, 64 X 48 arrays. Unit cell development in IBM 0.13 µm CMOS for 256 X 256 array. Developed fan-out concept to maintain small cell pitch while allowing for multi-sampling analog architecture. Evolved multi-sampling concepts for programmable sample time stamp and number of samples.
- Technical advisor for integrated circuit development across Raytheon. This includes design review / debug of existing IC developments.
- Involved in the design and development of data converters, IBM 5HP IF sampling Band-pass Σ-Δ, compact DDS, and RF transceivers for the military and commercial markets. Circuit concepts include fast frequency hopping PLLs, active biquad filters, and a sine weighted DAC.
- Developed Tondelayo 802.11a half duplex transceiver chipset in IBM 5HP for start-up (Systemonic) acquired by Philips. The transceiver demonstrated 802.11a frequency bands in the 5- 6 GHz frequency range using a PCMCIA format.
- Technical contributor to conversion of 0.6µm to 0.5µm NS CMOS for 14 bit, 10 MSPS radiation hard, algorithmic ADC. Involved in design and review process.
- Cooperative effort with LUCENT for next generation design improvements and completed plastic / ceramic package performance evaluation trade-off of CSP1152A CMOS 14 bit, 65 MSPS ADC for Sirius radio application.
- Technical evaluator for BOEING 0.35µm CMOS 1.0625 Gbit/sec Multi-channel Fibre Channel Transceiver for Raytheon AESA application. Contributed to

design reviews, layout reviews, design changes / iterations, suggested simulations to run, and evaluated test results.

- Developed concepts for the integration and packaging of RF MEMS devices with integrated circuits. Circuit architectures included RF front ends with tunable capacitors, tunable RF band-pass and notch filters, as well as active MUX circuits for frequency hopping between filters.

1993–1999 Hughes Communications Products El Segundo, CA

Senior Staff Engineer / Senior Scientist

- Technical lead of the development ICs for the Digital Receiver Program. This included NS ABIC-IV 0.8µm BiCMOS ICs with the following functions: LNA, mixer, LO driver, DAGC, fractional frequency hopping low phase noise PLL, IF amplifier, video amplifier, serial interface, log detection / blanking, and control logic, and a LUCENT CBIC-V2 summing amplifier IC. Involved in the packaging and test of plastic packaged parts. Digital Receiver board contained 2 chip UHF receiver, single chip GPS receiver IC, and master PLL IC.
- Technical lead for research and development of RF and analog ICs in CMOS, Hughes NB SOS / SOI, silicon (NS ABIC-IV, V, MAXIM SHPi), and IBM SiGe bipolar / BiCMOS process technologies. Functions included LNAs, RF LNA, mixer, VCO, ring oscillator, video amplifier, IF amplifier, sample / hold, high speed 10 bit ECL-to-CMOS translator / latch, 12 bit DAC, and LP Σ-Δ.
- Development of AM / FM LNAs in IC Delco 1.2µm CMOS for automotive radio.
- Involved in the chipset development for NS for the 1.0625 Gbit/sec ANSI X3T11 8B/10B standard using ABIC-IV process. Involved in laser diode driver, TZA, SIPO, PISO, Transceiver ICs.
- Involved with process development / modeling for CMOS, SOS, and silicon / SiGe BiCMOS process technologies.
- Team member of the NS ABIC-IV ADC chip development based on requirements for the ICO satellite system
- Involved in the debug, characterization, and production of hybrids and modules for airborne radar and AMRAAM missile applications.

1991–1993 Radar Systems Group, Hughes Aircraft El Segundo, CA

Staff Engineer

- Lead the IC development of high performance data converter components including sample / hold, summing amplifier, timing generator, band-gap, ADC reference amplifier, video amplifier, DAC, flash quantizers, and buffer amplifier in LUCENT CBIC-U / U2 and MAXIM SHPi and CPi processes.
- Involved in the development of mixer ICs for high dynamic range radar using HRL InP, AlGaAs, and Litton and Hughes D-MESFET technologies.

Fall Semester 1990 Electrophysics Department, USC Los Angeles, CA

Lecturer

- Taught EE448, Senior Electronics. Generated syllabus, created homework problems, tests, and solutions. Handed out final grades.

1986–1991 Radar Systems Group, Hughes Aircraft El Segundo, CA

Member of Technical Staff

- Involved in the design of components for high performance data converters.

- Contributed to the design of high dynamic range buffer amplifiers, sample / holds, integrators, and gain stages in Hughes 2 µm CBiCMOS, Fairchild 1.25 µm Fast-Z Fineline, and NS Aspect-II, Aspect-III, and ABIC-IV.
- Designed 2 bit adaptive threshold ADC IC in ORBIT 2µm CMOS for EPLRS radio.
- Contributed to architecture for Hughes NB 2 µm CMOS gate array ASIC.
- Involved with process development / modeling for bipolar, complementary bipolar, CMOS, BiCMOS, CBiCMOS.
- Generated analog tile array for the Hughes Carlsbad CBiCMOS process.

July 1985–1986 Radar Systems Group, Hughes Aircraft El Segundo, CA

Member of Technical Staff

- Involved in design of high speed digital ICs for the VHSIC (Very High Speed Integrated Circuit) program using Fairchild Fast-Z Fineline 1.25µm bipolar.
- Involved in design of high speed 64 X 16, 124 X 24, and 1K X 24 SRAM ICs.
- Contributed to the merged junction bipolar SPICE model.
- Designed current mode logic for UHSBL (Ultra High Speed Bipolar Logic) cell library in NS Aspect-III. Cells used in high speed MUX, DMUX, and DDS ICs.
- Developed digital IC architectures for high speed radar signal processing.

Education

1980-1985 UCLA Westwood, CA

- BS Electrical Engineering Summa Cum Laude, Phi Beta Kappa
- UCLA's Most Outstanding Senior Electrical Engineering Student

1985-1987 UCLA Westwood, CA

- MS Electrical Engineering

1987-1989 USC Los Angeles, CA

- Engineer's Degree Electrical Engineering

1990-Present USC Los Angeles, CA

- PHD Candidate under the advisement of Prof. John Choma Jr.
- Completed Thesis: "Nonlinear Error Correction for the Bipolar Canonic Cells."
- Designed, fabricated, and DC wafer probed amplifier circuits in MAXIM SHPi bipolar process to verify theory developed.

Publications

- M. Chambers and L. Linder, "A Precision Monolithic Sample- And-Hold for Video Analog-to-Digital Converters," ISSCC Feb. 1991.
- B. Felder, et al., "A Low Noise 13 Bit 10 MSPS ADC Hybrid with High Dynamic Range," GOMAC 1994.
- W. Cheng, et al., "A 3 Bit, 40GSPS ADC- DAC in 0.12µm SiGe," ISSCC Feb. 2004.
- O. Panfilov, et al., "Direct Conversion Transceivers as a Promising Solution for Building Future Ad-hoc Networks," International Conference on Next Generation Tele-traffic and Wired / Wireless Advanced Networking September 2007.
- O. Panfilov, et al., "Test Results of the Direct Conversion Transceiver Demo Board", November 2007 SDR Forum Technical Conference.

- O. Panfilov, et al., “Overcoming Challenges of Direct Conversion Software Radio,” IEEE International Design and Test Workshop December 2007.
- A. Varghese and L.F. Linder, “Software Defined Radios for Wireless Handsets,” April 2008 Wireless Design & Development Magazine.
- S. Elahmadi, et al., “A Monolithic One-Sample / Bit Partial-Response Maximum Likelihood SiGe Receiver for Electronic Dispersion Compensation of 10.7 GB / s Fiber Channels,” OFC / NFOEC March 2009.
- S. Elahmadi, et al., “A 50 dB Dynamic Range, 11.3 GSPS, Programmable Finite Impulse Response (FIR) Equalizer in 0.18μm SiGe BiCMOS Technology for High Speed Electronic Dispersion Compensation (EDC) Applications,” RFIC Symposium, June 2009.
- J. Edwards, et al., “A 12.5 Gbps Analog timing Recovery System for PRML Optical Receivers,” RFIC Symposium, June 2009.
- D. Baranauskas, et al., “A 6th Order 1.6 to 3.2 GHz Tunable Low-Pass Linear Phase gm-C Filter for Fiber Optic Adaptive EDC Receivers,” RFIC Symposium, June 2009.
- S. Elahmadi, et al., “An Analog PRML Receiver for up to 400km of Uncompensated OC-192 Fiber-Optic Channels,” ESSCIRC September 2009.
- S. Elahmadi, et al., "An 11.1 Gbps Analog PRML Receiver for Electronic Dispersion Compensation of Fiber Optic Communications," IEEE JSSC, vol.45, no. 7, July 2010.
- Montierth, D., Strans, T., Leatham, J., Linder, L., and Baker, R. J., "Performance and Characteristics of Silicon Avalanche Photo detectors in the C5 Process," 2012 IEEE Midwest Symposium on Circuits and Systems, Boise, Idaho.
- Rauch M. and Linder L., "Collaborating with Nu-Trek," 2012 HiRev Industry Day, December 2012, Los Angeles, California.

Awards / Achievements

- IEEE Senior Member
- Two-time Hughes Aircraft Division Patent Award winner
- 55 issued US patents, over 300 international patents, several US patents pending
- Numerous IC design team awards at Hughes and Raytheon
- Hughes Masters Fellow, Engineers Fellow, Doctoral Fellow
- 2008 IEEE San Fernando Valley Section Entrepreneurial Business Plan Competition Judge
- Menara Networks EDC IC Team Award – world’s first error free operation over 400 km of uncompensated fiber

IC Process Experience

- CMOS, silicon / SiGe bipolar, silicon / SiGe BiCMOS, complementary bipolar, CBiCMOS, SOI, SOS, GaAs D-mode / E-mode MESFET, AlGaAs / InP HBT

Skills

- CADENCE Analog Artist Schematic Composer, Spectre Simulator

Security Clearance

- Secret clearance is presently supported by Nu-Trek.
- US Citizen