IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF COLORADO

BELL SEMICONDUCTOR, LLC Plaintiff, v. PHISON ELECTRONICS, INC. Defendant.	Case No. 1:22-cv-2197 **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Bell Semiconductor, LLC ("Bell Semic" or "Plaintiff") brings this Complaint against Defendant PHISON Electronics, Inc. ("Phison") for infringement of U.S. Patent Nos. 7,149,989 ("the '989 patent") and 7,260,803 ("the '803 patent") (collectively the "Lakshmanan patents"). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1. This is a patent infringement suit relating to Phison's unauthorized and unlicensed use of the Lakshmanan patents. The metal design and insertion technologies claimed in the Lakshmanan patents are used by Phison in the production of one or more of its devices, including its PS2251-17-43.

2. Semiconductor devices include different kinds of materials to function as intended. For example, these devices typically include both metal (i.e., conductor) and insulator materials, which are deposited or otherwise processed sequentially in layers to form the final device. These layers—and the interconnects and components formed within them—have gotten much smaller

over time, increasing the performance of these devices dramatically. These devices have also become exceedingly more complex with increasing numbers of layers and increasingly smaller device features, all to enable increasingly faster devices operating at higher clock speeds. As a result, it has become more important to reduce the chance of short circuits and to keep the layers planar as the device is being built because defects and warpage can cause fabrication issues and malfunctioning of the device. Manufacturers use a process called Chemical Mechanical Planarization/Polishing ("CMP") to smooth out the surface of the device periodically between deposition and/or etching of each layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be "polished" away at different rates, leading to erosion or dishing on the surface. To reduce this problem "dummy" interconnect material, also known as "dummy fill," is typically inserted into low-density regions of the device to increase the overall uniformity of the structures on the surface of the layer and reduce the density variability across the surface of the device. Dummy fill is typically inserted by a dummy fill tool, which checks the metal density of the device and places dummy metal into regions that do not meet the metal density needed to minimize the likelihood that CMP processes causes the device to malfunction.

3. Prior to development of the methodology described in the '803 patent, if a designer requested even a small change to a semiconductor device, the dummy fill pattern must be thrown out. This is problematic because it can take up to 30 hours to run the dummy fill tool to create the dummy fill pattern. By starting over, the entire device design layout could be delayed by 30 hours or more. This issue is exacerbated with every subsequent change that again causes the dummy fill

process to begin again from scratch. Such an iterative, time-consuming process negatively impacts the fabrication schedule and causes costs to go up.

4. Viswanathan Lakshmanan, Richard Blinne, Vikram Shrowty, and Lena Montecillio ("the '803 Inventors"), the inventors of the '803 patent, understood the drawbacks of this process and set out to develop a more efficient method for inserting dummy metal into a circuit design after portion(s) of it have changed. The '803 Inventors ultimately conceived of a dummy fill insertion procedure that did not require having to rerun the dummy fill tool whenever any change was made to the layout. The claimed invention, after a portion of the design data has changed, first performs a check to determining whether any dummy metal objects intersect with any other objects in the design data. Then any intersecting dummy metal objects are deleted from the design data, thereby avoiding having to rerun the dummy fill tool.

5. The inventions disclosed in the '803 patent provide many advantages over the prior art. In particular, they provide a simple and efficient method for ensuring dummy metal does not intersect other components such that the dummy fill tool does not have to be rerun. *See* Ex. A at 2:6–22. As mentioned above, this is very beneficial as it substantially reduces the run time of the dummy fill tool, shortens the overall design timeline, and avoids cost overruns and delays, making it less costly to make changes later in the design process. *See* Ex. A at 1:51–65. Given the aforementioned increased complexity of circuit designs and the corresponding delays from ECOs and layout changes, these efficiency gains have become more and more important in completing the design process without affecting time-to-market. These significant advantages are achieved through the use of the patented inventions and thus the '803 patent presents significant commercial value for companies like Phison.

6. The ’989 patent addresses another way to minimize short circuits and malfunctioning devices. When creating a semiconductor device, designers typically create layout designs that contain the topological information used to identify structures within several layers of the semiconductor device. These layout designs are ultimately used as blueprints to create the physical semiconductor device. Prior to development of the methodology described in the ’989 patent, the designs would be validated at the very end of the design cycle, when all components have been placed and routed. However, if the validation process detects a design fault, like a short circuit, at the very end of the design cycle, then the timing of the entire integrated circuit design may have to be reset. In some cases, the design may have to be re-floorplanned and the entire design cycle may have to be reiterated, causing delays on of several weeks or months, depending on the overall complexity of the design and the process node. Similarly, it is not possible to simply run the validation check early in the process to avoid this issue. Doing so would cause the validation process to incorrectly identify a large number of errors because the circuit design is incomplete in early stages.

7. Viswanathan Lakshmanan, Alan Holesovsky, Lisa Miller, and Jonathan Kuppinger (“the ’989 Inventors”), the inventors of the ’989 patent, understood the drawbacks of both late stage and early stage validation processes and decided to create something better. The ’989 Inventors ultimately conceived of a validation procedure that specifies validation checks on certain physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground. The claimed invention receives a representation of an integrated circuit design and a physical design rule deck that specifies rule checks to be performed on the integrated circuit design. The claimed invention generates a specific rule deck from the physical design rule deck, where the specific rule deck is a subset that includes only physical design rules

that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design. A physical design validation is performed on the integrated circuit design from the specific rule deck to identify texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design.

8. The inventions disclosed in the ’989 patent provide many advantages over the prior art. In particular, they provide the ability to perform an early validation process that does not falsely identify a number of unfounded errors in the early stage of the design. *See* Ex. B at 2:47–58. For instance, in early stages, the patented process can identify violations in floorplanning, texted metal shorts, and errors in power map structure. *See* Ex. B at 2:64–3:7. Early defect detection saves computer processing time, avoids severe voltage droop, and allows for correction in early stages, each of which would otherwise result in costly schedule delays and unacceptable turnaround time. *See* Ex. B at 3:7–20. Moreover, this allows high-level power and signal-routing such that individual blocks with defined pins can be finalized by the responsible members of design team in parallel, at substantial decrease in design time and overall gains in efficiency. These significant advantages are achieved through the use of the patented inventions and thus the ’989 patent presents significant commercial value for companies like Phison.

9. Bell Semic brings this action to put a stop to Phison’s unauthorized and unlicensed use of the inventions claimed in the Lakshmanan patents.

THE PARTIES

10. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

11. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America's greatest technology incubators. Bell Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

12. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor–related inventions was developed over many years by some of the world's leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation ("LSI"). This portfolio reflects technology that underlies many important innovations in the development of semiconductors and integrated circuits for high–tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

13. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since those early days at Bell Labs. For example, Bell Semic's CTO was an LSI Fellow and Broadcom Fellow. He is known throughout the world as an innovator with more than 300 patents to his name, and he has a sterling reputation for helping semiconductor fabs improve their efficiency. Bell Semic's

CEO took a brief hiatus from the semiconductor world to work with Nortel Networks in the telecom industry during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees and employees. In addition, several Bell Semic executives previously served as engineers at many of these companies and were personally involved in creating the ideas claimed throughout Bell Semic's extensive patent portfolio.

14. On information and belief, Phison has its principal place of business and corporate headquarters at No. 1, Qunyi Rd., Zhunan Township, Miaoli, 35059 Taiwan. On information and belief, Phison develops, designs, and/or manufactures products in the United States, including in this District, according to the '803 and '989 processes/methodologies; and/or uses the '803 and '989 patented processes/methodologies in the United States, including in this District, to make products; and/or distributes, markets, sells, or offers to sell in the United States and/or imports products into the United States, including in this District, that were manufactured or otherwise produced using the patented process. Additionally, Phison introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

JURISDICTION AND VENUE

15. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

16. This Court has personal jurisdiction over Phison under the laws of the State of Colorado, due at least to its substantial business in Colorado and in this District. Phison has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of Colorado, and in this District by continuously and systematically placing

goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of Colorado and in this District, Phison, directly or through intermediaries: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the Lakshmanan patented process/methodology; (iii) distributes, markets, sells, or offers to sell products formed according to the Lakshmanan patented process/methodology; and/or (iv) imports products formed according to the Lakshmanan patented process/methodology.

17. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because Phison has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, Phison maintains a regular and established place of business, including an SSD Engineering Lab, at 329 Interlocken Parkway, Suite 250, Broomfield, CO 80021.

18. Currently, Phison is advertising four jobs in the Broomfield area. These positions include those that relate to the '803 and '989 patented technology, including two SSD Firmware Engineers, an SSD Test Engineer and Customer Firmware Project Manager. *See PhisonBlog Careers*, Phison (https://phisonblog.com/careers-us/) (last visited August 11, 2022). Moreover, on information and belief, Phison employs three engineers in Colorado. *See* Search Results for Current Phison Employees, LinkedIn (https://www.linkedin.com/search/results/people/?currentCompany=%5B%22784647%22%5D&geoUrn=%5B%22105763813%22%5D&heroEntityKey=urn%3Ali%3Aorganization%3A784647&keywords=phison%20electronics%20corps.%20&origin=FACETED_SEARCH&sid=_5q).

19. Venue is also convenient in this District. This is at least true because of this District's close ties to this case—including the technology, relevant witnesses, and sources of proof noted above—and its ability to quickly and efficiently move this case to resolution.

20. On information and belief, Bell Semic's cause of action arises directly from Phison's circuit design work and other activities in this District. Moreover, on information and belief, Phison has derived substantial revenues from its infringing acts occurring within the State of Oregon and within this District.

U.S. PATENT NO. 7,149,989

21. Bell Semic is the owner by assignment of the '989 patent. The '989 patent is titled "Method of Early Physical Design Validation and Identification of Texted Metal Short Circuits in an Integrated Circuit Design." The '989 patent issued on December 12, 2006. A true and correct copy of the '989 patent is attached as Exhibit B.

22. The inventors of the '989 patent are Viswanathan Lakshmanan, Alan Holesovsky, Lisa Miller, and Jonathan Kuppinger.

23. The application that resulted in the issuance of the '989 patent was filed on September 22, 2004. The '989 patent claims priority to September 22, 2004.

24. The '989 patent generally relates to "methods of verifying an integrated circuit design to ensure adherence to process rules and overall manufacturability of the integrated circuit design for a specific technology." Ex. B at 1:10–15.

25. The '989 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior validation methodology was disadvantageous because "a design fault detected so late might reset the time schedule for the entire integrated circuit design." Ex. B at 2:42–44. In some cases, this means the "design may have to be re-floorplanned, and the

entire design cycle may have to be reiterated." Ex. B at 2:44–46. Existing early design validation processes resulted in "substantial amount[s] of computer processing time that would severely impact the product turnaround time." Ex. B at 2:50–54. In addition, it would "falsely report" a large number of design errors "due to the incomplete circuit design, making it difficult to sort out the design errors that need to be corrected before the circuit design is completed." Ex. B at 2:54–58.

26. In light of the drawbacks of the prior art, the Inventors recognized the need to "provide[] design rules that may be used in conjunction with a design rule check tool and/or a layout vs. schematic tool in an early stage of the physical design to detect design rule violations in floorplanning, including input/output cell placement and construction and power distribution and power map structure." Ex. B at 2:64–3:3. Moreover, "texted metal short circuits may be identified most advantageously in the early or evolutionary aspects of the design flow," which reduc[es] the computer processing time required to validate an integrated circuit design," such as once layout design is complete. Ex. B at 3: 3–11. The inventions claimed in the '989 patent address this need.

27. The '989 patent contains two independent claims and 12 total claims, covering a method and computer program product. Claim 1 reads:

> 1. A method comprising the steps of:
>
> (a) receiving as input a representation of an integrated circuit design;
>
> (b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design;
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> (c) generating a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design; and

> (d) performing a physical design validation on the integrated circuit design from the specific rule deck to identify texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design.

28. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, minimizing the potential for design-based short circuits, ensuring overall manufacturability of devices, reducing probability of failure, and ultimately lessening the likelihood of defective devices. *See, e.g.*, Ex. B at 1:11–15; 3:3–19.

29. The claims of the ’989 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly validation processes. The claims of the ’989 patent disclose a new and novel solution to specific problems related to end-stage validation. As explained in detail above and in the ’989 patent specification, the claimed inventions improve upon the prior art processes by performing early-stage validation on texted metal short circuits. This has the advantage of ensuring manufacturability of devices, lessening the likelihood of short circuits and other defects, as well as substantially reducing the time needed to finalize a circuit design. This allows high-level power and signal-routing such that individual blocks with defined pins can be finalized by the responsible members of design team in parallel, at substantial decrease in design time and overall gains in efficiency.

U.S. PATENT NO. 7,260,803

30. Bell Semic is the owner by assignment of the ’803 patent. The ’803 patent is titled “Incremental Dummy Metal Insertions.” The ’803 patent issued on August 21, 2007. A true and correct copy of the ’803 patent is attached as Exhibit A.

31. The inventors of the ’803 patent are Viswanathan Lakshmanan, Richard Blinne, Vikram Shrowty, and Lena Montecillo.

32. The application that resulted in the issuance of the '803 patent was filed on October 10, 2003. The '803 patent claims priority to October 10, 2003.

33. The '803 patent generally relates to "a method for performing dummy metal insertion that avoids having to rerun the dummy fill software tool after the integrated circuit design is changed." Ex. A at 1:6–10.

34. The '803 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior dummy fill methodologies were disadvantageous because, when a customer requests a change, "the results of the dummy fill tool are thrown out, and the dummy fill tool is rerun in order to ensure that no dummy metal intersects with any of the design objects." Ex. A at 1:51–59. Unfortunately, this "may delay completion of the design by another 30 hours" and may "significantly impact the design schedule and result in cost overruns. Ex. A at 1:60–65. This is especially true when multiple changes are requested.

35. In light of the drawbacks of the prior art, the Inventors recognized the need to "insert[] dummy metal into an integrated circuit design after an ECO [Engineering Change Order] without requiring reruns of the dummy fill tool." Ex. A at 1:66–2:1. This "saves time on overall design execution" and helps manufacturers "meet aggressive design schedules." Ex. B at 2:15–22; 4:52–57. The inventions claimed in the '803 patent address this need.

36. The '803 patent contains two independent claims and 22 total claims, covering a method and computer readable medium for performing dummy metal insertion. Claim 1 reads:

> 1. A method for performing dummy metal insertion in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool, comprising:
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> > (a) after a portion of the design data is changed, performing a check to determine whether any dummy metal objects intersect with any other objects in the design data; and

(b) deleting the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool.

37. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, minimizing the potential for design-based short circuits, increasing the efficiency of the design process, and ensuring that devices meet their minimum density requirements, which reduces the probability of short circuits or other defects that render devices inoperable. *See, e.g.*, Ex. A at 1:24–42.

38. The claims of the ’803 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly dummy fill processes. The claims of the ’803 patent disclose a new and novel solution to specific problems related to rerunning dummy fill tools after a change order is received. As explained in detail above and in the ’803 patent specification, the claimed inventions improve upon the prior art processes by deleting dummy metal objects if a change order results in dummy metal objects that intersect with other objects in the design data. This has the advantage of maintaining minimum metal density without having to rerun the dummy fill tool, and results in substantially reducing the time needed to finalize a circuit design due to the ability to make late-stage ECOs and incremental changes in layout without needing to re-run the dummy fill tool for the entire layer.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,149,989

39. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

40. The ’989 patent is valid and enforceable under the United States Patent Laws.

41. Bell Semic owns, by assignment, all right, title, and interest in and to the ’989 patent, including the right to collect for past damages.

42. A copy of the ’989 patent is attached at Exhibit B.

43. On information and belief, Phison has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’989 patent by using the patented methodology to design one or more devices, including as one example the PS2251-17-43, in the United States.

44. On information and belief, Phison employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to validate its circuit designs (the “Accused Processes”) as recited in the ’989 patent claims. As one example, Phison’s Accused Processes perform a method that receives as input a representation of an integrated circuit design as required by claim 1 of the ’989 patent. Phison does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, into which a circuit design for its PS2251-17-43 is imported.

45. Phison’s Accused Processes also receive as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design. Phison does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, that receives various in-design verification processes for concurrent physical design and verification of the PS2251-17-43’s circuit designs.

46. Phison’s Accused Processes also generate a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design. Phison does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, that includes a “short finder,” “short locator,” or similar functionality that identifies texted metal short circuits. For example, the Accused Processes allow designers to select texted metal short circuits, which are shown by cell, text, net, layer and position. The nets may include ground, power, and other signal nets. An exemplary infringement analysis showing infringement of one or more claims of the ’989 patent is set forth in Exhibit D. The

declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit E and further describes Phison's infringement of the '989 patent.

47. Phison's Accused Processes infringe and continue to infringe one or more claims of the '989 patent during the pendency of the '989 patent.

48. On information and belief, Phison has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the '989 patent. Phison has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the '989 patent.

49. Phison's infringement of the '989 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

50. Bell Semic has been damaged by Phison's infringement of the '989 patent and will continue to be damaged unless Phison is enjoined by this Court. Bell Semic has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

51. Bell Semic is entitled to recover from Phison all damages that Bell Semic has sustained as a result of Phison's infringement of the '989 patent, including without limitation and/or not less than a reasonable royalty.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 7,260,803

52. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

53. The ’803 patent is valid and enforceable under the United States Patent Laws.

54. Bell Semic owns, by assignment, all right, title, and interest in and to the ’803 patent, including the right to collect for past damages.

55. A copy of the ’803 patent is attached at Exhibit A.

56. On information and belief, Phison has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’803 patent by using the patented methodology to design one or more devices, including as one example the PS2251-17-43, in the United States.

57. On information and belief, Phison employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to delete intersecting dummy metal objects from its circuit designs (the “Accused Processes”) as recited in the ’803 patent claims. As one example, Phison’s Accused Processes perform a method of dummy metal insertion in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool as required by claim 1 of the ’803 patent. Phison does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, that performs this dummy metal process for its PS2251-17-43 layout. The PS2251-17-43 includes dummy metal objects inserted by a dummy fill tool, such as an “integrated” or “in-design” flow.

58. After a portion of the design data is changed, Phison’s Accused Processes perform a check to determine whether any dummy metal objects intersect with any other objects in the design data. When Phison receives an Engineering Change Order (“ECO”), it employs a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to perform a Design Rule Check (“DRC”) to determine whether there are any rule violations, including those related to metal fill geometries and layout changes, in the PS2251-17-43’s design data.

59. Phison's Accused Processes also delete the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool. Phison does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, that repairs DRC violations associated with shorts caused by dummy fill geometries intersecting with other objects in the design data. For example, the Accused Processes allow designers to trim metal fill geometries that cause the short or DRC violation. An exemplary infringement analysis showing infringement of one or more claims of the '803 patent is set forth in Exhibit C. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit E and further describes Phison's infringement of the '803 patent.

60. Phison's Accused Processes infringe and continue to infringe one or more claims of the '803 patent during the pendency of the '803 patent.

61. On information and belief, Phison has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the '803 patent. Phison has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the '803 patent.

62. Phison's infringement of the '803 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

63. Bell Semic has been damaged by Phison's infringement of the '803 patent and will continue to be damaged unless Phison is enjoined by this Court. Bell Semic has suffered and

continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

64. Bell Semic is entitled to recover from Phison all damages that Bell Semic has sustained as a result of Phison's infringement of the '803 patent, including without limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

a) a judgment declaring that Phison has infringed one or more claims of the Lakshmanan patents in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;

b) an award of damages adequate to compensate Bell Semic for infringement of the Lakshmanan patents by Phison, in an amount to be proven at trial, including supplemental post-verdict damages until such time as Phison ceases its infringing conduct;

c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting Phison and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with Phison, from committing further acts of infringement;

d) a judgment requiring Phison to make an accounting of damages resulting from Phison's infringement of the Lakshmanan patents;

e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;

f) pre-judgment and post-judgment interest at the maximum amount permitted by law;

g) all other relief, in law or equity, to which Bell Semic is entitled.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: August 26, 2022

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*Application for Admission Forthcoming

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