IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC. Plaintiff, v. **MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS LLC,** Defendants.	)	JURY TRIAL DEMANDED

COMPLAINT

1. Plaintiff Netlist, Inc. ("Netlist"), by its undersigned counsel, for its Complaint against defendants Micron Technology Inc. ("Micron Technology"), Micron Semiconductor Products, Inc. ("Micron Semiconductor"), and Micron Technology Texas, LLC ("Micron Texas") (collectively, "Micron" or "Defendants"), states as follows, with knowledge as to its own acts, and on information and belief as to the acts of others:

2. This action involves six of Netlist's patents: U.S. Patent Nos. 10,860,506 (the "'506 Patent," Ex. 1), 10,949,339 (the "'339 Patent," Ex. 2), 11,016,918 (the "'918 Patent," Ex. 3), 11,232,054 (the "'054 Patent," Ex. 4), 8,787,060 (the "'060 Patent," Ex. 5), and 9,318,160 (the "'160 Patent," Ex. 6) (collectively, the "Patents-in-Suit").

I. THE PARTIES

3. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Drive, Suite 100, Irvine, CA 92617.

4. On information and belief, Micron makes dynamic random-access memory ("DRAM"), NAND Flash, and NOR Flash memory, and other memory products in semiconductor fabrication plants in the United States and other countries throughout the world. On information and belief, Micron sells its products to customers, including customers in this District, in the computer, networking and storage, consumer electronics, solid-state drives and mobile telecommunications markets.

5. On information and belief, Micron Technology is a corporation organized and existing under the laws of Delaware. On information and belief, Micron Technology has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Technology is registered to do business in the State of Texas, and can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

6. On information and belief, Micron Semiconductor is a corporation organized and existing under the laws of Idaho. On information and belief, Micron Semiconductor has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Semiconductor is registered with the Texas Secretary of State to do business in Texas. On information and belief, Micron Semiconductor can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

7. On information and belief, Micron Texas is a corporation organized and existing under the laws of Idaho. On information and belief, Micron Texas has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Texas also has a regular and established place of business at 950 West Bethany Drive, Suite 120, Allen, Texas 75013-3837. On information and belief, Micron Texas is registered with the Texas Secretary of State to do business in Texas. On information and belief, Micron Texas can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas, 78701-3218.

8. On information and belief, Micron Semiconductor and Micron Texas are wholly owned subsidiaries of Micron Technology. On information and belief, Micron Technology does not separately report revenue from Micron Semiconductor or Micron Texas in its filings to the Securities Exchange Commission, but rather reports combined revenue from its various products and subsidiaries.

9. On information and belief, Defendants have semiconductor fabrication plants in the United States and other countries throughout the world and manufacture memory products such as DRAM, NAND Flash, and NOR Flash at those plants. On information and belief, Defendants also use, sell, and offer for sale in the United States, import into the United States and/or export from the United States memory products, including DDR4 load reduced dual in-line memory modules ("LRDIMMs"), DDR5 dual in-line memory modules ("DIMMs"), HBM2E memory components, and other high bandwidth memory products and components, or unfinished versions thereof ("Accused Instrumentalities"). On information and belief, Defendants have at least used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district, *e.g.*, through sales and distribution channels managed by Micron Texas.

10. On information and belief, Defendants place, have placed, and contributed to placing Accused Instrumentalities into the stream of commerce via an established distribution channel knowing or understanding that such products would be sold and used in the United States, including in this judicial district. On information and belief, Defendants have also derived substantial revenues from infringing acts in this judicial district, including from the sale and use of the Accused Instrumentalities.

II. JURISDICTION AND VENUE

11. The Court has subject matter jurisdiction under 28 U.S.C. § 1338, in that this action arises under federal statute, the patent laws of the United States (35 U.S.C. §§ 1, *et seq.*).

12. Each Defendant is subject to this Court's personal jurisdiction consistent with the principles of due process and/or the Texas Long Arm Statute.

13. Personal jurisdiction exists generally over the Defendants because each Defendant has sufficient minimum contacts and/or has engaged in continuous and systematic activities in the forum as a result of business conducted within the State of Texas and the Eastern District of Texas. Personal jurisdiction also exists over each Defendant because each, directly or through subsidiaries, makes, uses, sells, offers for sale, imports, advertises, makes available, and/or markets products within the State of Texas and the Eastern District of Texas that infringe one or more claims of the Patents-in-Suit. Further, on information and belief, Defendants have placed or contributed to placing infringing products into the stream of commerce knowing or understanding that such products would be sold and used in the United States, including in this District.

14. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b) because Defendants (1) have committed and continue to commit acts of patent infringement in this District by, among other things, directly and/or indirectly making, using, selling, offering to sell, or importing products that infringe one or more claims of the Patents-in-

Suit, and (2) have done and continue to do business in this District by maintaining regular and established places of business, including at least at 805 Central Expressway South, Suite 100, Allen, Texas 75013.

III. FACTUAL ALLEGATIONS

Background

15. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

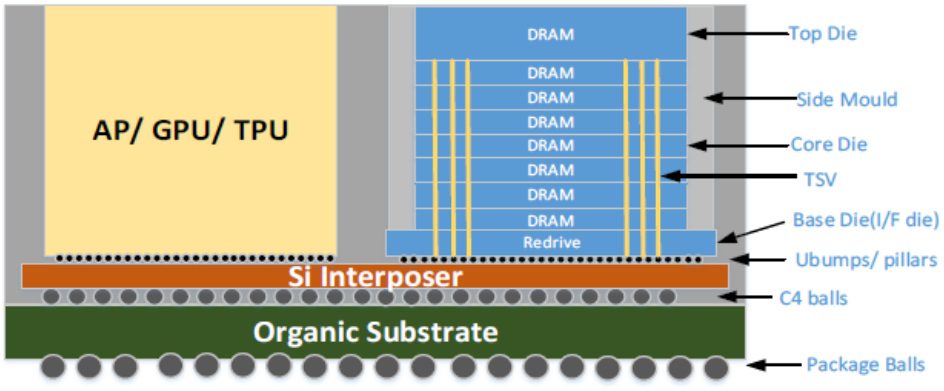
16. Netlist has a long history of being the first to market with disruptive new products such as the first LRDIMM, HyperCloud®, based on Netlist's distributed buffer architecture later adopted by the industry for DDR4 LRDIMM. Netlist was also the first to bring NAND flash to the memory channel with its NVvault® NVDIMM. These innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate ("DDR") technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory.

17. In many commercial products, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard.

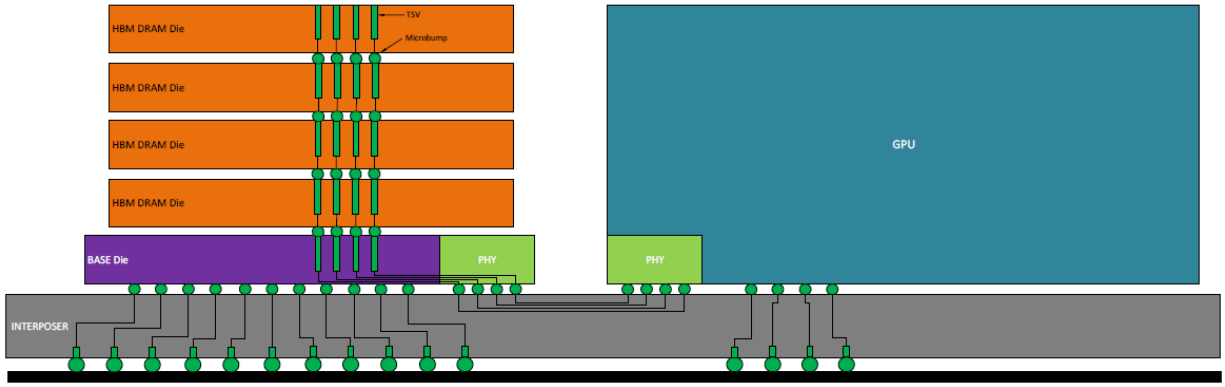
18. Memory modules are designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications (e.g. scaled data manipulation and aggregation, on-demand tracking, AI-based image analysis, weather patterning, etc.). The structure, function, and operation of memory modules is defined, specified, and standardized by the JEDEC Solid State Technology Association ("JEDEC"), the standard-setting body for the microelectronics industry. Memory modules are typically characterized by, among other things, the generation of DRAM on the module (*e.g.*, DDR5, DDR4, DDR3) and the type of module (*e.g.*, RDIMM, LRDIMM).

19. High bandwidth memory ("HBM") is a type of high-speed computer memory technology that relies in part on vertically stacked memory dies. In end products incorporating HBMs, a memory host such as a CPU and/or GPU is interconnected to a logic/driver/buffer die at the bottom of each memory die stack. The combined system of CPU/GPU and the memory stack is then mounted on a substrate for use, as illustrated below. This format substantially shortens the signal length between the host and the memory, which enables shorter communication time, smaller format, higher performance and lower power consumption.

Micron Technical Brief



Ex. 9 (Micron Technical Brief "Integrating and Operating HBM2E Memory") at 3 (annotations in original); *see also, e.g.*, Ex. 11 (Micron white paper titled "The Demand for High-Performance Memory") at 2:



High-bandwidth memory leverages stacked memory components for density and high I/O counts

The Asserted Netlist Patents

The '506 Patent

20. The '506 Patent is entitled "Memory Module With Timing-Controlled Data Buffering." Netlist owns the '506 Patent by assignment from the listed inventors Hyun Lee and Jayesh R. Bhakta. The '506 Patent was filed as Application No. 16/391,151 on April 22, 2019, issued as a patent on December 8, 2020, and claims priority to, among others, a utility application filed on July 27, 2013 (No. 13/952,599) and a provisional application filed on July 27, 2012 (No. 61/676,883).

21. Micron has had actual knowledge of the '506 Patent no later than April 28, 2021 via Exhibit A to Netlist's April 28, 2021 letter to Micron, and as of the filing of this Complaint.

22. As described in the '506 Patent, in conventional memory modules, the "distribution of control signals and a control clock signal in the memory module is subject to strict constraints" to ensure that memory devices on the memory module can be properly accessed. Ex. 1 at 2:18-20. For example, in some conventional memory modules, "control wires are routed so there is an equal length to each memory component, in order to eliminate variation of the timing of the control

signals and the control clock signal between different memory devices in the memory modules." *Id.* at 2:20-24. But as noted in the '506 Patent, "[t]he balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections." *Id.* at 2:24-27. In yet other conventional memory systems, the memory controller includes mechanisms such as read or write leveling for compensating for unbalanced wire lengths on the memory module. *Id.* at 2:28-32. However, with increasing memory operating speed and memory density "such leveling mechanisms are also insufficient to ensure proper timing of the control and/or data signals received and/or transmitted by the memory modules." *Id.* at 2:32-36.

23. The '506 Patent discloses a memory module operable in a memory system with a memory controller that includes memory devices, a module control circuit, and a plurality of buffer circuits coupled between respective sets of data signal lines in a data bus and respective sets of the memory devices. As summarized in the Abstract, "[e]ach respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal. Each respective buffer circuit includes a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals." *Id.*, Abstract.

24. The buffer circuits (118, highlighted below) are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective groups of memory devices as illustrated in the exemplary configuration of Figure 2A.

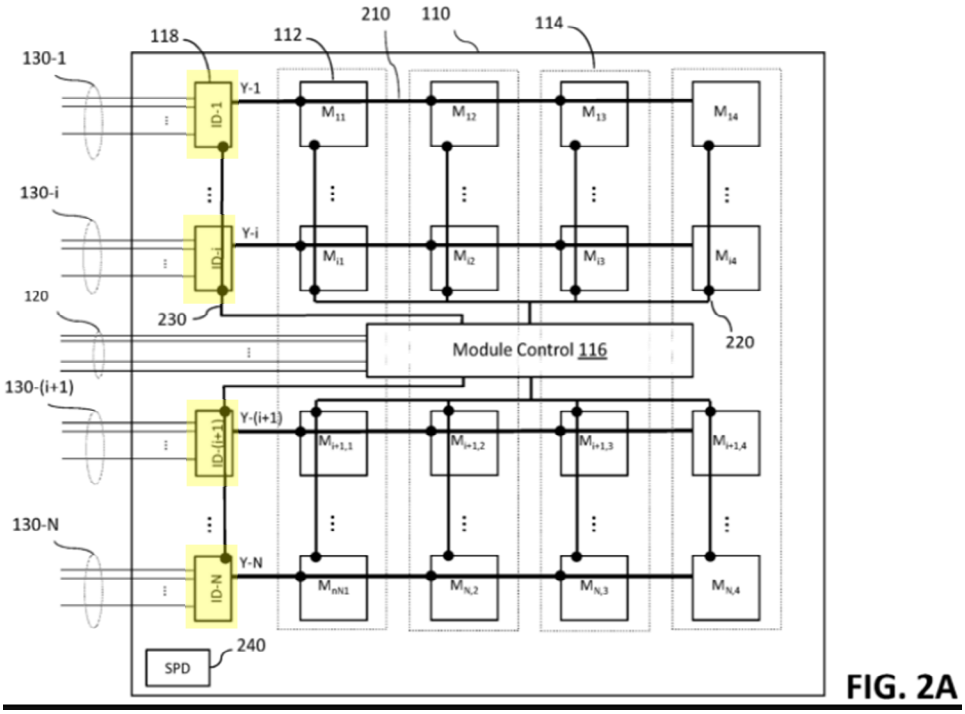


FIG. 2A

25. However, because the buffer circuits—or "isolation devices"—are distributed across the memory module, at high speeds of operation, the same set of module control signals sent by the module control circuit in the module may reach different buffer circuits at different times across one cycle of the system clock. *Id.* at 9:51-62 ("Because the isolation devices 118 are distributed across the memory module 110, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines 230 from the module control device 116 to the farthest positioned isolation devices 118, such as isolation device ID-1 and isolation device ID-(n−1) in the exemplary configuration shown in FIG. 2."). The '506 Patent discloses an embodiment wherein "each isolation devices includes signal alignment circuits that determine, during a write operation, a time

interval between a time when one or more module control signals are received from the module control circuit 116 and a time when a write strobe or write data signal is received from the MCH 101. This time interval is used during a subsequent read operation to time the transmission of read data to the MCH 101, such that the read data follows a read command by a read latency value associated with the system 100." *Id.* at 10:11-21.

The '339 Patent

26. The '339 Patent is entitled "Memory Module With Controlled Byte-Wise Buffers." Netlist owns the '339 Patent by assignment from the listed inventors Hyun Lee and Jayesh R. Bhakta. The '339 Patent was filed as Application No. 15/470,856 on March 27, 2017, issued as a patent on March 16, 2021, and claims priority to U.S. Patent Application No. 12/504,131 filed on July 16, 2009, U.S. Patent Application No. 12/761,179 filed on April 15, 2010 and U.S. Application No. 13/970,606 filed on August 20, 2013.

27. Micron has had actual knowledge of the '339 Patent no later than April 28, 2021 via Exhibit A to Netlist's April 28, 2021 letter to Micron, and as of the filing of this Complaint.

28. As described in the '339 Patent, in optimizing performance of memory subsystems (e.g. memory modules) "consideration is always given to memory density, power dissipation (or thermal dissipation, speed, and cost." Ex. 2 at 2:5-7. The '339 Patent further explains that "[g]enerally, these attributes are not orthogonal to each other, meaning that optimizing one attribute may detrimentally affect another attribute. For example, increasing memory density typically causes higher power dissipation, slower operational speed, and higher costs." *Id.* at 2:7-12. The '339 Patent is generally directed to a memory module optimized to reduce the load experienced by a system memory controller via the use of configurable data transmission circuits.

29. The '339 Patent discloses a memory module configured to communicate with a memory controller that includes DDR DRAM devices arranged in multiple ranks each of the same

width as the memory module, and a module controller configured to receive and register input control signals for a read or write operation from the memory controller and to output registered address and control signals. As summarized in the Abstract, "[t]he registered address and control signals selects one of the multiple ranks to perform the read or write operation. The module controller further outputs a set of module control signals in response to the input address and control signals. The memory module further comprises a plurality of byte-wise buffers controlled by the set of module control signals to actively drive respective byte-wise sections of each data signal associated with the read or write operation between the memory controller and the selected rank." *Id.*, Abstract.

30. Figure 3A illustrates an example of a memory subsystem consistent with embodiments disclosed in the '339 Patent.

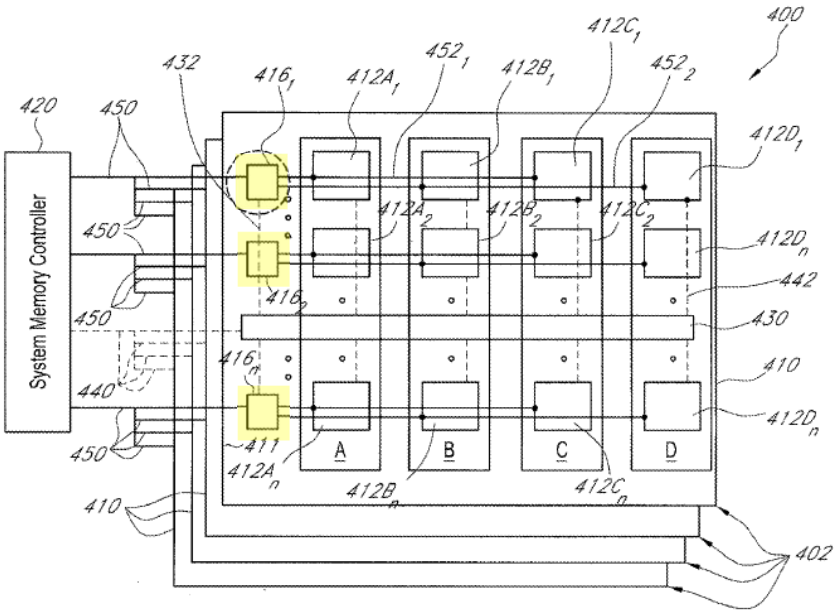


FIG. 3A

31. As shown above, Figure 3A depicts a memory subsystem 400 including memory modules 402 comprising memory devices 412, data transmission circuits 416 (highlighted above), and module control circuits 430. The data transmission circuits 416 operate to reduce the load

experienced by the memory controller 420 to improve performance of a read or write operation. *Id.* at 17:14-44 ("Referring again to FIG. 3A, when the memory controller 420 executes read or write operations, each specific operation is targeted to a specific one of the ranks A, B, C, and D of a specific memory module 402. The data transmission circuit 416 on the specifically targeted one of the memory modules 402 functions as a bidirectional repeater/multiplexor, such that it drives the data signal when connecting from the system memory controller 420 to the memory devices 412. The other data transmission circuits 416 on the remaining memory modules 402 are disabled for the specific operation. . . . Thus, the memory controller 420, when there are four four-rank memory modules, sees four load-reducing switching circuit loads, instead of sixteen memory device loads. The reduced load on the memory controller 420 enhances the performance and reduces the power requirements of the memory system . . . ."). In certain embodiments, "the data transmission circuit 416 comprises or functions as a byte-wise buffer. In certain such embodiments, each of the one or more data transmission circuits 416 has the same bit width as does the associated memory devices 412 per rank to which the data transmission circuit 416 is operatively coupled." *Id.* at 13:31-36.

The '918 Patent

32. The '918 Patent is entitled "Flash-DRAM Hybrid Memory Module." Netlist owns the '918 Patent by assignment from the listed inventors Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta. The '918 Patent was filed as Application No. 17/138,766 on December 30, 2020, issued as a patent on May 25, 2021, and claims priority to, among others, U.S. Application No. 13,559,476 filed on July 26, 2012; U.S. Application No. 12/240,916 filed on September 29, 2008; U.S. Application No. 12/131,873 filed on June 2, 2008; as well as to two provisional applications, filed on June 1, 2007 (No. 60/941,586) and July 28, 2011 (No. 61/512,871).

33. Micron has had actual knowledge of the '918 Patent since at least the filing of this Complaint.

34. As summarized in the Abstract, the '918 Patent discloses a memory module that includes a printed circuit board with an interface that couples it to a host system for provision of power, data, address and control signals, and additionally features "[f]irst, second, and third buck converters [that] receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage." Ex. 3, Abstract.

35. The '918 Patent discloses, *inter alia*, a power module that provides power to various components of the memory system as depicted in Figure 16, shown below.

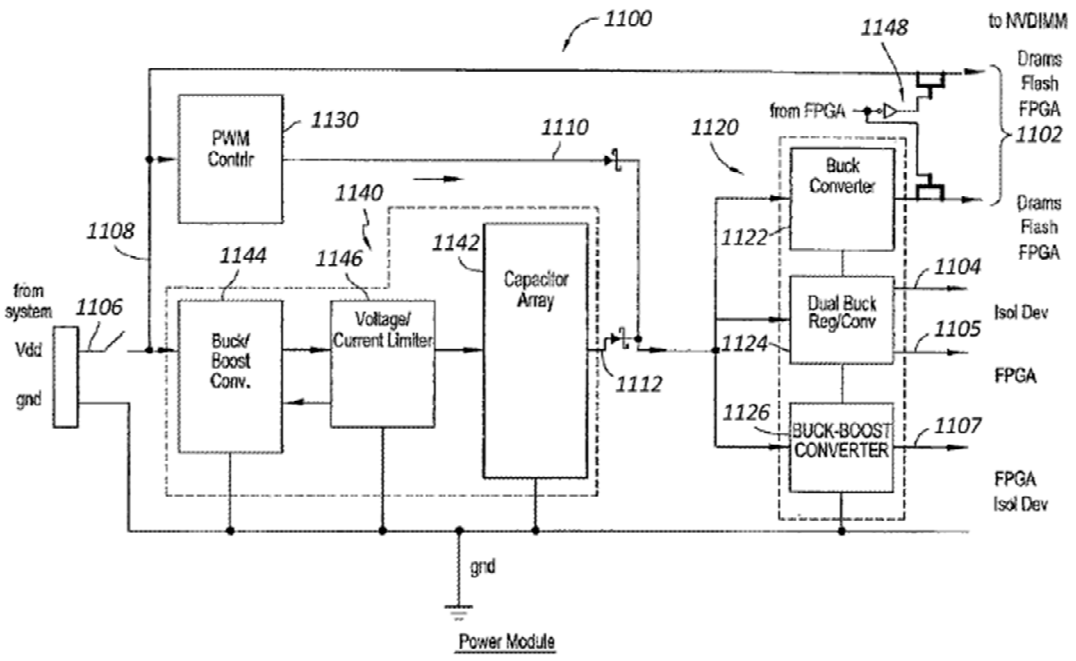


FIG. 16

36. The '918 Patent explains that "[t]he power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller." *Id.* at 28:3-15. "The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters." *Id.* at 29:18-19.

37. The '918 Patent also provides for voltage monitor circuit that, in response to detected over-voltage or under-voltage conditions, produces a trigger signal, which may in turn cause a logic element to write information into a non-volatile memory that is configured to store configuration information. *See*, *e.g.*, *id.* at 38:61-39:5, 39:23-36. As explained in the '918 Patent, in certain embodiments, "the non-volatile memory subsystem 1040 may backup the volatile memory subsystem 1030 in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system," or where "the memory system 1010 detects that the system voltage is below [or above] a certain threshold voltage," *e.g.* ten percent below or above a specified operating voltage. *See, e.g.*, *id.* at 24:9-32, 39:6-8, 39:19-22.

38. This design represents a fundamental and innovative departure from prior generations of DDR modules for which the voltage regulation was provided by power management units located on motherboards, external to the DDR modules. In contrast, the '918 Patent (as well as its continuation, the '054 Patent, discussed below), moves the voltage regulation and many other

power management functions into the DDR modules themselves, therefore allowing for more precise and accurate regulation of voltages and more efficient power management.

39. The inventions of the '918 Patent provide for the effective operation of DDR5 memory modules, by enabling, among other benefits, greater power efficiency than previous generations of DDR technology. The DDR5 standard is characterized by the use of an on-module power management system.

The '054 Patent

40. The '054 Patent is entitled "Flash-DRAM Hybrid Memory Module." Netlist owns the '054 Patent by assignment from the listed inventors Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta. The '054 Patent was filed as Application No. 17/328,019 on May 24, 2021, issued as a patent on January 25, 2022, and claims priority to, among others, U.S. Application No. 13,559,476 filed on July 26, 2012; U.S. Application No. 12/240,916 filed on September 29, 2008; U.S. Application No. 12/131,873 filed on June 2, 2008; as well as to two provisional applications, filed on June 1, 2007 (No. 60/941,586) and July 28, 2011 (No. 61/512,871).

41. Defendants have had actual knowledge of the '054 Patent since at least the filing of this Complaint.

42. As summarized in the Abstract, the '054 Patent discloses a memory module that includes a printed circuit board with an interface that couples it to a host system for provision of power, data, address and control signals, and additionally features "[f]irst, second, and third buck converters [that] receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage

monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage." Ex. 4, Abstract.

43. The '054 Patent discloses, *inter alia*, a power module that provides power to various components of the memory system as depicted in Figure 16, shown below.

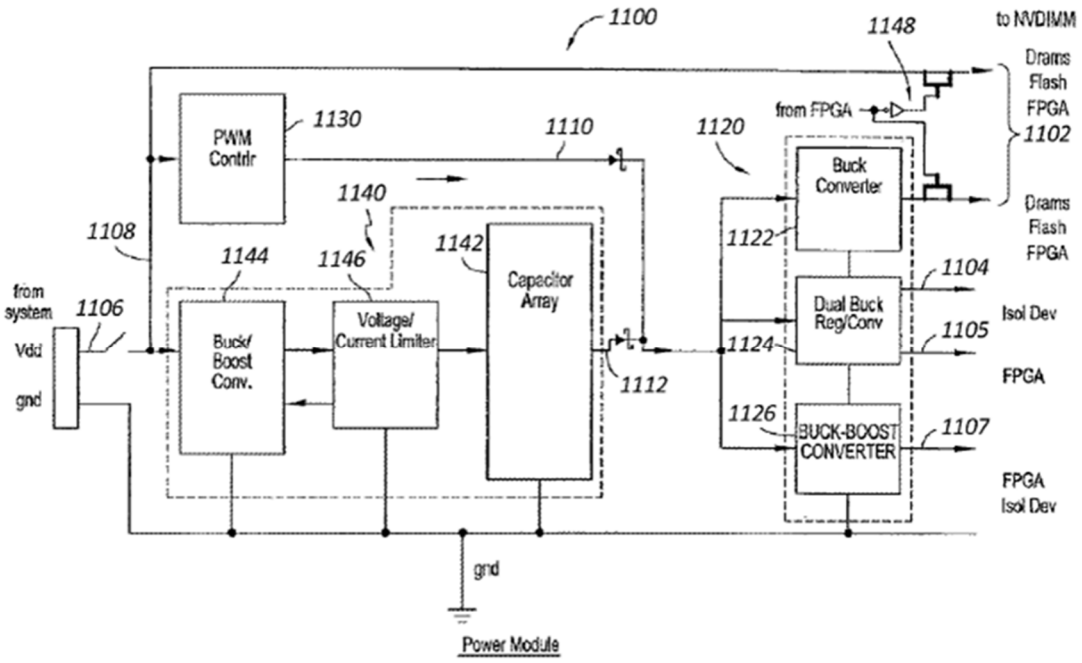


FIG. 16

44. Like the inventions of the '918 Patent, the inventions of the '054 Patent provide for the effective operation of DDR5 memory modules, by enabling, among other benefits, greater power efficiency than previous generations of DDR technology. *See supra*, ¶¶ 36-39.

The '060 and '160 Patents

45. The '060 Patent is entitled "Method and Apparatus for Optimizing Driver Load in a Memory Package." Netlist owns the '060 Patent by assignment from listed inventor Hyun Lee. The '060 Patent was filed as Application No. 13/288,850 on November 3, 2011, issued as a patent on July 22, 2014, and claims priority to a provisional application filed on November 3, 2010 (No. 61/409,893).

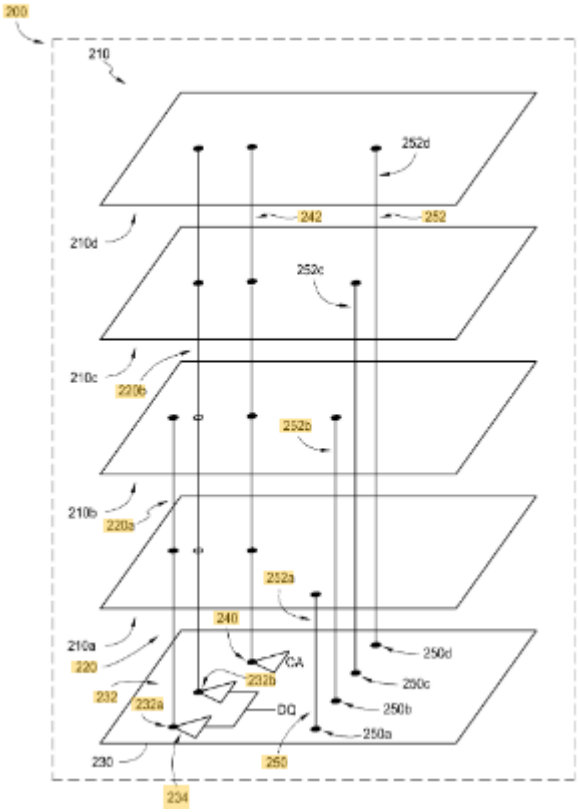
46. The ’160 Patent is a continuation of the ‘060 patent and is entitled “Memory Package with Optimized Driver Load and Method of Operation.” Netlist owns the ’160 Patent by assignment from listed inventor Hyun Lee. The ’160 Patent was filed as Application No. 14/337,168 on July 21, 2014, issued as a patent on April 19, 2016, and claims priority to, among others, a utility application filed on November 3, 2011 (No. 13/288,850, which issued as the ‘060 patent) and a provisional application filed on November 3, 2010 (No. 61/409,893).

47. Defendants have had actual knowledge of the ’060 and ’160 Patents since at least the filing of this Complaint.

48. The ’060 and ’160 Patents disclose systems and methods for optimizing a load in a memory package featuring a control die, array dies, and numerous die interconnects. In contrast to traditional DDR modules in which different DRAM devices are packaged individually and then assembled on a common printed circuit boards, the inventions of the ’060 and ’160 Patents are directed to DDR packages each having multiple vertically stacked DRAM devices interconnected to a common control circuit, all packaged in the same package.

49. For example, as summarized in the Abstract, the memory package features at least two die interconnects, where “[t]he first die interconnect is in electrical communication with a data port of a first array die and a data port of a second array die and not in electrical communication with data ports of a third array die. The second die interconnect is in electrical communication with a data port of the third array die and not in electrical communication with data ports of the first array die and the second array die.” Ex. 5, Abstract; Ex. 6, Abstract. The memory package’s control die includes “a first data conduit configured to transmit a data signal to the first die interconnect and not to the second die interconnect, and at least a second data conduit configured to transmit the data signal to the second die interconnect and not to the first die interconnect.” *Id.*

50. The ’060 and ’160 Patents explain that in conventional memory packages, the die interconnects are in communication with ***each*** of the array dies, which disadvantageously increases the load on the data conduit. Ex. 5, at 11:32-40. To address this problem, the ’060 and ’160 Patents disclose memory packages with multiple die interconnects in electrical communication with ***some***, but not all of the array dies, as illustrated below. *Id.* at 5:46-6:36.



51. As the ’060 and ’160 Patents explain, in the disclosed memory packages “[e]ach of these die interconnects 320 may be coupled to, or in electrical communication with at least one port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 ***without being in electrical communication with a port from at least one array die 310***, which may be in electrical communication with a different die interconnect 320. *Id.* at 5:54-62 (emphasis added). This enables the memory packages to be designed with smaller form factor in mind, and lowers power consumption. *See id.* at 7:22-8:62.

Micron's Infringing Activities

52. Defendants are worldwide semiconductor solution providers that primarily manufacture semiconductor memory products such as DRAM, DIMMs, and MCP (Multi-Chip Package), such as HBM. Defendants develop, manufacture, sell, offer to sell, import into the United States and export from the United States memory components and memory modules (including semi-finished ones) designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications as well as for use in consumer end products.

53. Netlist contacted Micron by letter dated April 28, 2021 requesting that it take a license; Micron has declined to take a license.

DDR4 Memory Modules

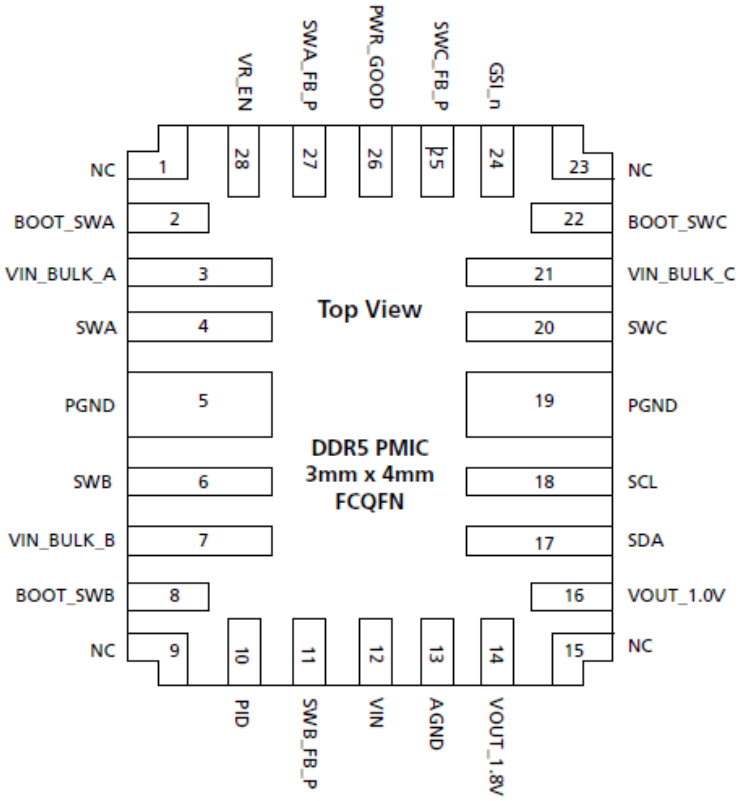
54. The accused DDR4 products include, without limitation, any Micron DDR4 LRDIMM products made in, sold in, offered for sale in, used in, exported from and/or imported into the United States by Micron. By way of non-limiting example, the accused DDR4 LRDIMM products include Micron products advertised on Micron's website. *See* Micron Technologies, DRAM Modules, *available at* https://www.micron.com/products/dram-modules. By way of non-limiting example, the accused DDR4 LRDIMM products include, without limitation, those with the following part numbers: MTA144ASQ16G72LSZ-2S6, MTA144ASQ16G72LSZ-2S9, MTA36ASF4G72LZ-2G6, MTA36ASF8G72LZ-2G9, MTA36ASF8G72LZ-3G2, MTA72ASS16G72LZ-3G2, MTA72ASS8G72LZ-2G6, and MTA72ASS8G72LZ-2G9. The accused DDR4 LRDIMM products include all branded, alternatively branded and non-branded products by Micron.

DDR5 Memory Modules

55. The accused DDR5 products include, without limitation, any Micron DDR5 products made in, sold in, offered for sale in, used in, exported from and/or imported into the United States by Micron. By way of non-limiting example, the accused DDR5 products include Micron products advertised on Micron's website. *See* Micron Technologies, DRAM Modules, *available at* https://www.micron.com/products/dram-modules. By way of non-limiting example, the accused DDR5 products include memory modules such as Micron's DDR5 UDIMMs, including, without limitation, those with the following part numbers: MTC16C2085S1UC48B, MTC4C10163S1UC48B, and MTC8C1084S1UC48B. On information and belief, Micron makes, sells, offers for sale, uses, exports from and/or imports into the United States DDR5 RDIMMs, LRDIMMs, UDIMMs and SODIMMs. The accused DDR5 products include all branded, alternatively branded and non-branded products by Micron.

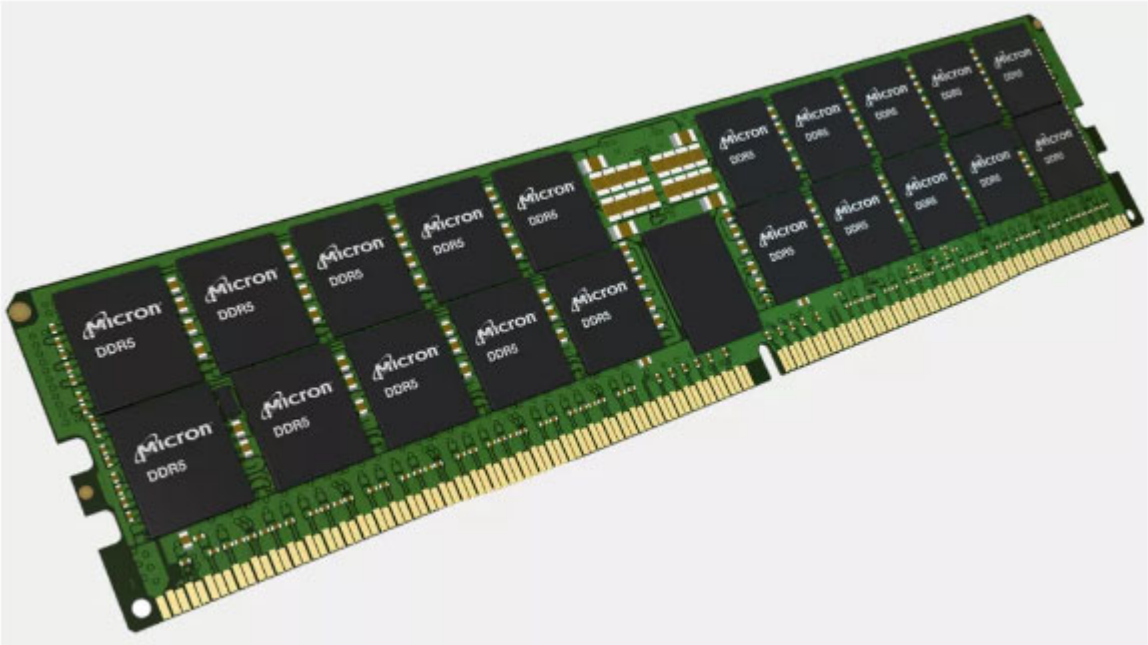
56. As further example, the Accused Instrumentalities include, without limitation, any DDR5 products made, sold, offered for sale, used and/or imported into the United States by Defendants, including those modules utilizing power management integrated circuits ("PMICs") supplied by third parties. *See* Ex. 13 (Micron DDR5 SDRAM UDIMM Part Catalog), and figure below.

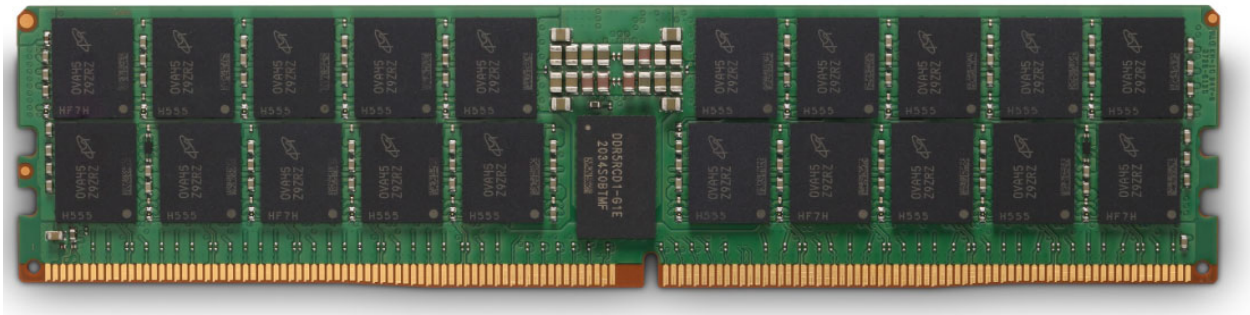
Figure 1: PMIC Package



Id. at 13 (schematic diagram of PMIC on Micron's DDR5 DIMMs).

57. By way of non-limiting example, the accused DDR5 products also include products publicized in a June 2, 2021 report on Micron's Technology Enablement Program. Ex. 14 at 1-2 ("Micron has showcased its DDR5 registered memory modules for servers and revealed that its DDR5 technology enablement program (TEP) has reached a milestone of 250 members from over 100 companies. Micron are on track to ship DDR5 DRAM ICs and memory modules later this year when the appropriate platforms become available.").





Id. at 1-2 (depictions of Micron's DDR5 RDIMMs).

58. When comparing DDR5 with DDR4, a key feature that Micron highlights is "Voltage Regulation on the Module." *See* Ex. 10 at 2 (available from https://www.micron.com/products/dram-modules) (referencing White Paper "Micron® DDR5: Client Module Features").

Micron White Paper

Voltage Regulation on the Module

Historically, power management has been done on the motherboard. DDR5 modules introduce local voltage regulation on the module. The voltage regulation is achieved by a power management integrated circuit (PMIC). The PMIC provides the brains of a smart voltage regulation system for the DDR5 DIMM, enabling configurability of voltage ramps and levels as well as current monitoring. The introduction of the PMIC enables on-DIMM threshold protection, as well as additional features such as error injection capabilities, programmable power-on sequence and power management. Additionally, the presence of the PMIC on the module enables better power regulation and reduces complexity of the motherboard design by reducing the scope of DRAM power delivery network (PDN) management.

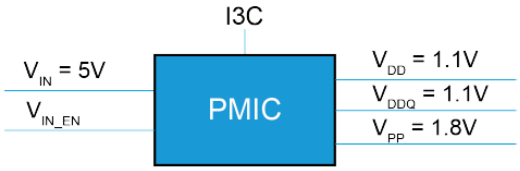


Figure 2: DDR5 Client PMIC (Basic Diagram)

59. The new power delivery solution also helps free up additional edge pins for isolation enhancement, thereby improving signal integrity. *See id.* at 3.

High Bandwidth Memory ("HBM")

60. HBM is a type of high-speed computer memory technology that relies in part on vertically-stacked memory dies and differs from the DDR5 DIMM formats described in the paragraphs above. Micron is a major supplier of HBM.

61. An illustration of Micron HBM2E DRAM is as follows.

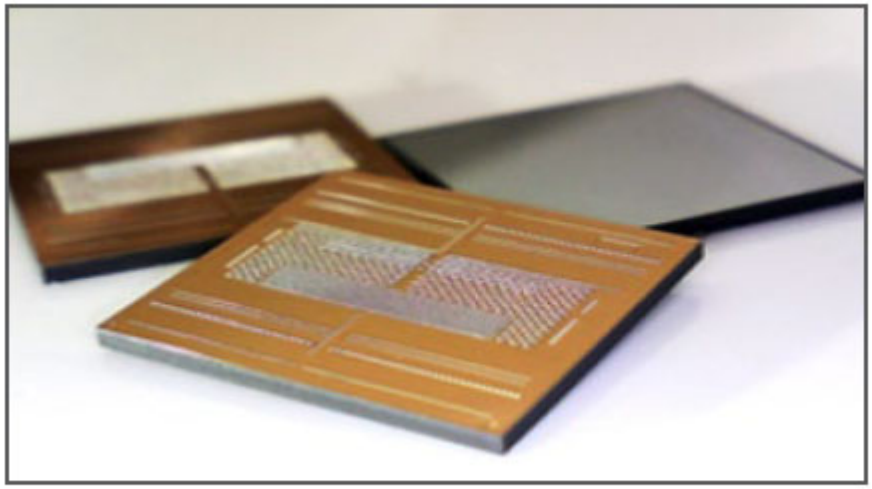


Figure 1: Micron HBM2E DRAM

Ex. 9 (Micron Technical Brief "Integrating and Operating HBM2E Memory") at 1.

62. HBM is part of Micron's Ultra-Bandwidth Solution. According to Micron, "High-bandwidth memory (HBM) is the fastest DRAM on the planet, designed for applications that demand the maximum bandwidth between memory and processing." *Id.* Micron boasts that "[b]y tightly integrating through-silicon-via (TSV) stacked memory die with host application-specific integrated circuit (ASIC) . . ., in the same chip package, Micron delivers the best bandwidth possible," and that "[Micron's] HBM2E device provides top energy efficiency and high capacity in a very small footprint." *Id.*

63. In the accused HBM products, at least eight DRAM memory dies are vertically connected in a single stacked device. The stack is then interconnected to an additional logic or base die which interfaces with the host ASIC. On information and belief, the DRAM dies and the logic die are shipped as a stack and Micron's customers then have them integrated with the ASIC host as a system-in-package, as illustrated below. *Id.* at 2. The use of silicon interposers to interconnect DRAMs and the host enables the data bus to run much wider than is possible with discrete DRAMs, therefore allowing the data to run at much lower per-pin data rate and at much reduced power requirement. *Id.* That is, HBM significantly increases the bandwidth while still maintaining power efficiency, which in turn simplifies designs. *Id.*

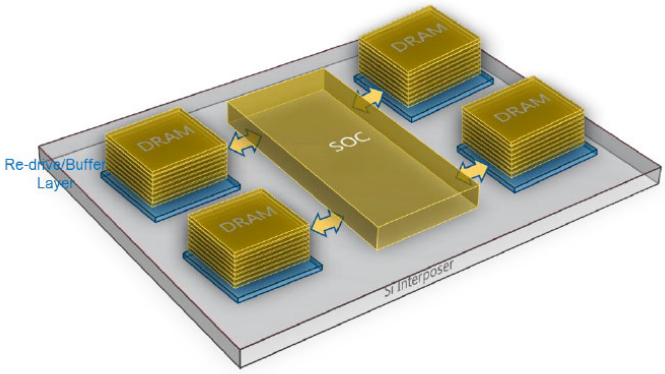


Figure 1: Example of a System-in-Package (SiP) With HBM2E DRAMs

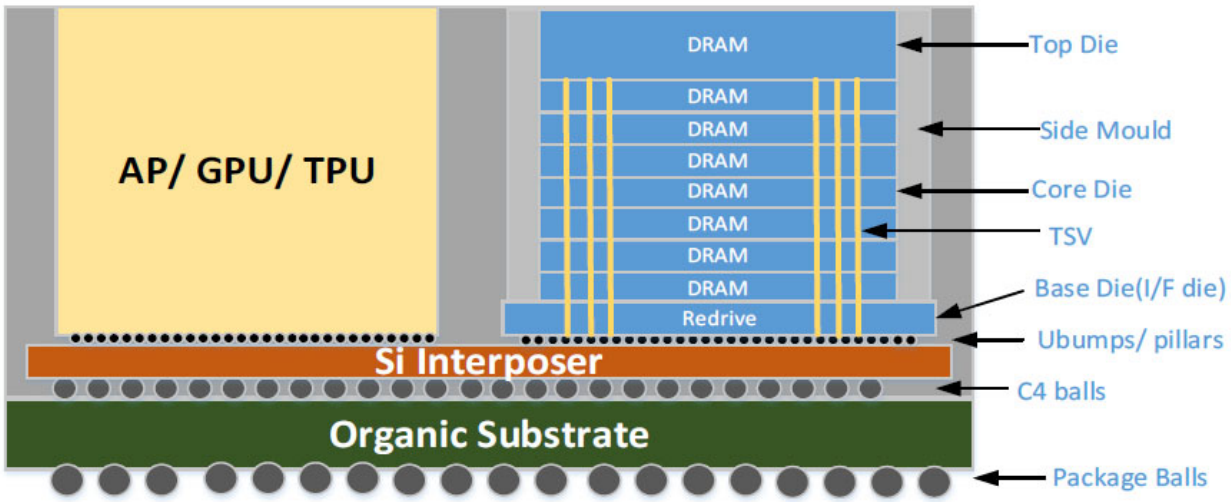


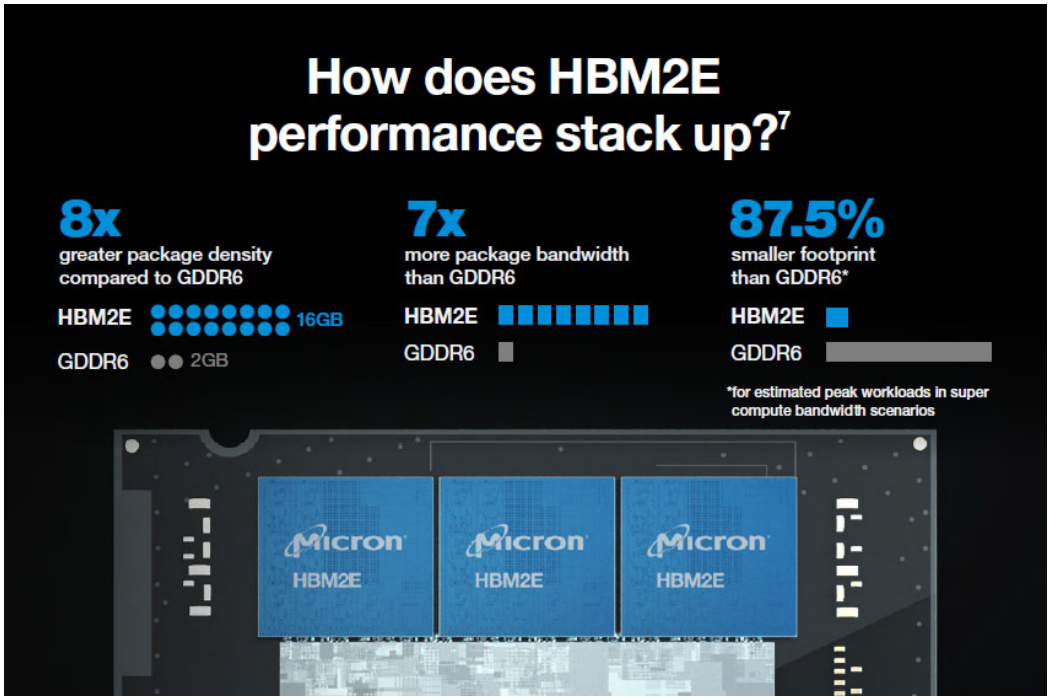
Figure 3: Cross Section of a System-in-Package (SiP) With HBM2E

Id. at 2-3 (annotations in original).

64. The Accused HBM Products include, without limitation, any Micron HBM2E and newer products with 8 or more stacked DRAM dies made, sold, used, offered for sale, and/or imported into the United States by Micron. By way of non-limiting example, the Accused HBM Products include Micron HBM2E products having the following part numbers: MT54A16G8080A00AC-28, and MT54A16G8080A00AC-32. The accused HBM Products also include ones created by Micron customers or their contractors who took raw DRAM or flash or

unfinished versions of the products and then created infringing products. The accused HBM Products include all branded, alternatively branded and non-branded products by Micron.

65. By way of non-limiting example, the Accused HBM products also include products marketed and publicized in a 2021 press release titled "HBM2E The Leader in High Bandwidth," as shown below.



Ex. 7 (depictions of Micron's HBM2E Product).

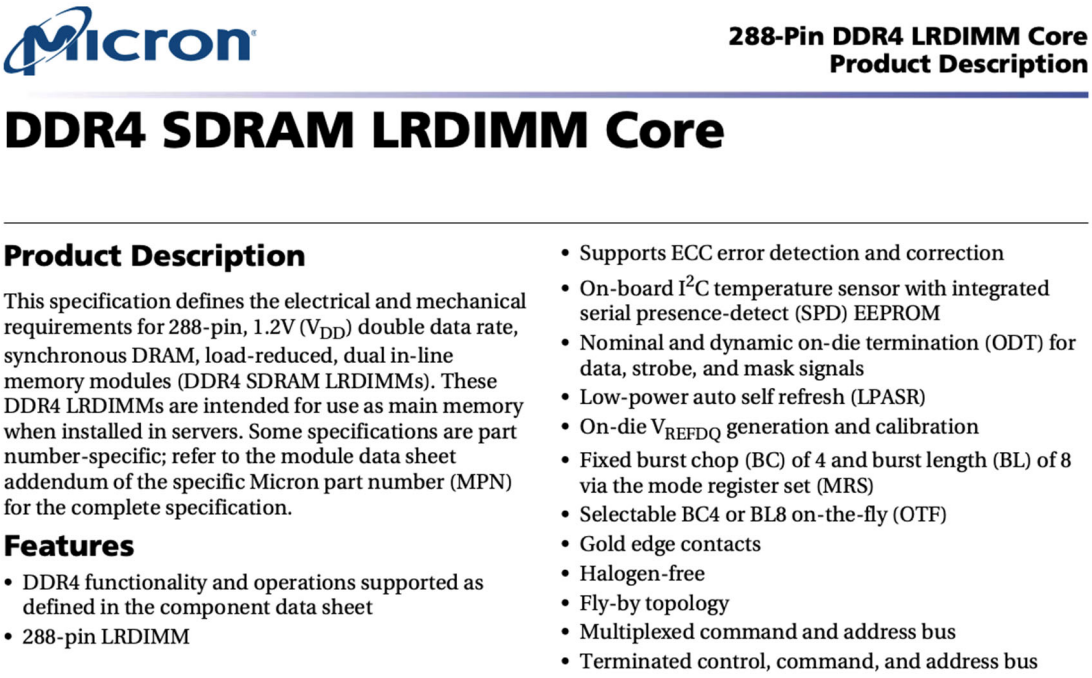
IV. FIRST CLAIM FOR RELIEF – '506 PATENT

66. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

67. On information and belief, Micron directly infringed and is currently infringing at least one claim of the '506 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example, and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '506 Patent.

68. For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus. As an example, Micron's website markets and contains datasheets for

the accused DDR4 LRDIMMs. *See* Micron Technologies, DRAM Modules, *available at* https://www.micron.com/products/dram-modules. An example is depicted below.



Micron

288-Pin DDR4 LRDIMM Core
Product Description

DDR4 SDRAM LRDIMM Core

Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2V (V_{DD}) double data rate, synchronous DRAM, load-reduced, dual in-line memory modules (DDR4 SDRAM LRDIMMs). These DDR4 LRDIMMs are intended for use as main memory when installed in servers. Some specifications are part number-specific; refer to the module data sheet addendum of the specific Micron part number (MPN) for the complete specification.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin LRDIMM
- Supports ECC error detection and correction
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- On-die V_{REFDQ} generation and calibration
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Multiplexed command and address bus
- Terminated control, command, and address bus

Ex. 16 at 1 (Micron DDR4 SDRAM LRDIMM Core specification).

69. The accused DDR4 LRDIMMs each include a registering clock driver (RCD) "[t]o reduce the electrical load on the host memory controller's command, address, and control bus." *Id*. at 12. It communicates with a server's memory controller via control and address signal lines in a memory bus as well as a data bus. For example:

Table 5: Pin Descriptions

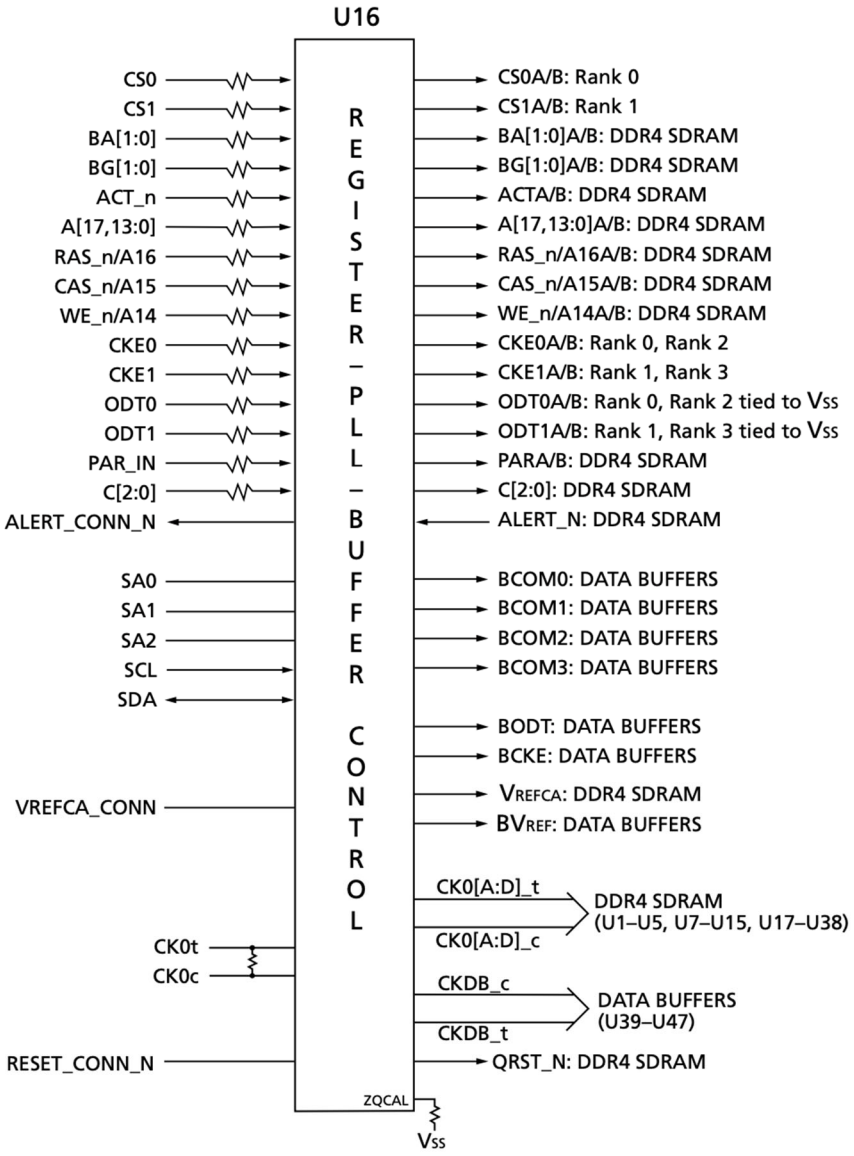
Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (initiator/target) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).

Table 5: Pin Descriptions (Continued)

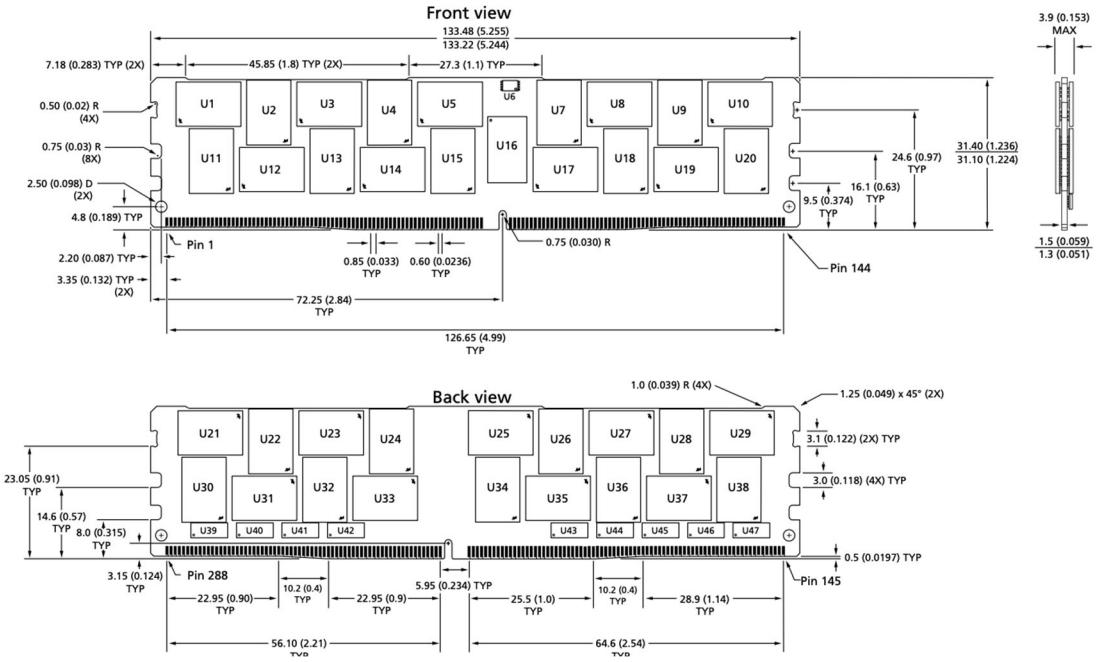
Symbol	Type	Description
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to V_{DD} on DIMMs.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.

Id. at 6-7.

See also, e.g., Ex. 15 (Micron MTA36ASF4G72LZ datasheet) at 9:



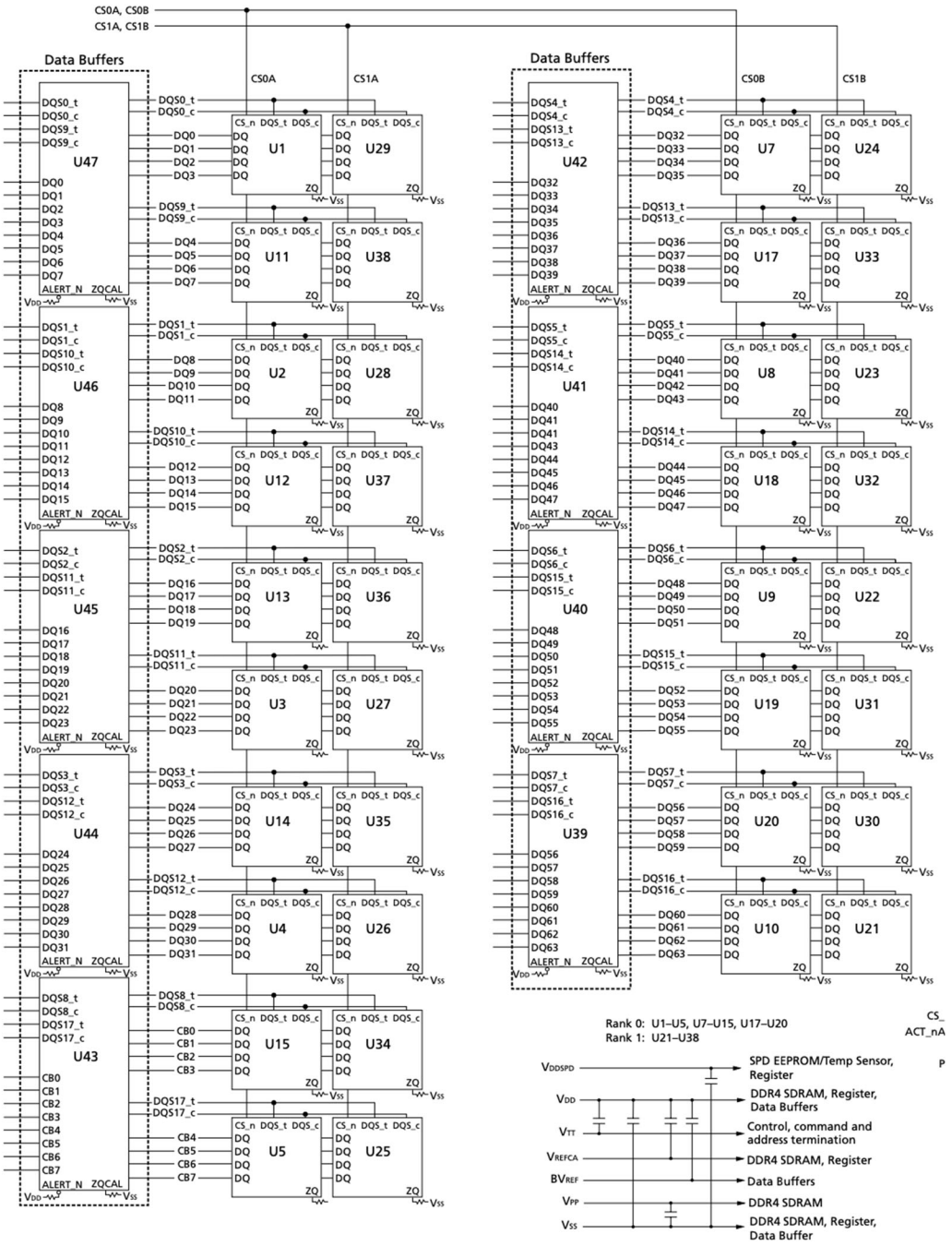
70. The accused DDR4 LRDIMMs further each comprise a module board having edge connections to be coupled to respective signal lines in the memory bus, as illustrated in the examples below.



Id. at 24 (depiction of a Micron DDR4 LRDIMM).

71. The accused DDR4 LRDIMMs further each comprise a module control device (*e.g.*, a RCD) on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals, and memory devices (*e.g.*, DDR4 SDRAMs) arranged in multiple ranks on the module board and coupled to the module control device (*e.g.*, RCD) via module C/A signal lines that conduct the registered C/A signals as illustrated in the examples above and below.

Figure 2: Functional Block Diagram

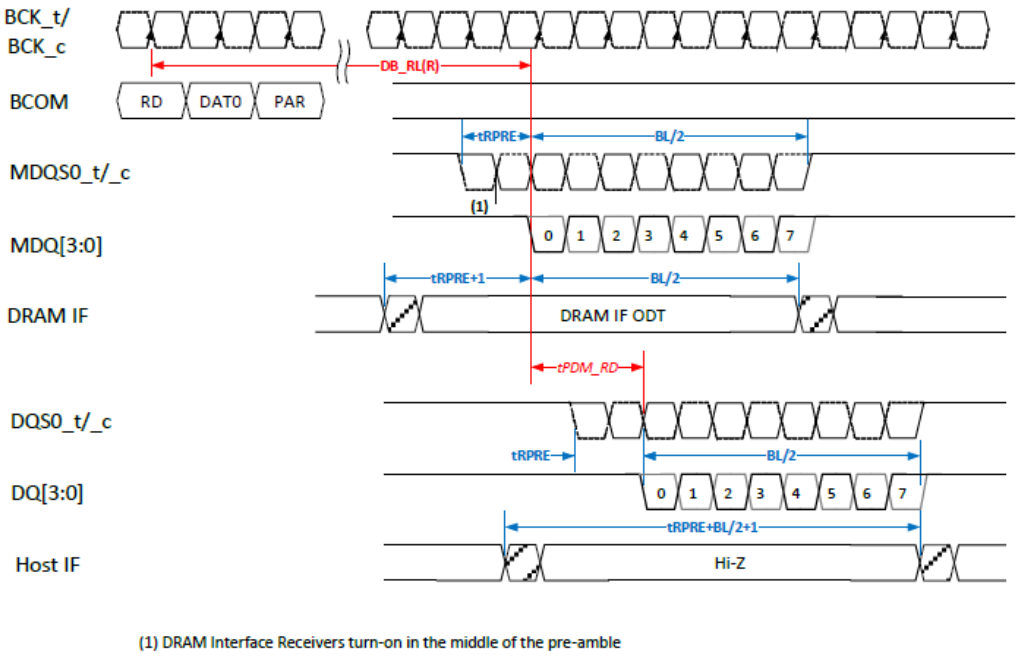


Id. at 9.

72. In each accused DDR4 LRDIMM, the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and a first memory device in the selected rank

is configurable to output at least a first section of the read data and at least a first read strobe. For example, each accused DDR4 LRDIMM follows the timing sequence for a READ command shown below.

Figure 3 shows the timing sequence for a Read command.



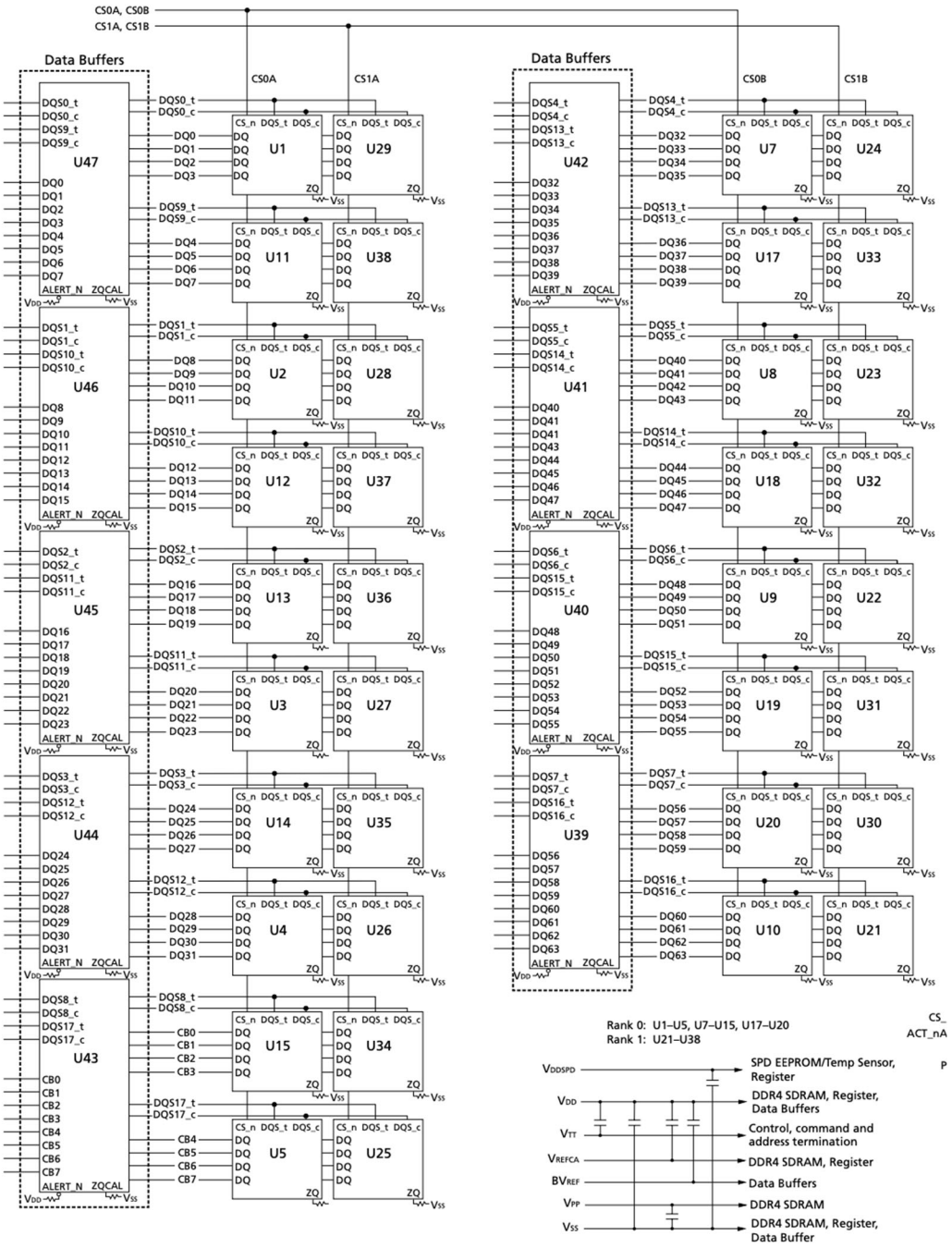
(1) DRAM Interface Receivers turn-on in the middle of the pre-amble

Figure 3 — READ Timing

Ex. 18 (JEDEC JESD82-32A Standard), at 14; *see also, e.g.*, Ex. 15 (Micron MTA36ASF4G72LZ datasheet) at 9 (functional block diagram for a representative product, depicted above).

73. The accused DDR4 LRDIMMs further each include data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, as illustrated below. *See, e.g.*, Ex. 15 (Micron MTA36ASF4G72LZ datasheet) at 9 (depicting Micron's DDR4 LRDIMMs including data buffers coupled between at least one respective memory device in each of the multiple ranks) (annotations in original).

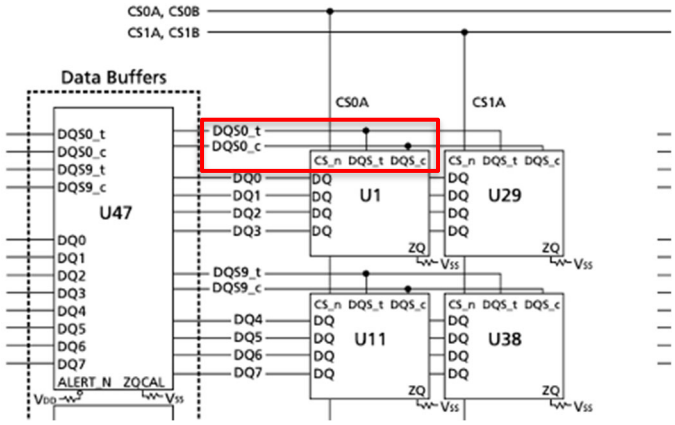
Figure 2: Functional Block Diagram



74. In each accused DDR4 LRDIMM, a first data buffer on the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals: delay the first read strobe by a first predetermined amount to generate a first delayed read strobe; sample the first section of the read data using the first delayed read strobe; and transmit the

first section of the read data to a first section of the data bus; wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations. For example, the strobes MDQS0_t and MDQS0_c are delayed by a variable delay circuitry and produce a first delayed read strobe in response to one or more module control signals (*e.g.*, BCOM[3:0]). The data buffer determines the predetermined amount of delay based on, for example, BCW signals received from the memory controller of the host in one or more previous operations, which signals in turn are in response to information sent by the memory module as part of MRD training.

Figure 2: Functional Block Diagram



Ex. 15 (Micron MTA36ASF4G72LZ datasheet) at 9 (annotated).

75. On information and belief, Micron also indirectly infringes the '506 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Micron's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Micron has induced, and currently induces, the infringement of the '506 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM and other materially similar products that infringe the '506 Patent. On information and belief, Micron provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM

products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

76. On information and belief, Micron also indirectly infringes the '506 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Micron has contributed to, and currently contributes to, Micron's customers and end-users infringement of the '506 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM and other materially similar products that infringe the '506 Patent. On information and belief, the accused DDR4 LRDIMM products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Micron is aware that the product or process that includes the accused DDR4 LRDIMM and other materially similar products would be covered by one or more claims of the '506 Patents. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM and other materially similar products infringes at least one claim of the '506 Patent.

77. Micron's infringement of the '506 Patent has damaged and will continue to damage Netlist. Micron has had actual notice of the '506 Patent since at least April 28, 2021. Micron's infringement of the '506 Patent has been continuing and willful. Micron continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Micron knew or should have known that its actions constituted an unjustifiably high risk of infringement.

V. SECOND CLAIM FOR RELIEF – '339 PATENT

78. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

79. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '339 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '339 Patent.

80. For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprises a N-bit-wide memory module (*e.g.*, 64-bit-wide) mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide. For instance, each LRDIMM includes a RCD "[t]o reduce the electrical load on the host memory controller's command, address, and control bus." Ex. 16 (Micron DDR4 SDRAM LRDIMM Core specification) at 12. It communicates with a server's memory controller via control and address signal lines in a memory bus as well as a data bus. For example:

Table 5: Pin Descriptions

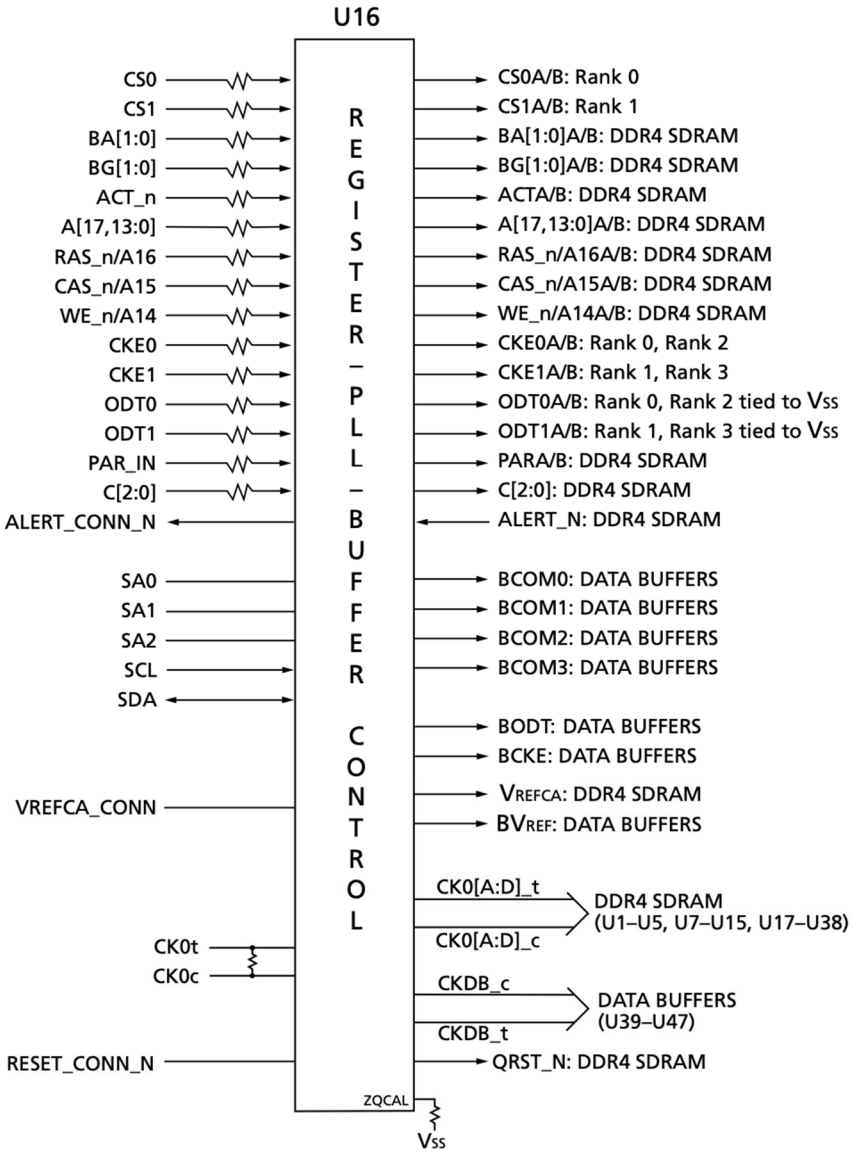
Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (initiator/target) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to V_{DD} on DIMMs.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.

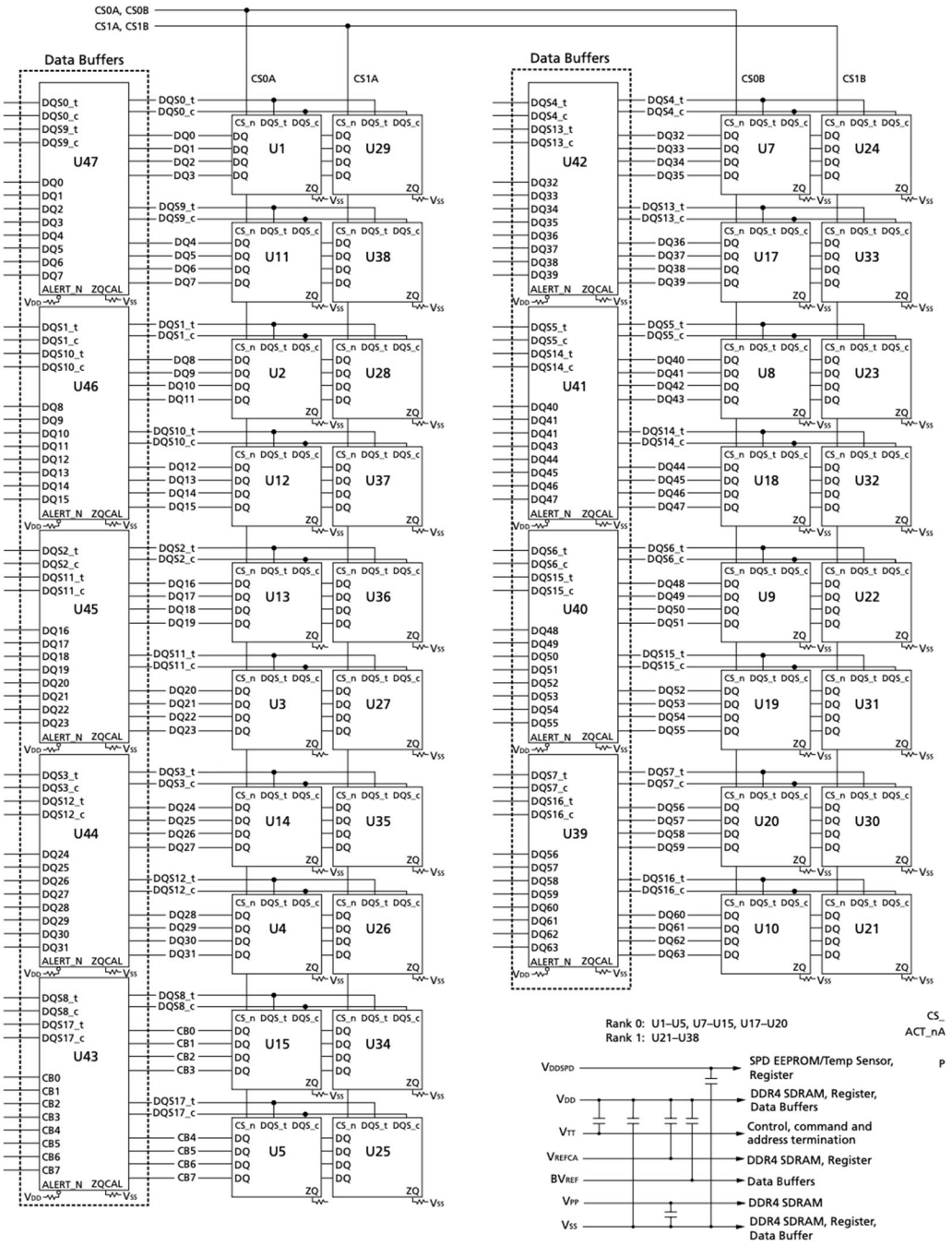
Id. at 6-7.

See also, e.g., Ex. 15 (Micron MTA36ASF4G72LZ datasheet) at 9:



81. In the configuration above, there are 9 sets of byte-wide signal lines including 64-bit wide data signal lines (DQ0-DQ63) and 8-bit wide check bits signal lines (CB0-CB7). For example:

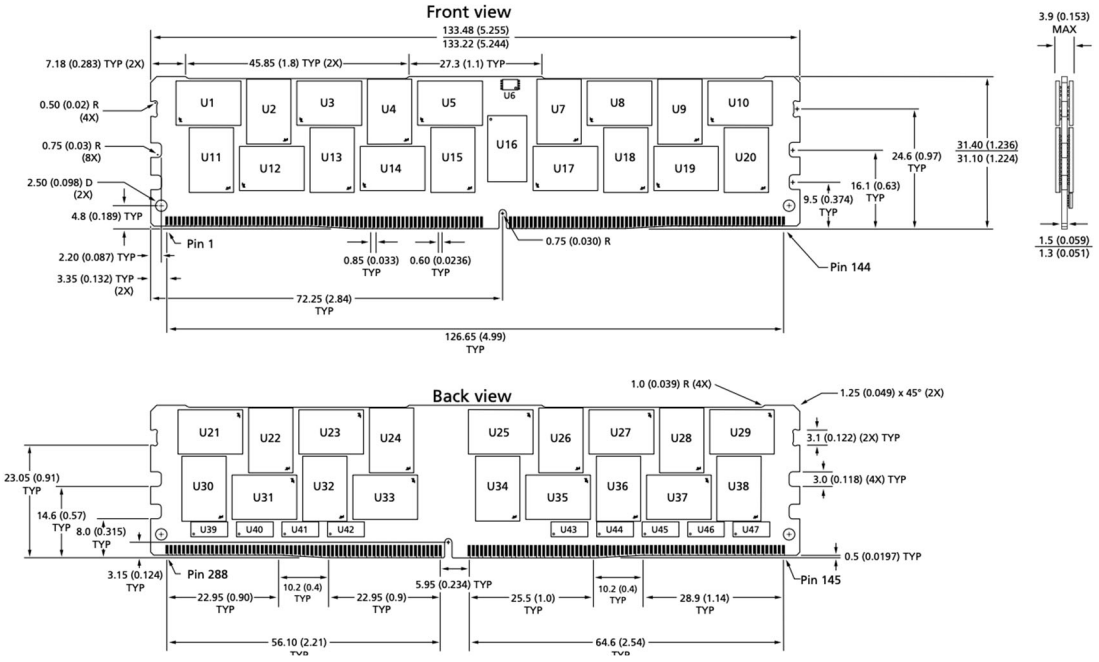
Figure 2: Functional Block Diagram



Id.

82. The accused DDR4 LRDIMMs each comprise a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of

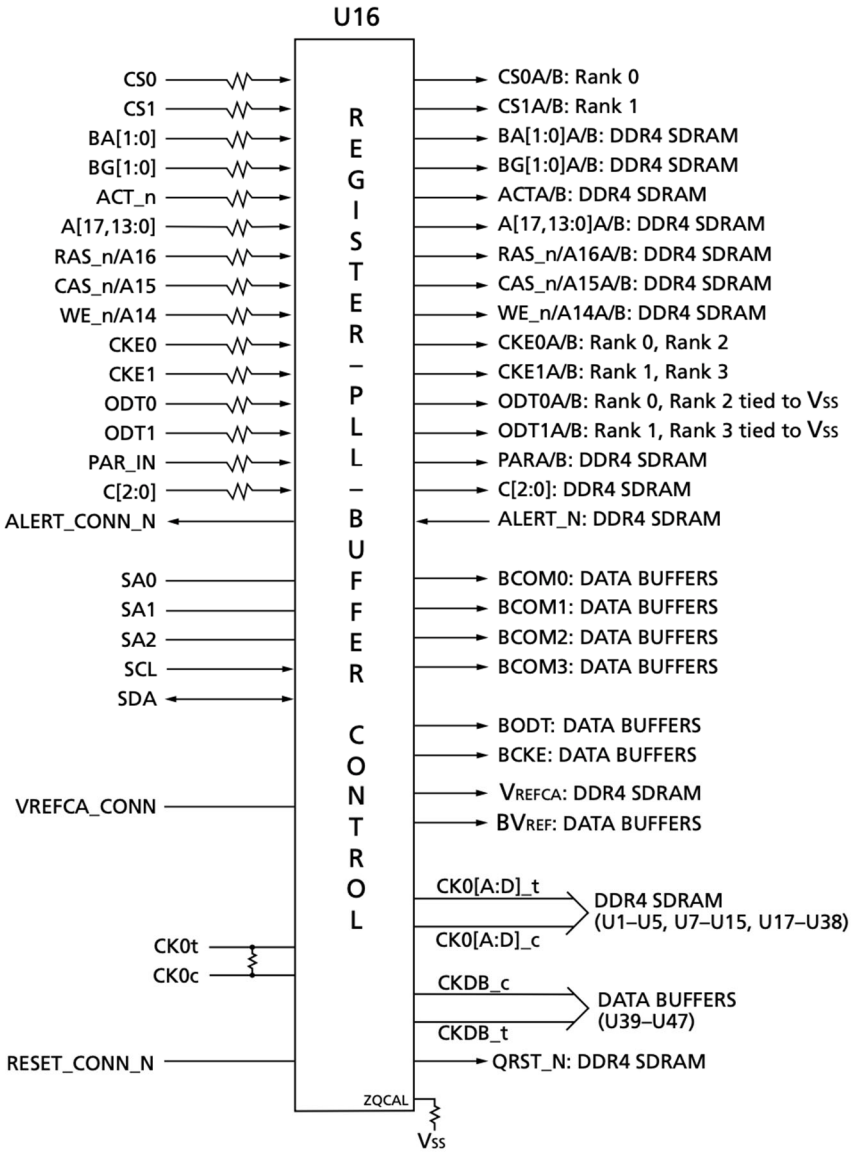
the PCB and configured to be releasably coupled to corresponding contacts of the memory socket. For example:



Id. at 24 (depiction of a Micron DDR4 LRDIMM).

83. The accused DDR4 LRDIMMs each include double data rate dynamic random access memory (*e.g.*, DDR4 DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks. As shown above, each DDR4 LRDIMM includes multiple ranks of memory devices.

84. The accused DDR4 LRDIMMs further comprise a module controller (*e.g.*, RCD) coupled to the PCB and operatively coupled to the DDR DRAM devices. For example:



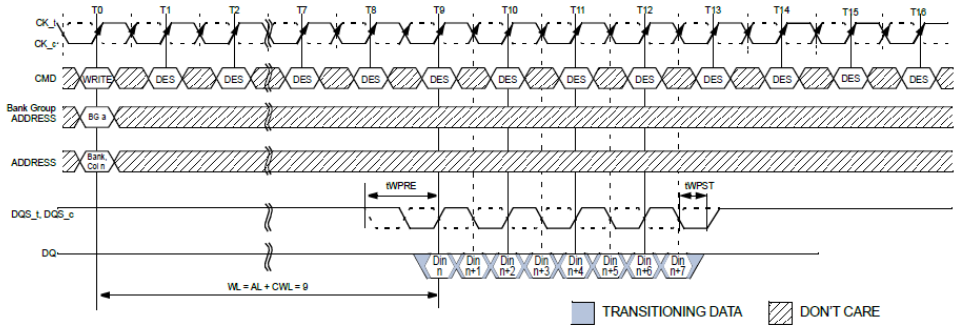
Id. at 9.

85. The module controller (*e.g.*, RCD) is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data (*e.g.*, by using a registered chip-select signal to select a target rank for

performing the memory write operation), wherein the module controller is further configurable to output module control signals (*e.g.*, during a first clock cycle when BCOM [3:0] is 1000, the module control signals would correspond to a write WR command) in response to at least some of the input address and control signals. For example, a Write burst operation results in a burst of data and data strobes received by the DDR4 LRDIMM via the DQS/DQ pins of the memory bus, and to write the data via data buffers into a memory device as determined by input address and control signal (*e.g.*, CS signal). *See, e.g.*, Ex. 19 (JESD79-4C DDR4 SDRAM Standard), at 122 (reproduced below); Ex. 15 (Micron MTA36ASF4G72LZ datasheet) at 9.

4.25.5 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.



NOTE 1 BL = 8, WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
NOTE 2 DIN n = data-in to column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

Figure 128 — WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)

86. Further, as illustrated above and below, the accused DDR4 LRDIMMs also each comprise a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals, wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side, wherein the each respective byte-wise buffer is disposed on the PCB

at a respective position corresponding to the respective set of the plurality of sets of data signal lines.

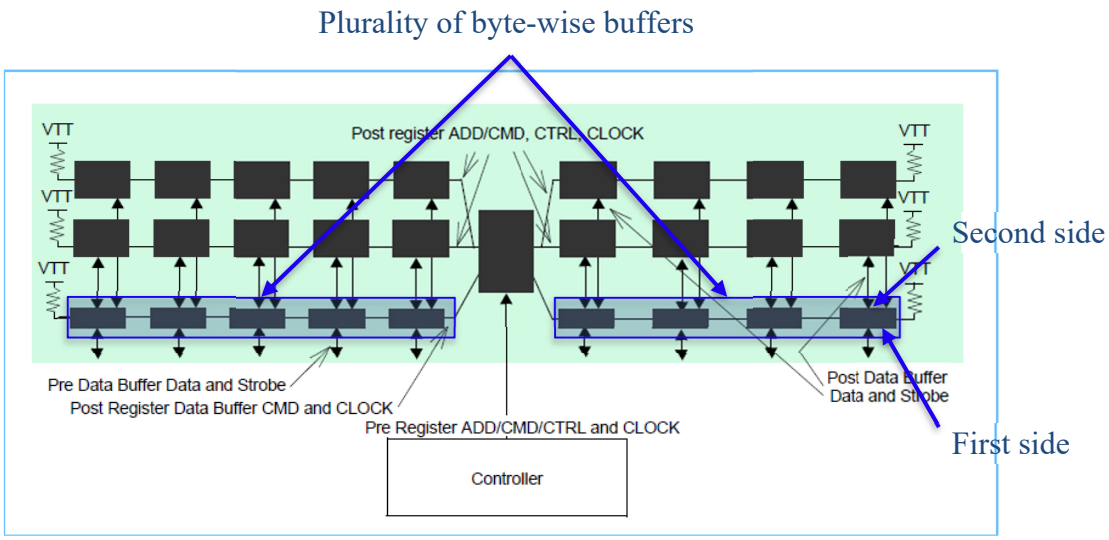


Figure 3 — LRDIMM Topologies

Ex. 20 (JEDEC 21C Standard), at 4.20.27-17.

87. In each of the accused DDR4 LRDIMMs, the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals and the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers, *e.g.*, via the MDQ_OE signal associated with a particular TX for a particular MDQ bit, to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period. For example:

4.61 Logic Diagram

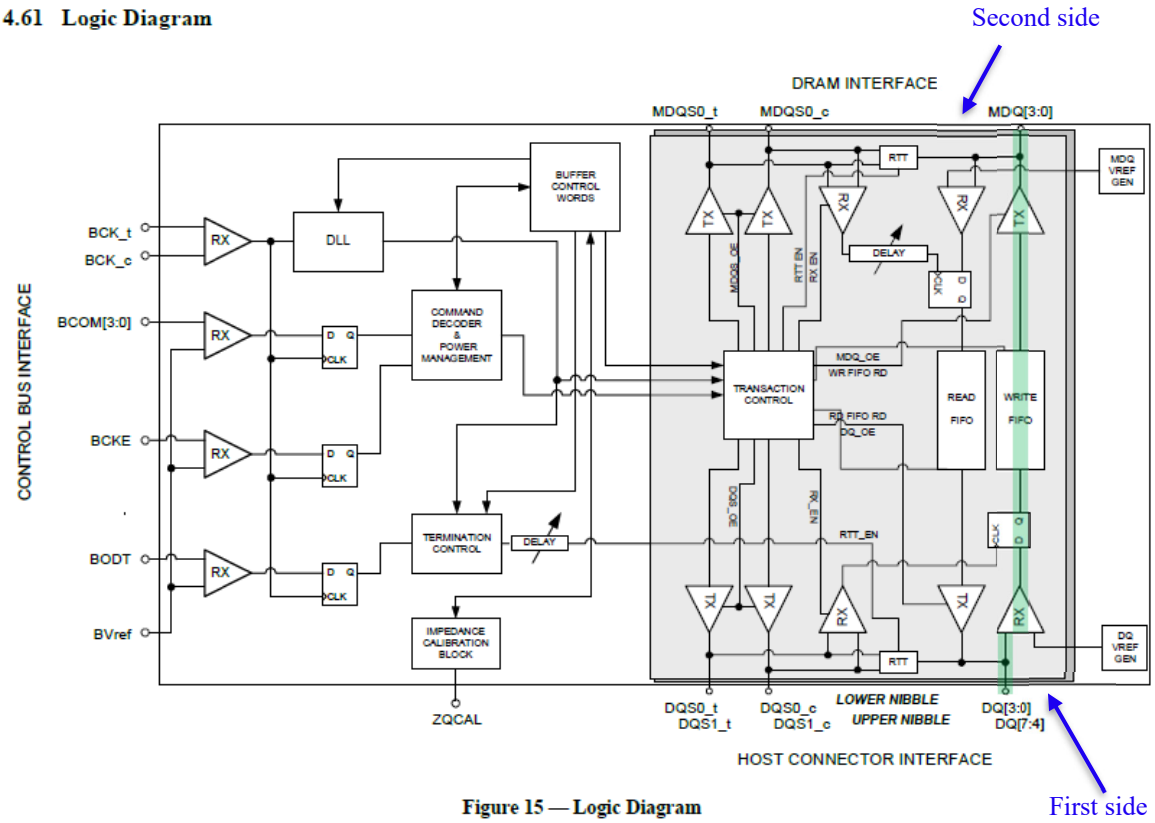


Figure 15 — Logic Diagram

Ex. 18 (JESD82-32A Standard), at 95 (showing an example of a byte-wise data path (upper nibble and lower nibble), highlighted in green, between the first side at DQ and the second side at MDQ).

88. In each of the accused DDR4 LRDIMMs, the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period. For example:

Figure 2 shows the timing sequence for a Write command.

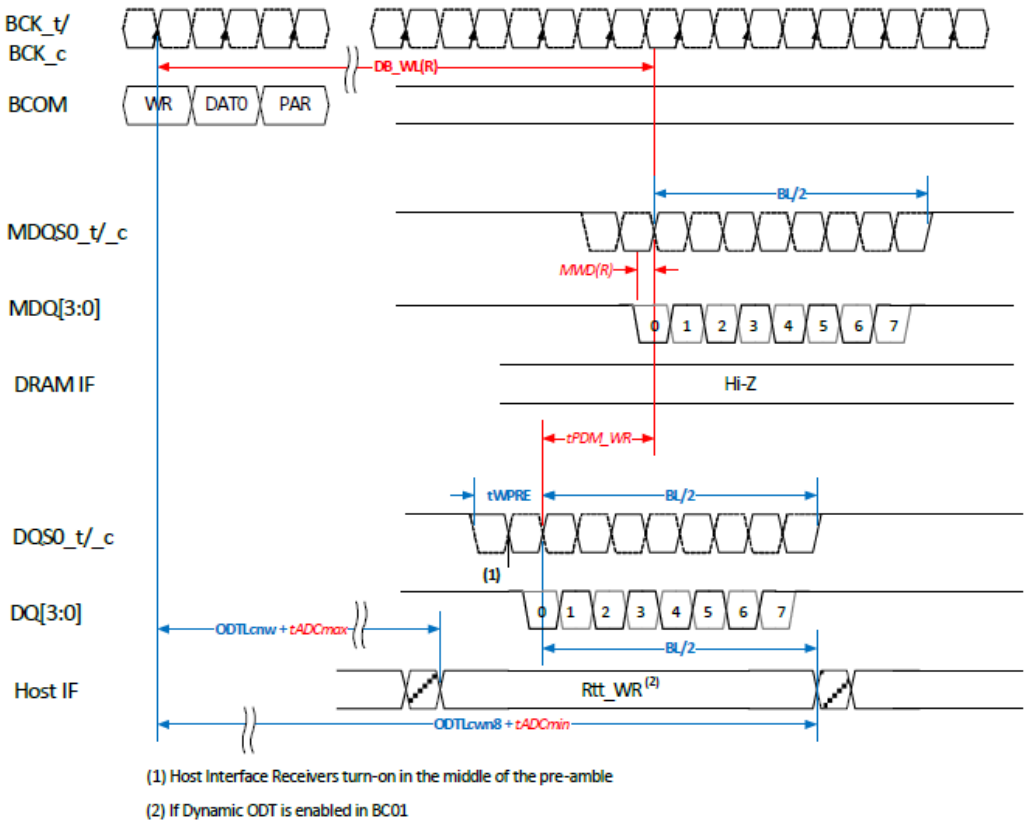


Figure 2 — WRITE Timing

Id. at 13.

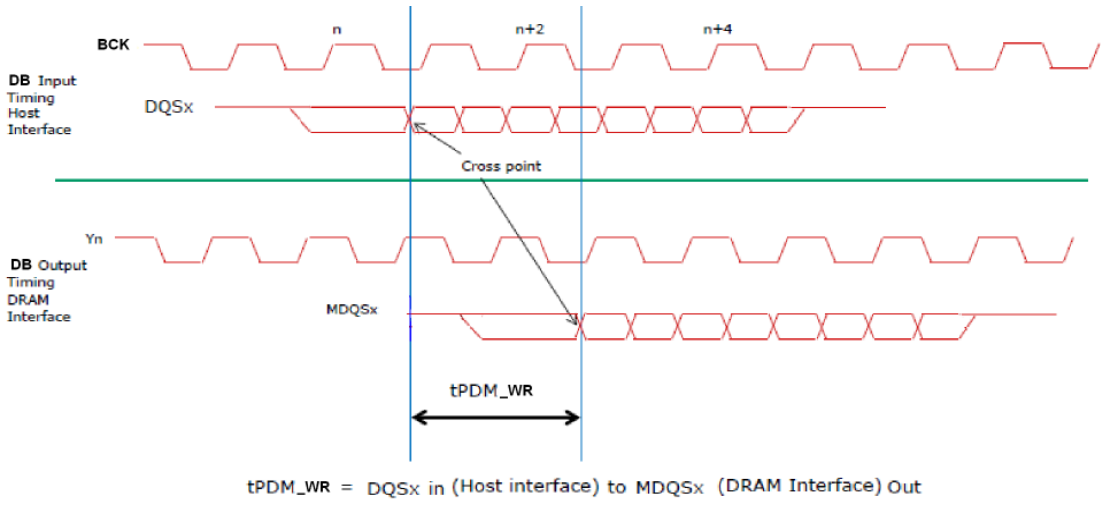


Figure 56 — tPDM_WR Latency Measurement

Id. at 165.

Table 146 — WRITE Output Timings

		DDR4-1600/ 1866/2133		DDR4-2400/ 2666		DDR4- 2933		DDR4-3200		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing											
tDVB	Data valid before MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
tDVA	Data valid after MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
Data Strobe Timing											
MDQS_t - MDQS_c differential output low time	tMQSL	0.46	-	0.46	-	0.46	-	0.46	-	tCK	1, 3
MDQS_t - MDQS_c differential output high time	tMQSH	0.46	-	0.46	-	0.46	-	0.46	-	tCK	2, 3

Unit UI = tCK(avg).min/2

NOTE 1: tMQSL describes the instantaneous differential output low pulse width on MDQS_t - MDQS_c, as measured from on falling edge to the next consecutive rising edge

NOTE 2: tMQSH describes the instantaneous differential output high pulse width on MDQS_t - MDQS_c, as measured from on rising edge to the next consecutive falling edge

NOTE 3: The specification values are affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.). However, these parameters should be met whether clock jitter is present or not.

Id. at 169.

89. On information and belief, Micron also indirectly infringes the '339 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Micron's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Micron has induced, and currently induces, the infringement of the '339 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM products and other materially similar products that infringe the '339 Patent. On information and belief, Micron provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

90. On information and belief, Micron also indirectly infringes the '339 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Micron has contributed to, and currently contributes to, Micron's customers and end-users infringement of the '339 Patent through its affirmative acts of selling and

offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the '339 Patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Micron is aware that the product or process that includes the accused DDR4 LRDIMM products and other materially similar products would be covered by one or more claims of the '339 Patent. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the '339 Patent.

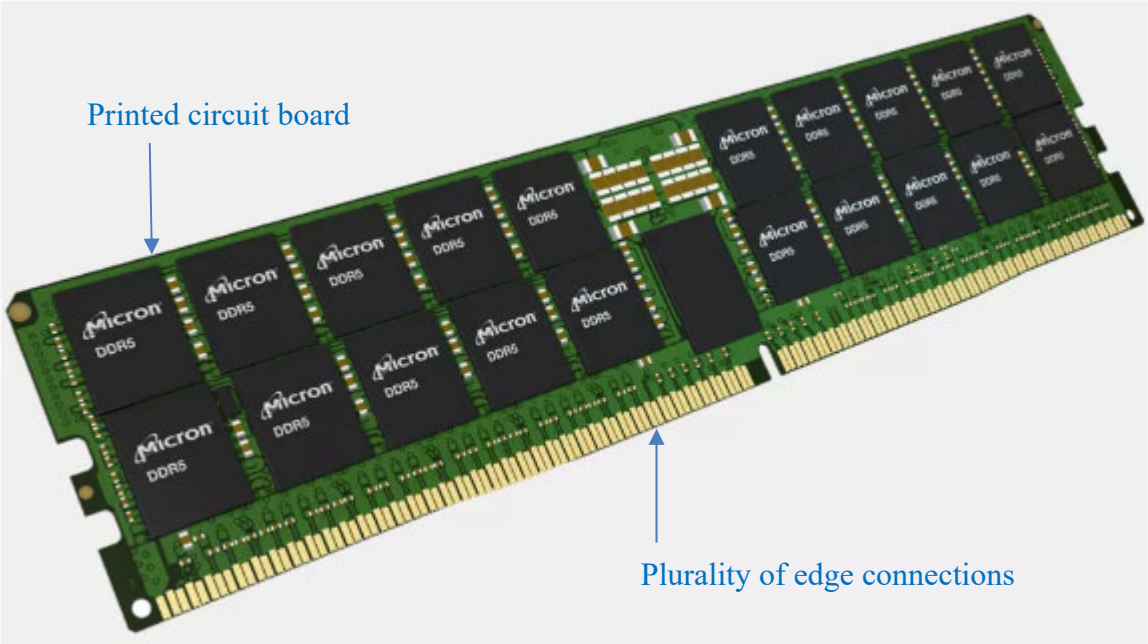
91. Micron's infringement of the '339 Patent has damaged and will continue to damage Netlist. Micron has had actual notice of the '339 Patent since at least April 28, 2021. Micron's infringement of the '339 Patent has been continuing and willful. Micron continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Micron knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VI. THIRD CLAIM FOR RELIEF – '918 PATENT

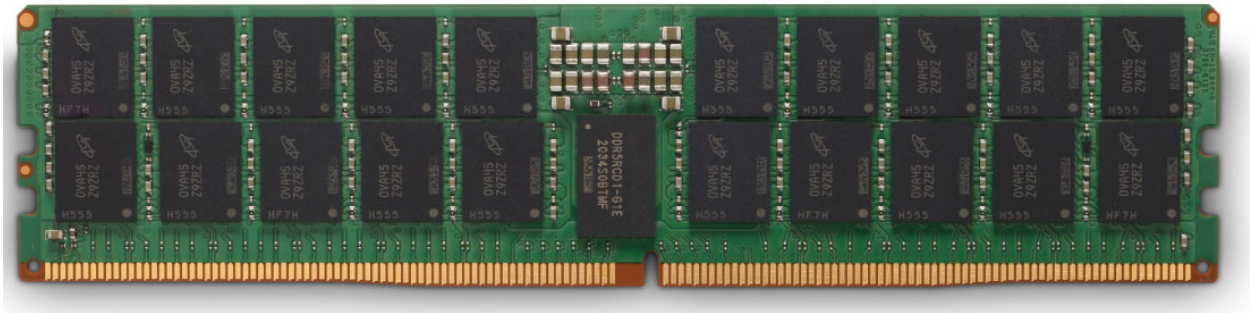
92. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

93. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '918 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR5 LRDIMMs, DDR5 RDIMMs, DDR5 SODIMMs, DDR5 UDIMMs, and other products with materially the same structures in relevant parts. For example, and as shown below, the accused DDR5 memory modules and other products with materially the same structures in relevant parts infringe at least one claim of the '918 Patent.

94. For example, the accused DDR5 products comprise a memory module comprising: a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system, as illustrated below.



Ex. 14 at 1 (annotated depiction of a Micron DDR5 RDIMM).



Id. at 2 (depiction of a Micron DDR5 RDIMM).

95. The accused DDR5 products further comprise a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck

converter configured to provide a third regulated voltage having a third voltage amplitude; and a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude. For example, Micron's DDR5 memory modules feature an on-module PMIC that is new for DDR5. As shown below, the on-board PMIC receives a nominal 12V input supply V_BULK, as well as an alternative power supply VIN_Management. Ex. 8 (Micron® DDR5: Key Module Features) at 2. On information and belief, V_BULK is the power input to buck converters while VIN_Management supplies power to other components on the board. The output of the PMIC includes three voltages VDD, VDDQ, and VPP outputted by buck converts and a nominal 1.0V output by a linear dropout regulator (LDO). On information and belief, VDD and VDDQ are nominally at 1.1V and VPP is nominally at 1.8V. *Cf.*, Ex. 10 at 2, Fig. 2 (listing aforementioned nominal voltage amplitudes for VDD, VDDQ, and VPP for Micron's DDR5 UDIMMs/SODIMMs).

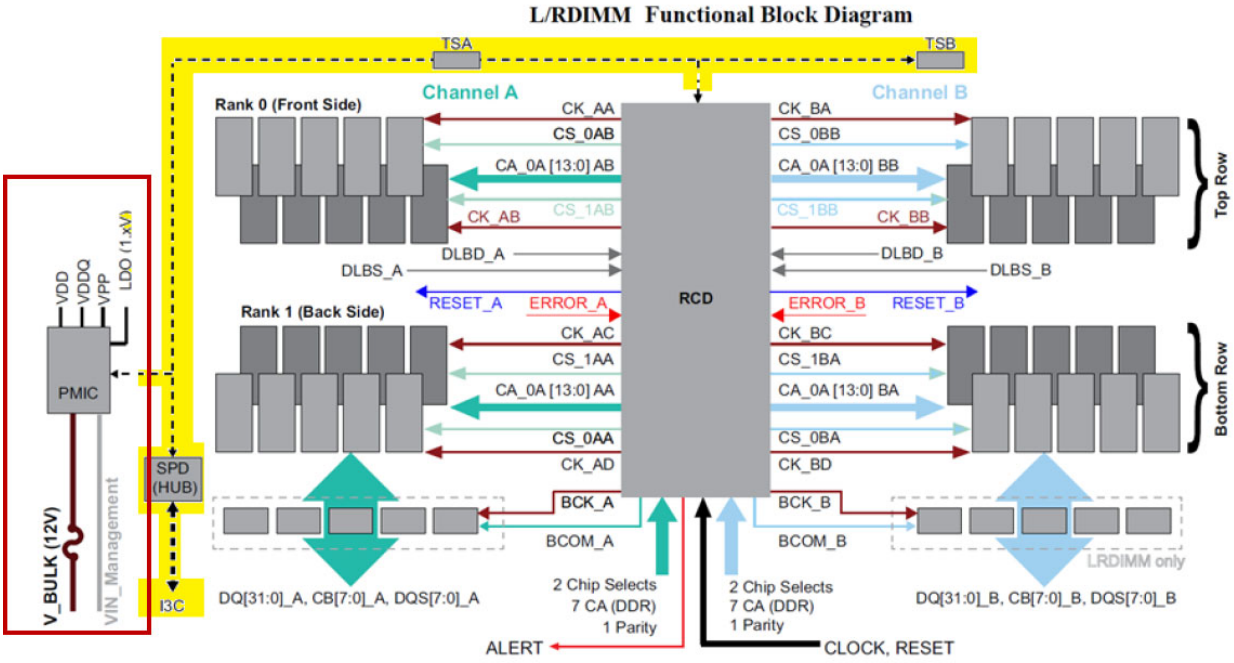
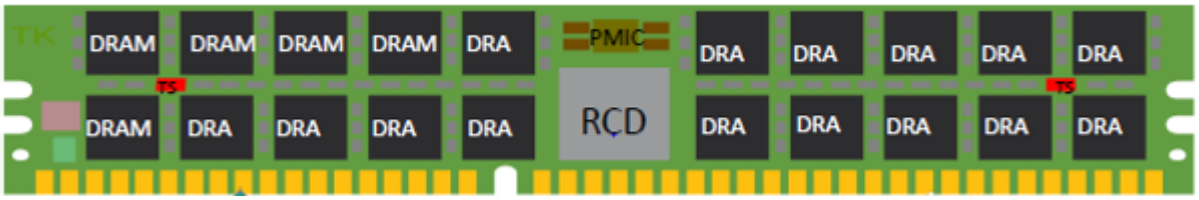


Figure 2: Functional Block Diagram of RDIMM and LRDIMM Memory

See also, e.g., *id.* at 2 ("DDR5 modules introduce local voltage regulation on the module. The voltage regulation is achieved by a power management integrated circuit (PMIC). The PMIC provides the brains of a smart voltage regulation system for the DDR5 DIMM, enabling configurability of voltage ramps and levels as well as current monitoring. Power management has historically been done on the motherboard. The introduction of PMICs allows additional features like threshold protection, error injection capabilities, programmable power on sequence, and power management features. The presence of the PMIC on the module enables better power regulation and reduces complexity of the motherboard design by reducing the scope of DRAM power delivery (PDN) management.").



Ex. 8 (Micron® DDR5: Key Module Features) at 1 (depicting on-module PMIC).

96. The PMIC provides the required regulated voltages, in accordance with the latest DDR5 standards. For example:

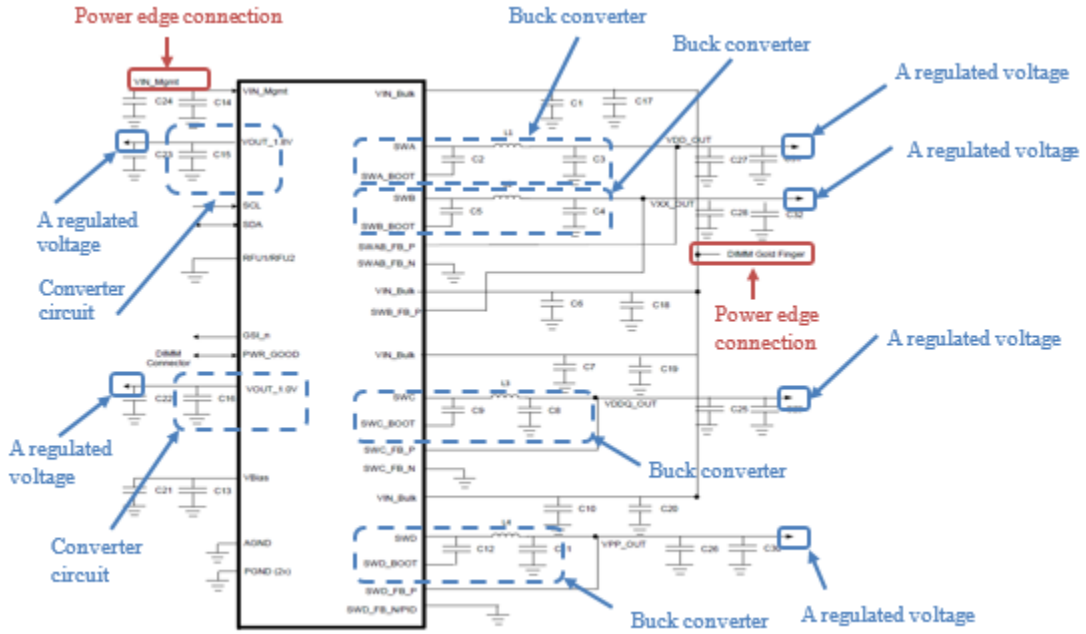


Figure 10 — Single Phase Regulator Example Schematic

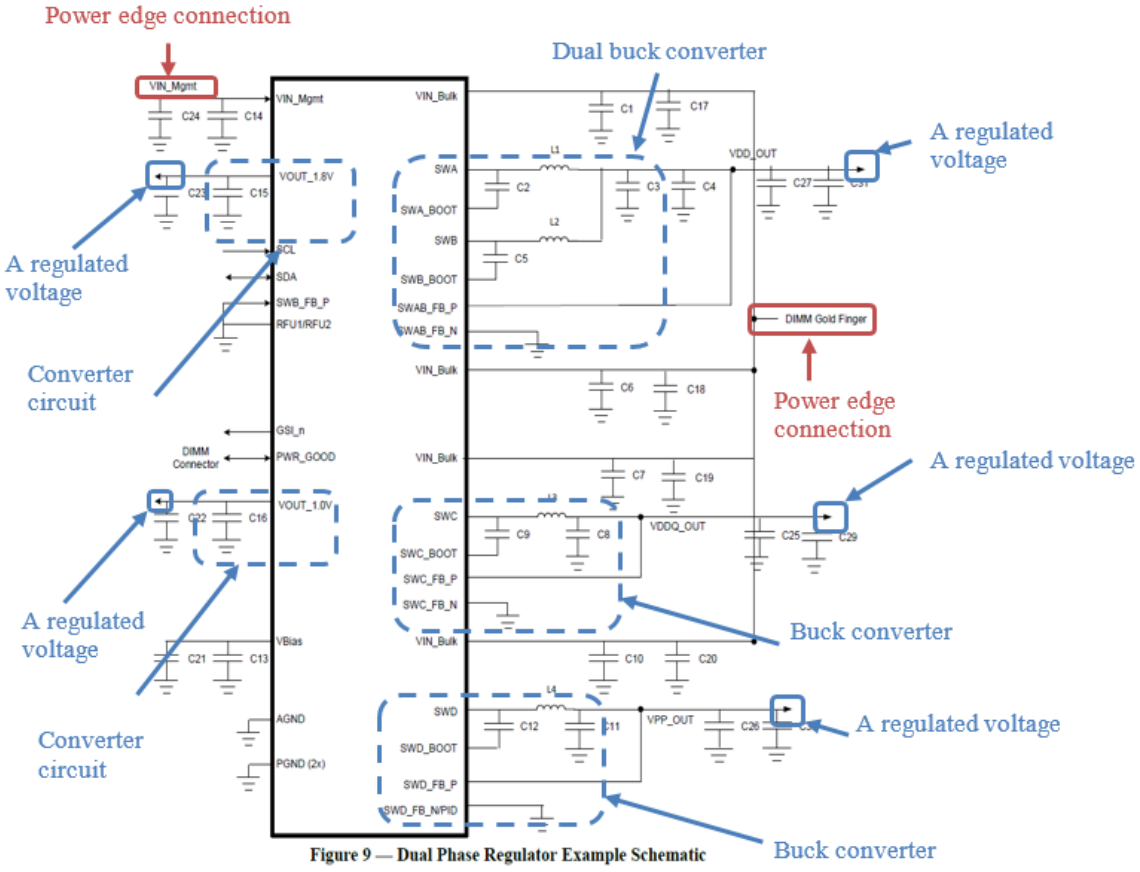
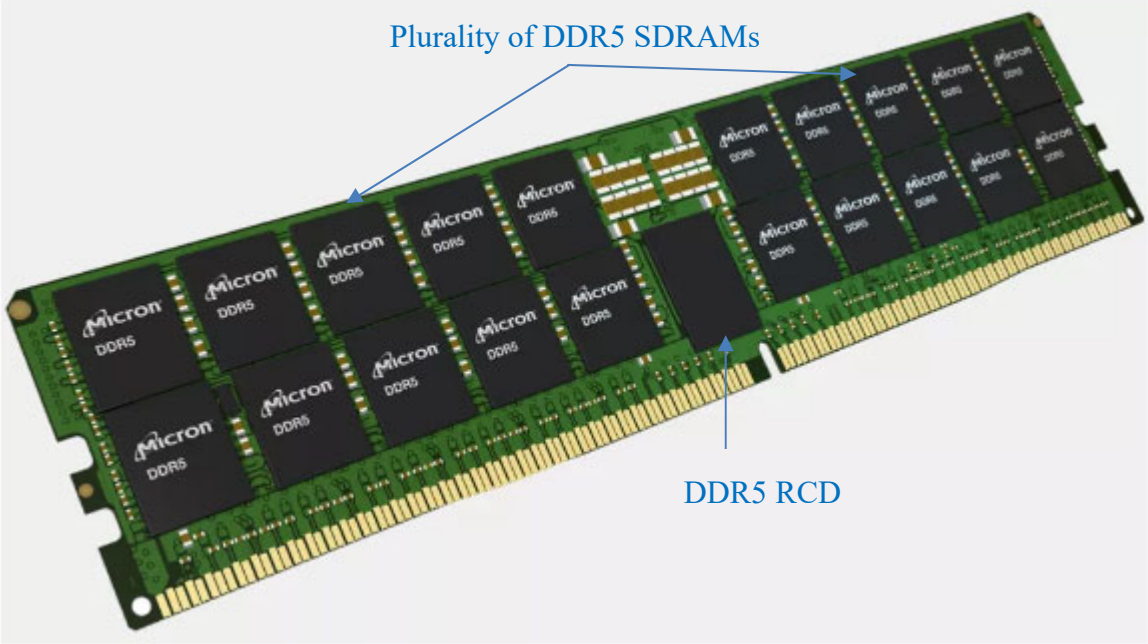


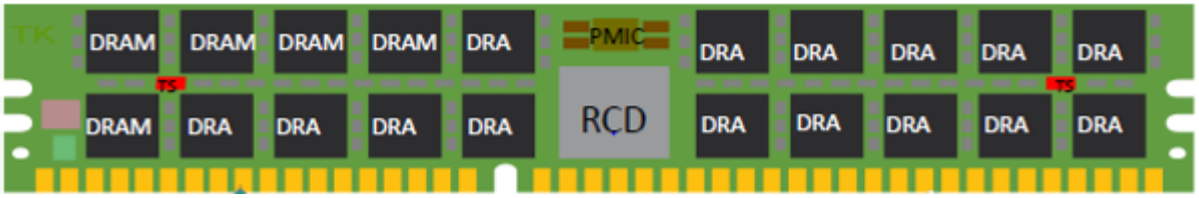
Figure 9 — Dual Phase Regulator Example Schematic

Ex. 21 (JEDEC Power Management Specification for DDR5) (annotated), at 19-20.

97. The accused DDR5 products further comprise a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising: a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and at least one circuit (*e.g.*, RCD) coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, as illustrated below.



Ex. 14 at 1 (annotated depiction of a Micron DDR5 RDIMM). *See also, e.g.*, Ex. 8 (Micron® DDR5: Key Module Features) at 1 (depicting DDR5 RDIMM with a plurality of components including DDR5 SDRAMs and RCD):



2.4 DDR5 SDRAM X4/8 Ballout using MO-210

Table 1 provides the ballout for DDR5 SDRAM X4/8 using MO-210.

Table 1 — DDR5 SDRAM X4/8 Ballout Using MO-210

AN	1	2	3	4	5	6	7	8	9	10	11	
AL		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	DNU	A
B		VDD	VDDQ	DQ2				DQ3	VDDQ	VDD		B
C		VSS	DQ0	DQS_t				DM_n, TDQS_t	DQ1	VSS		C
D		VDDQ	VSS	DQS_c				TDQS_c	VSS	VDDQ		D
E		VDD	DQ4	DQ6				DQ7	DQ5	VDD		E
F		VSS	VDDQ	VSS				VSS	VDDQ	VSS		F
G		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN		G
H		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		H
J		VDDQ	CA4	CA0				CA1	CA5	VDDQ		J
K		VDD	CA6	CA2				CA3	CA7	VDD		K
L		VDDQ	VSS	CA8				CA9	VSS	VDDQ		L
M		CAI	CA10	CA12				CA13	CA11	RESET_n		M
N	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU	N

Ex. 22 JEDEC 79-5 DDR5 SDRAM Standard), at 3.

Table 3 — Pinout Description (Continued)

Symbol	Type	Function
LBDQ	Output	Loopback Data Output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.1 V
VDD	Supply	Power Supply: 1.1 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 1.8V
ZQ	Reference	Reference Pin for ZQ calibration. This ball is tied to an external 240 ohm resistor(RZQ), which is tied to V_{SS}.

Id. at 6.

10.1 Operating Electrical Characteristics

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 189 — Operating Electrical Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage[1]	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V
V_{DDIO}	DDR5RCD01 Sideband Interface I/O Supply Voltage		0.95	1.0	1.05	V

Ex. 17 (JEDEC DDR5 RCD Standard, JESD 82-511), at 176.

98. The at least one circuit (*e.g.*, RCD) is operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices. For example:

3.1 Description

The DDR5RCD01 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

Id. at 5.

99. The at least one circuit is coupled to both the second regulated voltage and the fourth regulated voltage. For example, the RCD receives both VDDIO and VDD or VDDQ input, with the amplitude of VDDIO (*e.g.*, 1.0V) being less than the amplitude of VDD (*e.g.*, 1.1V) or VDDQ (*e.g.*, 1.1V).

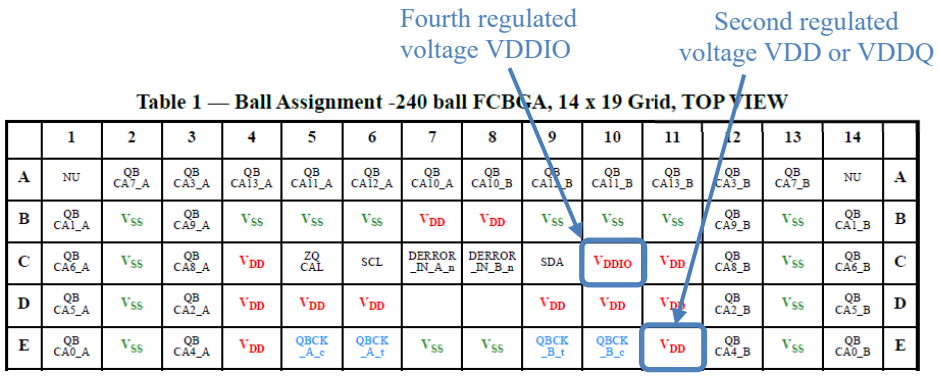


Table 1 — Ball Assignment -240 ball FCBGA, 14 x 19 Grid, TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NU	QB CA7_A	QB CA3_A	QB CA13_A	QB CA11_A	QB CA12_A	QB CA10_A	QB CA10_B	QB CA12_B	QB CA11_B	QB CA13_B	QB CA3_B	QB CA7_B	NU	A
B	QB CA1_A	V_{SS}	QB CA9_A	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	QB CA9_B	V_{SS}	QB CA1_B	B
C	QB CA6_A	V_{SS}	QB CA8_A	V_{DD}	ZQ CAL	SCL	DERROR _IN_A_n	DERROR _IN_B_n	SDA	V_{DDIO}	V_{DD}	QB CA8_B	V_{SS}	QB CA6_B	C
D	QB CA5_A	V_{SS}	QB CA2_A	V_{DD}	V_{DD}	V_{DD}			V_{DD}	V_{DD}	V_{DD}	QB CA2_B	V_{SS}	QB CA5_B	D
E	QB CA0_A	V_{SS}	QB CA4_A	V_{DD}	QBCK _A_c	QBCK _A_t	V_{SS}	V_{SS}	QBCK _B_t	QBCK _B_c	V_{DD}	QB CA4_B	V_{SS}	QB CA0_B	E

Id. at 3.

100. Micron's infringement of the '918 Patent has damaged and will continue to damage Netlist. Micron has had actual notice of the '918 Patent since at least the filing of this Complaint.

VII. FOURTH CLAIM FOR RELIEF – '054 PATENT

101. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

102. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '054 Patent by, among other things, making, using, selling,

offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR5 LRDIMMs, DDR5 RDIMMs, DDR5 SODIMMs, DDR5 UDIMMs, and other products with materially the same structures in relevant parts. For example, and as shown below, the accused DDR5 memory modules and other products with materially the same structures in relevant parts infringe at least one claim of the '054 Patent.

103. For example, the accused DDR5 products comprise a memory module comprising a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system. *See* illustration below (reproduced from Ex. 10 at 1).

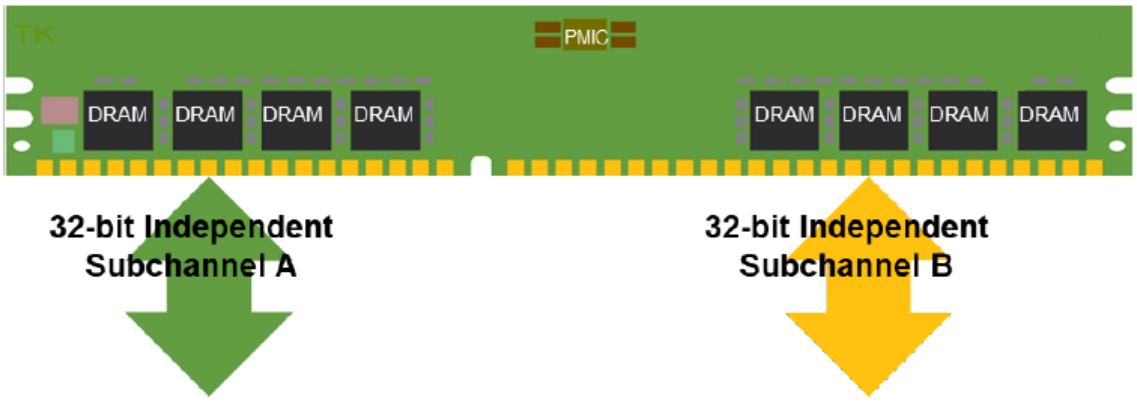


Figure 1: DDR5 1Rx8 UDIMM Module Illustrating Two Independent Subchannels

104. The accused DDR5 products further comprise a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages. For example, Micron UDIMMs and SODIMMs include the following basic configuration for a PMIC (Ex. 10 at 2-3). VDD, VDDQ and VPP are regulated voltages produced by buck converters, SWA, SWB and SWC.

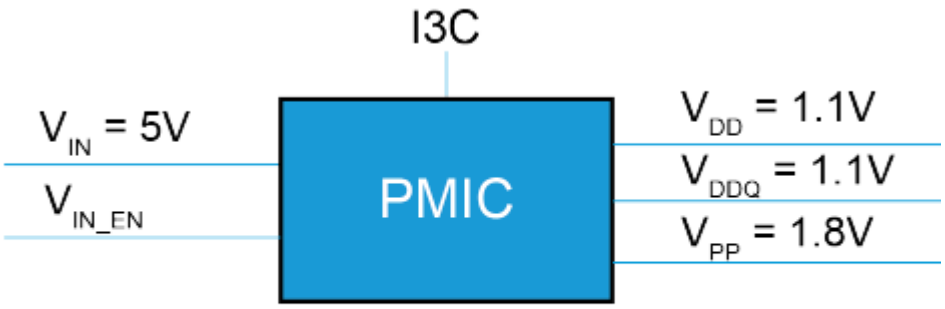


Figure 2: DDR5 Client PMIC (Basic Diagram)

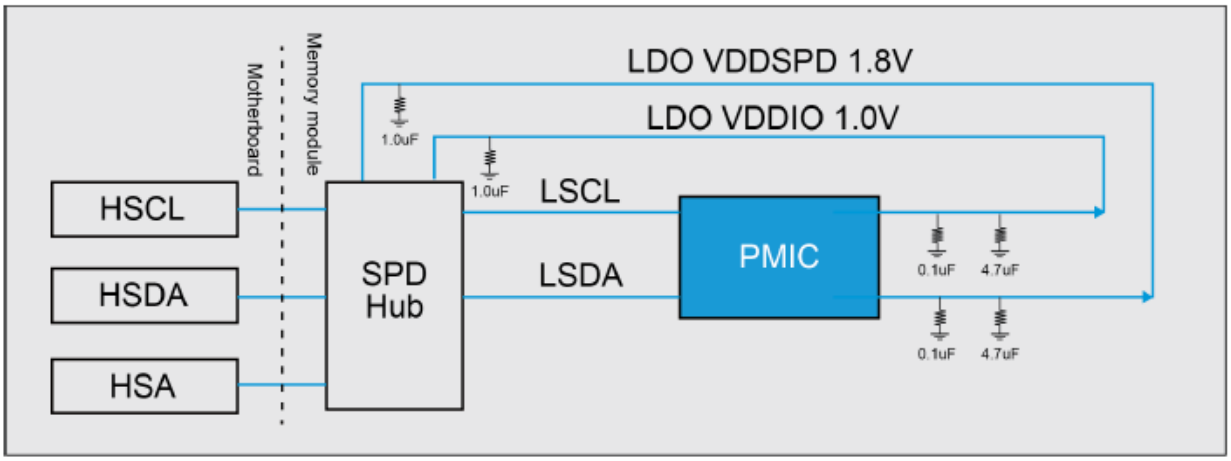
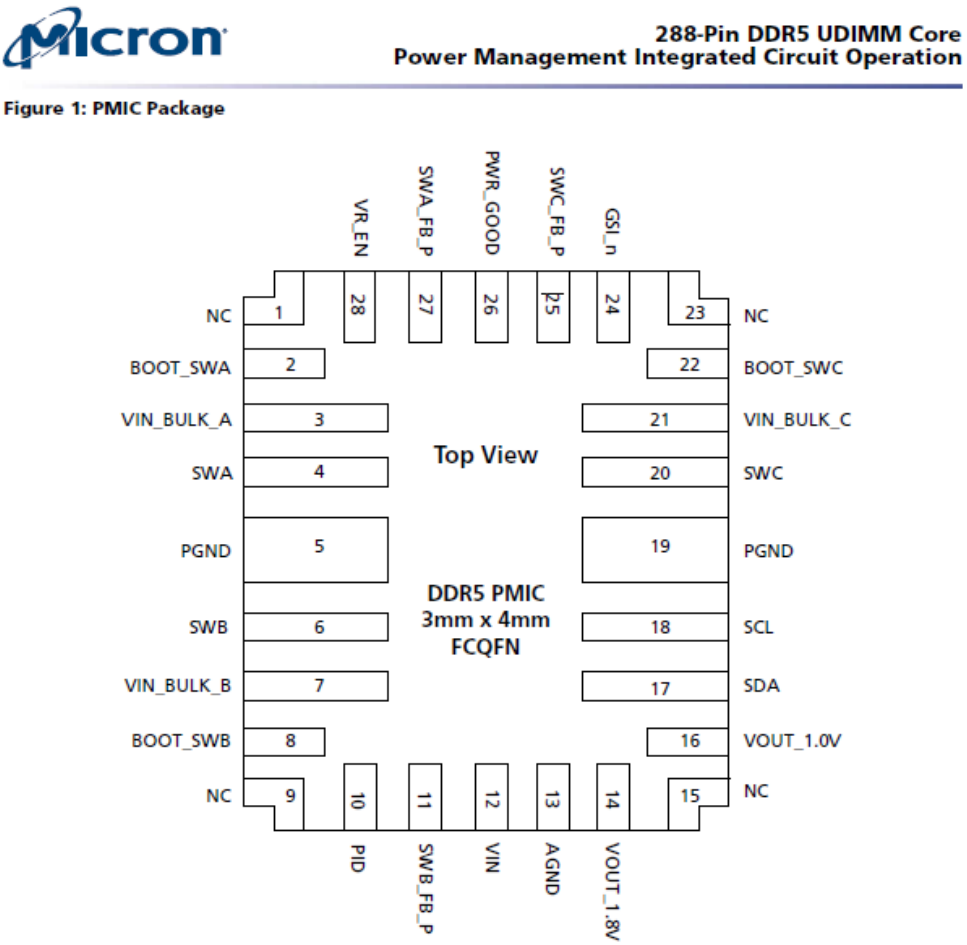


Figure 3: DDR5 Client SPD Hub (Basic Diagram)

See also Ex. 13 at 13 (schematic diagram of PMIC on Micron's DDR5 DIMMs):



105. The voltage conversion circuit, which includes the relevant parts of PMIC, *e.g.*, the inductors, capacitors, and other necessary elements that comprise at least three buck converters, provides the at least three required regulated voltages. The regulated voltages include VDD, VDDQ, VPP, among others. On information and belief, the magnitude of these regulated voltages are programmable. *See*, *e.g.*, Ex. 8 (Micron® DDR5: Key Module Features) at 2 ("The PMIC provides the brains of a smart voltage regulation system for the DDR5 DIMM, enabling configurability of voltage ramps and levels as well as current monitoring."). For example, VDD and VDDQ can be programmed to have an amplitude of 1.1V. As another example, VPP can be a regulated voltage at 1.8V. DRAMs on the PCB are each coupled to the VDD, VDDQ and VPP regulated voltages. The voltage conversion circuit can also have other voltage regulators,

including linear voltage dropout regulators. Outputs from these other voltage regulators include, *e.g.*, a 1.8V output for powering components such as SPD, and a 1.0V output that may also be used to power SPD or where applicable, components such as a RCD that is present in RDIMMs and LRDIMMs. The observed voltages and behavior are consistent with the latest DDR5 standards, within error tolerance. *See supra*, ¶¶ 96-99. For example, the datasheet for Micron's DDR5 UDIMM products indicates that the PMIC provides the required voltage amplitudes listed above:

Table 1: Product Family Attributes

Parameter	Options	Notes
DIMM organization	x64, x72 ECC	Two 32-bit sub-channels (non-ECC), two 36-bit sub-channels (ECC)
DIMM dimensions (nominal)	133.35mm x 31.25mm	Refer to Module Dimensions
Pin count	288	
DDR5 SDRAM densities supported	16Gb, 24Gb, 32Gb, 64Gb	78/82-ball FBGA package for x4/x8 devices
Capacity	8Gb–128GB	
DDR5 SDRAM width	x8, x16	
Data transfer rate	PC5-3200 to PC5-5600	Refer to Key Timing Parameters
Serial presence detect hub with temperature sensor	1024 byte	
Voltage (external supply, nominal)	V_{IN_Bulk}: 5V	Bulk input DC supply voltage from system
Voltage (PMIC output)	V_{DD}: 1.1V	Supply voltage from PMIC
	V_{DDQ}: 1.1V	I/O Supply voltage from PMIC
	V_{PP}: 1.8V	Pump voltage from PMIC
	1.8V LDO output	From PMIC to HUB
	1.0V LDO output	
Interface	1.1V signaling	
DRAM operating temperature	T_{OPER} = 0 to 95°C	Refer to Thermal Characteristics

106. The accused DDR5 products further comprise a plurality of components (such as DRAM devices, thermal sensors, SPD and, where applicable, RCD and data buffers) coupled to the PCB, each component of which is coupled to at least one regulated voltage of the plurality of regulated voltages, including a plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages, such as VDD.

107. The accused DDR5 products further comprise a controller coupled to the PCB, which includes a voltage monitor circuit coupled to an input voltage, such as VIN_BULK or where applicable, VIN_MGMT, received from the host system via the interface. The controller and the

voltage monitoring circuit may be part of the PMIC. In response to the voltage monitor detecting an amplitude change in the input voltage (*e.g.*, an over- or under-voltage condition on the input power pins), the memory module transitions from a first operable state (*e.g.*, with all components operating normally) to a second operable state (*e.g.*, with the PMIC, thermal sensors, and/or SPD still operating, but not necessarily all components operating). *See e.g.*, Ex. 21 (JEDEC Power Management Specification for DDR5) at 2, 37, 40:

2.2 Common Features summary

Table 1 — PMIC Device Type Summary

Device Type	SWA	SWB	SWC	SWD	Unit
PMIC5000 - Current Capability per Phase	5	5	5	5	A
PMIC5010 - Current Capability per Phase	3	3	3	3	A

- VIN_Bulk input supply range: 4.25 V to 15.0 V
- VIN_Mgmt input supply range: 3.0 V to 3.6 V
- Four step down switching regulators: SWA, SWB, SWC & SWD
- Programmable dual phase and single phase regulator for SWA and SWB
- 3 LDO regulators: VBias, VOUT_1.8V, VOUT_1.0V
- Automatic switchover from VIN_Mgmt input supply to VIN_Bulk input supply
- Error injection capability
- Persistent Error log registers
- Secure mode and programmable of operation
- Independently programmable output voltages, power up and power down sequence for switch regulators
- Input and output power good status reporting mechanism
- VIN_Bulk input supply protection feature: Input over voltage
- Output switch regulators protection feature: Output over voltage, output under voltage, output current limiter
- Output current and power measurement, output current threshold mechanism
- Temperature measurement, temperature warning threshold, critical temperature shutdown
- Multi Time Programmable Non-Volatile Memory
- Programmable and DIMM specific registers for customization
- General Status Interrupt Function
- Flexible Open Drain IO (I^2C) and Push Pull (I3C Basic) IO Support

Table 30 — Events Interrupt Summary

Event	Status Bit	Clear Bit	Mask Bit	Threshold Bits	Trigger VR Disable?	PWR_GOOD Output	GSI_n Output
VIN_Bulk Power Good	R08 [7]	R10 [7]	R15 [7]	R1A [7:5]	No	Low	Low
VIN_Bulk Over Voltage	R08 [0]	R10 [0]	R15 [0]	R1B [7]	Yes	Low	Low
VIN_Mgmt Over Voltage	R08 [1]	R10 [1]	R15 [1]	R1B [5]	No	High	Low
SWA Output Power Good	R08 [5]	R10 [5]	R15 [5]	R21 [1:0]; R22 [7:6]	No	Low	Low
SWB Output Power Good	R08 [4]	R10 [4]	R15 [4]	R23 [1:0]' R24 [7:6]	No	Low	Low
SWC Output Power Good	R08 [3]	R10 [3]	R15 [3]	R25 [1:0]; R26 [7:6]	No	Low	Low
SWD Output Power Good	R08 [2]	R10 [2]	R15 [2]	R27 [1:0]; R28 [7:6]	No	Low	Low
1.8 V LDO Power Good	R09 [5]	R11 [5]	R16 [5]	R1A [2]	No	Low	Low
1.0 V LDO Power Good	R33 [2]	R14 [2]	R19 [2]	R1A [0]	No	Low	Low
VBias LDO Power Good	R09 [6]	R11 [6]	R16 [6]	R1A [3]	No	Low	Low
SWA Output Over Voltage	R0A [7]	R12 [7]	R17 [7]	R22 [5:4]	Yes	Low	Low
SWB Output Over Voltage	R0A [6]	R12 [6]	R17 [6]	R24 [5:4]	Yes	Low	Low
SWC Output Over Voltage	R0A [5]	R12 [5]	R17 [5]	R26 [5:4]	Yes	Low	Low
SWD Output Over Voltage	R0A [4]	R12 [4]	R17 [4]	R28 [5:4]	Yes	Low	Low
SWA Output Under Voltage	R0B [3]	R13 [3]	R18 [3]	R22 [3:2]	Yes	Low	Low
SWB Output Under Voltage	R0B [2]	R13 [2]	R18 [2]	R24 [3:2]	Yes	Low	Low
SWC Output Under Voltage	R0B [1]	R13 [1]	R18 [1]	R26 [3:2]	Yes	Low	Low
SWD Output Under Voltage	R0B [0]	R13 [0]	R18 [0]	R28 [3:2]	Yes	Low	Low
VBias LDO Output or VIN_Bulk Input Under Voltage	R33 [3]	R14 [3]	R19 [3]	Vendor Specific	Yes	Low	Low
SWA Output Current Limit	R0B [7]	R13 [7]	R18 [7]	R20 [7:6]	No	High	Low
SWB Output Current Limit	R0B [6]	R13 [6]	R18 [6]	R20 [5:4]	No	High	Low
SWC Output Current Limit	R0B [5]	R13 [5]	R18 [5]	R20 [3:2]	No	High	Low
SWD Output Current Limit	R0B [4]	R13 [4]	R18 [4]	R20 [1:0]	No	High	Low
SWA Output High Current/Power	R09 [3]	R11 [3]	R16 [3]	R1C [7:2]	No	High	Low
SWB Output High Current/Power	R09 [2]	R11 [2]	R16 [2]	R1D [7:2]	No	High	Low
SWC Output High Current/Power	R09 [1]	R11 [1]	R16 [1]	R1E [7:2]	No	High	Low
SWD Output High Current/Power	R09 [0]	R11 [0]	R16 [0]	R1F [7:2]	No	High	Low
High Temperature Warning	R09 [7]	R11 [7]	R16 [7]	R1B [2:0]	No	High	Low
Critical Temperature	R08[6]	N/A	N/A	R2E [2:0]	Yes	Low	Low
VIN_Mgmt to VIN_Bulk Switchover	R09 [4]	R11 [4]	R16 [4]	R2F [7]	No	High	Low
Valid VIN_Mgmt in Switchover State	R33 [4]	R14 [4]	R19 [4]	N/A	No	High	Low
PEC Error	R0A [3]	R12 [3]	R17 [3]	N/A	No	High	Low
Parity Error	R0A [2]	R12 [2]	R17 [2]	N/A	No	High	Low

8.15 Input Over Voltage Protection

An input over voltage protection mechanism is implemented to limit the voltages to the PMIC. The PMIC actively monitors the input voltage VIN_Bulk and VIN_Mgmt rail.

There are two possibilities where PMIC recognizes the input over voltage event.

1. VIN_Mgmt input goes above the threshold set in register Table 122, "Register 0x1B" [5].
2. VIN_Bulk input goes above the threshold set in register Table 122, "Register 0x1B" [7].

When either one or both event occurs for a period longer than tInput_OV_GSI_Assertion time then PMIC sets the register Table 103, "Register 0x08" [1:0] accordingly and drives GSI_n output signal as shown in Table 30 at the same time. Note that at this point, the PMIC does not assert PWR_GOOD output signal. The PMIC allows access to all registers and PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may clear the VIN_Mgmt or VIN_Bulk input over voltage status register by writing '1' to register Table 111, "Register 0x10" [1:0] appropriately or by writing '1' to global status clear register Table 115, "Register 0x14" [0]. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status register Table 103, "Register 0x08" [1:0] will remain at '1'.

108. Furthermore, in response to the detected over- or under- voltage, the controller is configured to perform operations such as a write operation that records predefined bit value(s) in a register. The register is a non-volatile memory because the information written to the register by the controller is retained even after power-off. *See, e.g.*, *id.* at 105, 112:

14.2 Register Map Breakdown

Table 96 — Register Map Breakdown

Register Range	Region	Comments
0x00 - 0x3F	Host Region	Host Accessible Registers
0x40 - 0x6F	DIMM Vendor Region	DIMM Vendor Registers - Non Volatile Memory Allows DIMM vendors to program the PMIC for a given DRAM/DIMM vendor designs. These are password protected registers and password is selected by DIMM vendor. Under normal operation, these registers are not used by any host. These registers require password for read access. Access to these registers without correct password will return all data as '0'. These registers require complete power cycle before it takes in effect. Changing these registers under normal operation is considered an illegal operation.
0x70 - 0xFF	Vendor Specific Region	Vendor Specific Registers - Non Volatile Memory These are vendor specific password protected registers. Under normal operation these registers are not used by any host. These registers require password for read access. Access to these registers without correct password will return all data as '0'.

Table 99 — Register 0x04

	R04		
Bits	Attribute	Default	Description[1,2]
7	ROE	0	R04 [7]: GLOBAL_ERROR_COUNT Global Error Count Since Last Erase Operation[3] 0 = No Error or Only 1 Error since last Erase operation 1 = > 1 Error Count since last Erase operation
6	ROE	0	R04 [6]: GLOBAL_ERROR_LOG_BUCK_OV_OR_UV Global Error Log History for Buck Regulator Output Over or Under Voltage[4] 0 = No Error Occurred 1 = Error Occurred
5	ROE	0	R04 [5]: GLOBAL_ERROR_LOG_VIN_BULK_OVER_VOLTAGE Global Error Log History for VIN_Bulk Over Voltage[4] 0 = No Error Occurred 1 = Error Occurred
4	ROE	0	R04 [4]: GLOBAL_ERROR_LOG_CRITICAL_TEMPERATURE Global Error Log History for Critical Temperature[4] 0 = No Error Occurred 1 = Error Occurred
3:0	RV	0	R04 [3:0]: Reserved

1. The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 5.0V for VIN_Bulk voltage and 100 ms duration from PWR_GOOD signal assertion to guarantee the write operation into non-volatile memory.
2. Host must explicitly perform Erase operation to erase this entire register Table 99, "Register 0x04" [7:0] via Table 151, "Register 0x39". The PMIC needs minimum of 100 ms for Erase operation.
3. PMIC counts the error since last erase operation and if more than one error occurs, it sets this bit to '1'. Host must explicitly perform Erase operation to erase this entire register Table 99, "Register 0x04" [7:0].
4. PMIC sets the bit when error occurs.

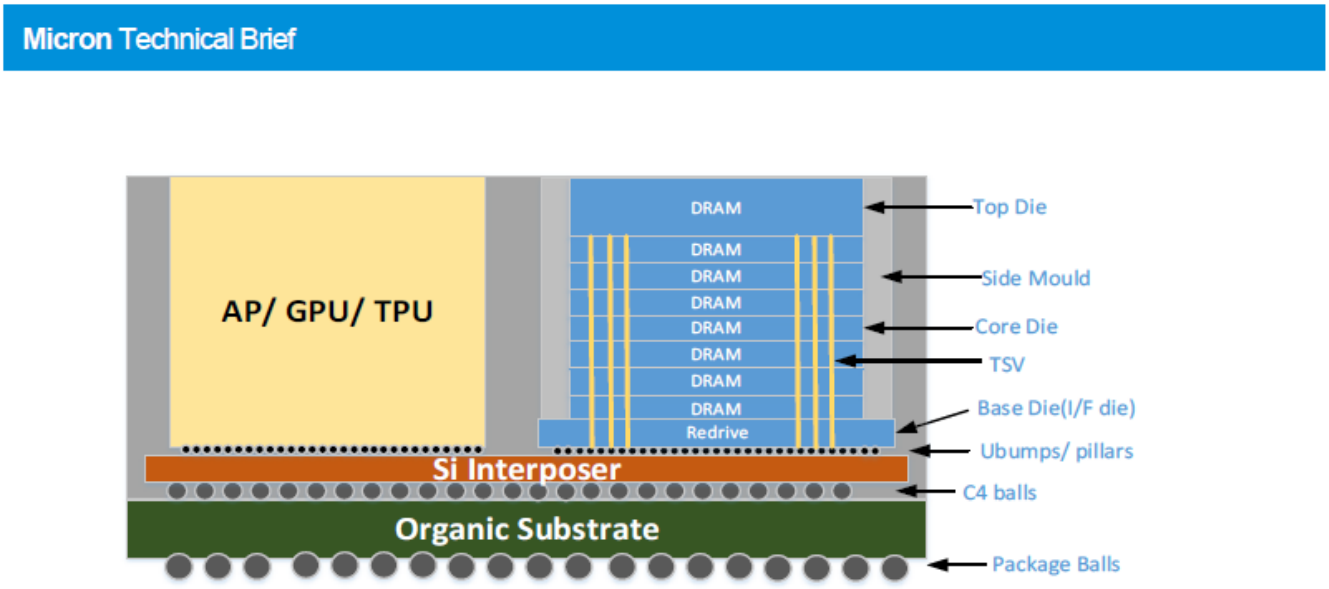
109. Micron's infringement of the '054 Patent has damaged and will continue to damage Netlist.

VIII. FIFTH CLAIM FOR RELIEF – '060 PATENT

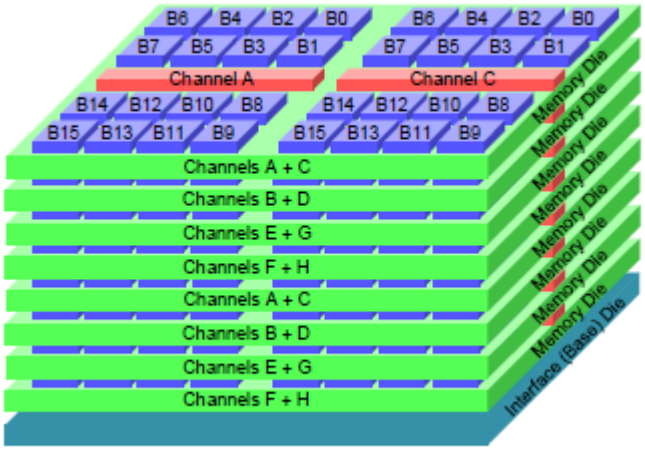
110. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

111. On information and belief, Defendants directly infringed and are currently infringing at least claim 20 of the '060 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused HBM Products, and other products with materially the same structure in relevant part. For example, and as shown below, the Accused HBM Products and other products with materially the same structure and operating mechanisms in relevant part infringe at least one claim of the '060 Patent.

112. The Accused HBM Products each include a plurality of array dies arranged in a stack (*e.g.*, 8 stacked DRAM dies). The plurality of array dies can be divided into at least two groups of array dies. The dies are interconnected via TSVs and associated bumps and bond pads. *See, e.g.*, Ex. 9 (Micron Technical Brief "Integrating and Operating HBM2E Memory") at 3 (providing a cross-sectional illustration of a system-in-package with Micron HBM2E) (annotations in original):



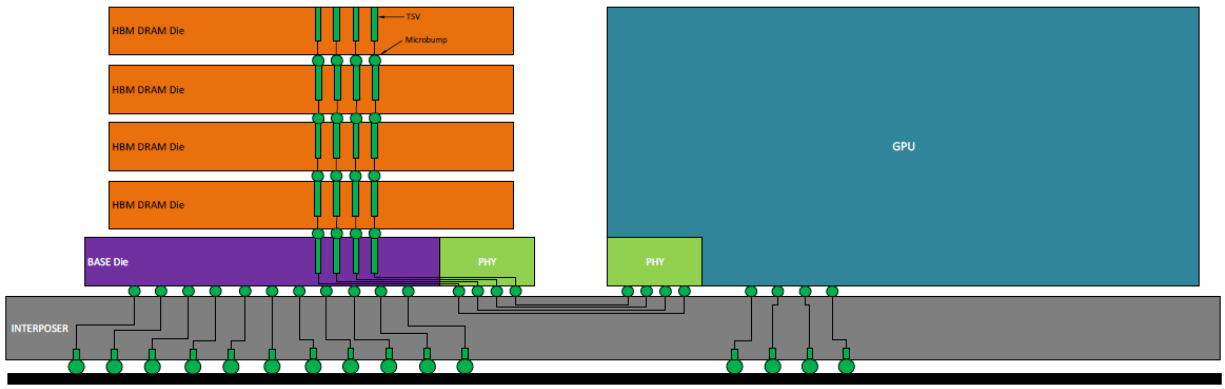
See also, e.g., *id.* (providing an example of HBM2E channel organization for a 8-high product):



113. The Accused HBM Products also have at least two die interconnects. For example, some TSVs only electrically interconnect some of the DRAM dies (first group of array die(s), selected from the group of DRAM dies that Micron annotates each individually as a "Core Die" or "Memory Die"), while others may electrically bypass this first group of array dies and electrically connect with the active transceiver logic of at least one of the other DRAM dies (second group of array die(s)). For instance, some TSVs may only be in electrical communication with

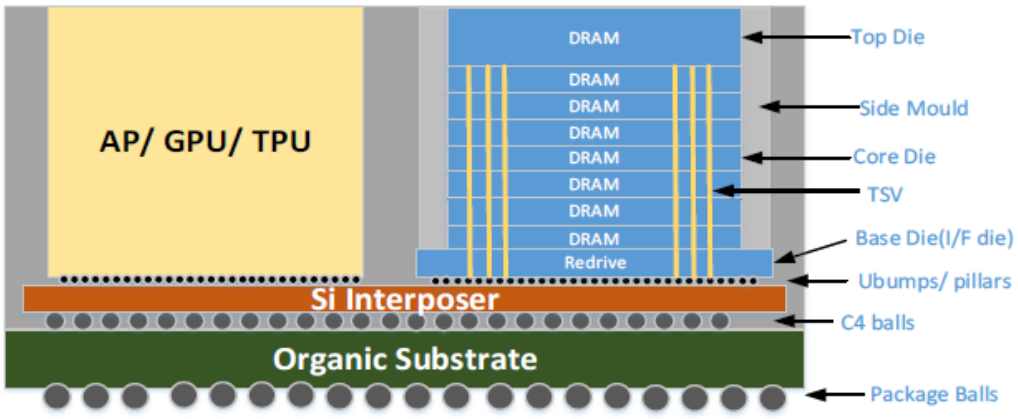
dies 0 and 4 with channels F+H, but not with any of the other DRAM dies. Others may only be in electrical communication with dies 1 and 5 (or 2 and 6, or 3 and 7), but not any of the other dies.

114. The Accused HBM Products also include a control die (*e.g.*, the bottom die in the image above, labeled by Micron as a "Interface (Base) Die"), with a plurality of input/output terminals, such as terminals for data and control/address signals via which the memory die stack communicates data and control/address signals with a CPU, GPU, FPGA, or other external dies. *See*, *e.g.*, Ex. 9 (Micron Technical Brief "Integrating and Operating HBM2E Memory") at 2 ("The HBM2E DRAM is soldered to a silicon interposer that routes all interface signals in very tiny traces to the host ASIC."); *see also* Ex. 11 (Micron white paper titled "The Demand for High-Performance Memory") at 2 (on information and belief, an 8-high product will have materially the same interconnect between the host and the HBM stack as the 4-high product illustrated below).



High-bandwidth memory leverages stacked memory components for density and high I/O counts

115. The control die also includes a first driver that drives data signal via the first die interconnects and a second driver that drives data signal via the second die interconnects. *E.g.*, *id.* at 6 ("The HBM2E interfaces use regular pull/push drivers with programmable driver strength for signaling."). *See, e.g.*, Ex. 9 (Micron Technical Brief "Integrating and Operating HBM2E Memory") at 3, 5 (annotations in original):



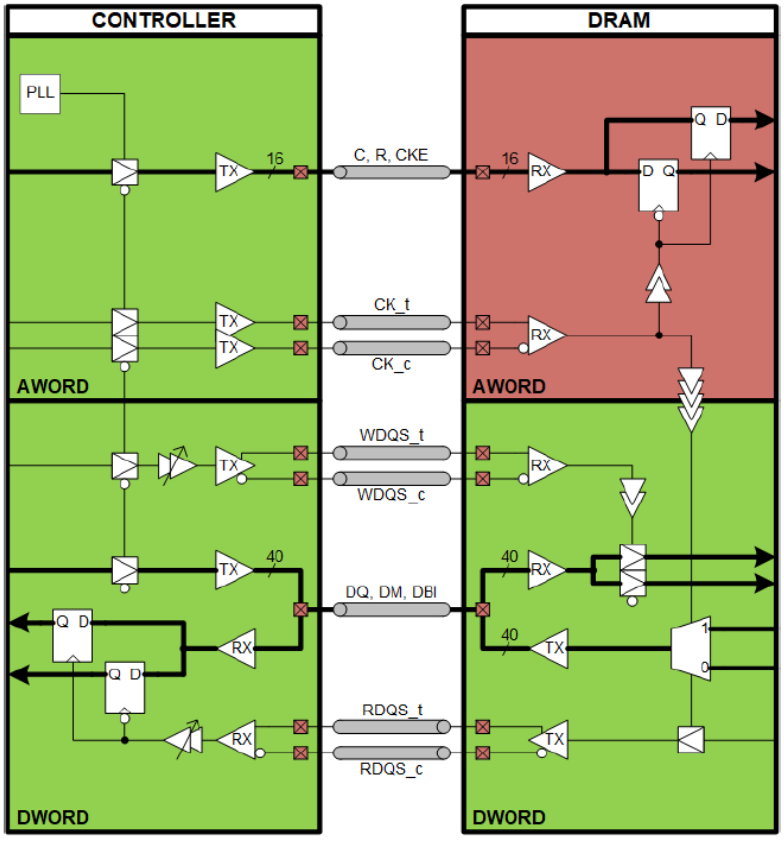


Figure 7: HBM2E DRAM Clocking Scheme

116. The operation of the Accused HBM Products includes a step of receiving a data signal at a first terminal (*e.g.*, a data terminal) of the input/output terminals and a step of receiving a control signal at second terminals (*e.g.*, control/address terminals) of the input/output terminals.

117. Chip select signals, which may be encoded in the received stack ID ("SID") signals, each select an array die to which data signals are to be driven by the corresponding data driver via the corresponding die interconnects. The Accused HBM Products select one of the first driver and the second driver in accordance with the chip select signal(s) to drive the data signal to the selected array die via the corresponding first or second die interconnect.

118. Micron's infringement of the '060 Patent has damaged and will continue to damage Netlist.

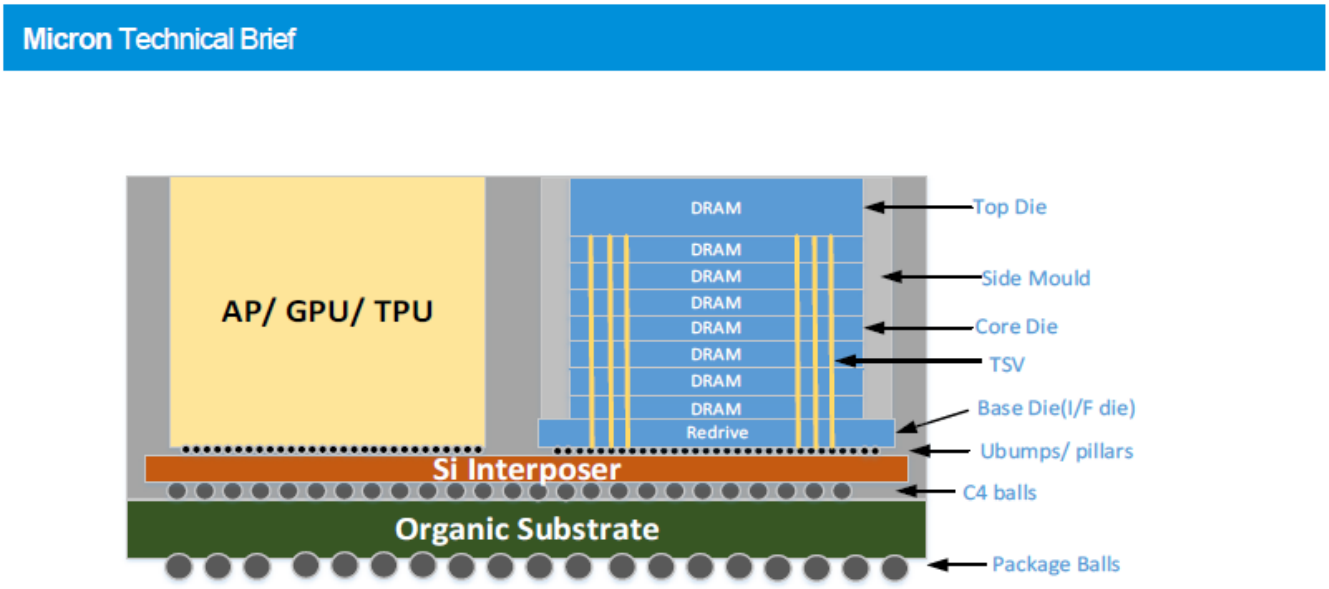
IX. SIXTH CLAIM FOR RELIEF – '160 PATENT

119. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

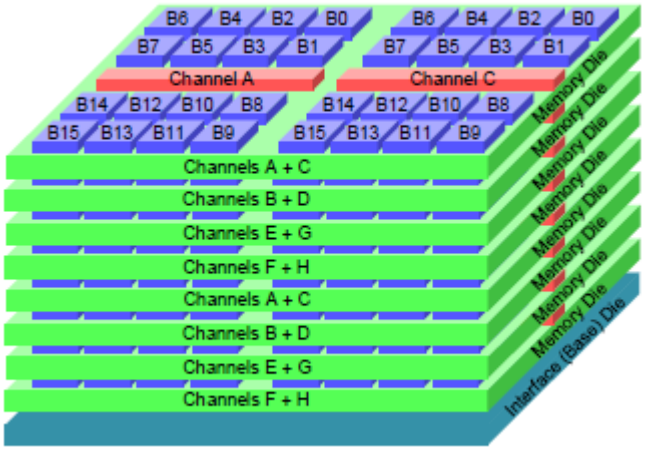
120. On information and belief, Defendants directly infringed and are currently infringing at least claim 1 of the '160 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused HBM Products, and other products with materially the same structure in relevant part. For example, and as shown below, the Accused HBM Products and other products with materially the same structure in relevant part infringe at least one claim of the '160 Patent.

121. For example, the Accused HBM Products include terminals for data and terminals for control signals (*e.g.*, command and address signals). *See*, *e.g.*, Ex. 12 (Datasheet for Micron 8GB/16GB HBM2E), Table 1 ("HBM2 Signal Descriptions").

122. The Accused HBM Products also each include stacked array dies (*e.g.*, 8 stacked DRAM dies) including at least two groups of array dies. The dies are interconnected via TSVs and associated bumps and bond pads. *See* Ex. 9 (Micron Technical Brief "Integrating and Operating HBM2E Memory") at 3:



See also, e.g., *id.* (providing an example of HBM2E channel organization for a 8-high product):



123. The Accused HBM Products also have at least two interconnects, each in electrical communication with one group of array dies but not in communication with a second group of array dies. For example, first die interconnects are in electrical communication with a first group of array dies and not in electrical communication with a second group of at least one array die; and second die interconnects are in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies. This may be achieved by electrically coupling certain TSVs with active transceiver logic for only a subset of

the dies. For example, some TSVs may only interconnect some of the DRAM dies (first group of array dies) and some may bypass this first group of DRAM dies and electrically connect with the active transceiver logic of at least some of the other DRAM dies (second group of array dies).

124. The Accused HBM Products also each include a control die (*e.g.*, the bottom "Base Die" in the image above). The control die includes first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals. The data conduit includes first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies; and the second data conduit include second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die. The second driver size is different from the first driver size, for example, to account for the different distances data signals have to travel to reach the respective array dies in the stack. *E.g.*, Ex. 9 at 6 ("The HBM2E interfaces use regular pull/push drivers with programmable driver strength for signaling.").

125. Micron's infringement of the '160 Patent has damaged and will continue to damage Netlist.

X. DEMAND FOR JURY TRIAL

126. Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

XI. PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Micron infringes the Patents-in-Suit;

B. all equitable relief the Court deems just and proper as a result of Micron's infringement;

C. an award of damages resulting from Micron's acts of infringement in accordance with 35 U.S.C. § 284;

D. enhanced damages pursuant to 35 U.S.C. § 284;

E. that Micron's infringement of the '506 and '339 patents is willful;

F. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

G. an accounting for acts of infringement and supplemental damages, without limitation, pre-judgment and post-judgment interest; and

H. such other equitable relief which may be requested and to which Netlist is entitled.

Dated: June 10, 2022

Respectfully submitted,

/s/ Draft

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