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20   **IN THE UNITED STATES DISTRICT COURT**

21   **FOR THE SOUTHERN DISTRICT OF CALIFORNIA**

22

23   BELL SEMICONDUCTOR, LLC,   Case No. **'22CV594 BEN KSC**

24   Plaintiff,

25   v.   **COMPLAINT**

26   NXP USA, INC.,   **DEMAND FOR JURY TRIAL**

27   Defendant.

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MCKOOL SMITH HENNIGAN, P.C.
LOS ANGELES, CA

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Plaintiff Bell Semiconductor, LLC ("Bell Semic" or "Plaintiff") brings this Complaint against Defendant NXP USA, Inc. ("NXP") for infringement of U.S. Patent No. 7,007,259 ("the '259 patent"). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1.   This is a patent infringement suit relating to NXP's unauthorized and unlicensed use of the '259 patent. The circuit design methodology claimed in the '259 patent is used by NXP in the production of one or more of its semiconductor chips, including its NXP LS1043A Quad-Core Networking Processor.

2.   This is a patent infringement suit relating to NXP's unauthorized and unlicensed use of the '259 patent. The circuit design methodology and system claimed in the '259 patent is used by NXP in the production one or more of its semiconductor chips, including its NXP LS1043A Quad-Core Networking Processor.

3.   Semiconductor devices include different kinds of materials to function as intended. For example, these devices typically include both metal (i.e., conductor) and insulator materials, which are deposited or otherwise processed sequentially in layers to form the final device. These layers—and the interconnects and components formed within them—have gotten much smaller over time, increasing the performance of these devices dramatically. As a result, it has become even more important to keep the layers planar as the device is being built because defects and warpage can cause fabrication issues and malfunctioning of the device. Manufacturers use a process called Chemical Mechanical Planarization/Polishing ("CMP") to smooth out the surface of the device periodically between deposition and/or etching of each layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be "polished" away at

COMPLAINT

1   different rates, leading to erosion or dishing on the surface. To reduce this problem

2   "dummy" material, also known as "dummy fill," is typically inserted into low-density

3   regions of the device to increase the overall uniformity of the structures on the surface

4   of the layer and reduce the density variability across the surface of the device.

5   However, dummy fill can increase capacitance if it is placed too close to signal wires,

6   which slows the transmission speed of signals and degrades the overall performance

7   of the device.

8   4.   Prior to development of the methodology described in the '259 patent,

9   the most widely implemented technology for insertion of dummy metal into a circuit

10   design required hardcoding a large "stay–away" distance between the dummy metal

11   and clock nets, which led to less space available for dummy metal insertion. This

12   methodology often made it impossible to insert enough dummy metal to meet the

13   required minimum density. The traditional dummy fill tools would often complete

14   their run without reaching the minimum density, thus requiring at least a second run of

15   the tool for the problem areas. In each problem area, the "stay-away" distance was

16   reduced manually. And if there was more than one problem area, the manufacturer

17   would have to make multiple runs of the tool, as it would have to address one problem

18   area at a time. This was an involved, iterative process that had the potential to

19   negatively impact the fabrication schedule and potentially the yield of the run, causing

20   costs to go up.

21   5.   Vikram Shrowty and Santhanakrishnan Raman ("the Inventors"), the

22   inventors of the '259 patent, understood the drawbacks of this "stay-away" design

23   process and set out to develop a more efficient method for inserting dummy metal into

24   a circuit design. The Inventors ultimately conceived of a dummy fill procedure that

25   minimizes the negative timing impact of dummy metal on clock nets, while still

26   achieving minimum density in a single run. The claimed invention begins by

27   identifying free spaces on each layer of the circuit design suitable for dummy metal

28   insertion as dummy regions. The dummy regions are then prioritized such that the

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1   dummy regions located adjacent to clock nets are filled with dummy metal last,

2   thereby minimizing any timing impact on the clock nets.

3   6.   The inventions disclosed in the '259 patent provide many advantages

4   over the prior art. In particular, they provide a simple and efficient method for dummy

5   metal insertion that minimizes the timing impact to clock nets and at the same time

6   guarantees reaching minimum density in a single pass. *See* Ex. A at 6:11–15. As

7   mentioned above, the patented invention results in the dummy regions being

8   prioritized such that the dummy regions located adjacent to clock nets are filled with

9   dummy metal last, thereby minimizing the timing impact on the clock nets. *See* Ex. A

10   at 2:29–47. Additionally, some embodiments of the patented invention further

11   prioritize the dummy regions such that the dummy regions adjacent to wider clock

12   nets are filled with dummy metal after dummy regions that are located adjacent to

13   narrower clock nets. *See* Ex. A at 2:35–39. These significant advantages are achieved

14   through the use of the patented inventions and thus the '259 patent presents significant

15   commercial value for companies like NXP.

16   7.   Bell Semic brings this action to put a stop to NXP's unauthorized and

17   unlicensed use of the inventions claimed in the '259 patent.

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THE PARTIES

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19   8.   Plaintiff Bell Semic is a limited liability company organized under the

20   laws of the State of Delaware with a place of business at One West Broad Street, Suite

21   901, Bethlehem, PA 18018.

22   9.   Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs

23   sprung out of the Bell System as a research and development laboratory, and

24   eventually became known as one of America's greatest technology incubators. Bell

25   Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was

26   widely considered one of the most important technological breakthroughs of the time,

27   earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial

28   transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its

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1   transistor patents to companies throughout the world, creating a technological boom

2   that led to the use of transistors in the semiconductor devices prevalent in most

3   electronic devices today.

4   10.   Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900

5   worldwide patents and applications, approximately 1,500 of which are active United

6   States patents. This patent portfolio of semiconductor–related inventions was

7   developed over many years by some of the world's leading semiconductor companies,

8   including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI

9   Corporation ("LSI"). This portfolio reflects technology that underlies many important

10   innovations in the development of semiconductors and integrated circuits for high–

11   tech products, including smartphones, computers, wearables, digital signal processors,

12   IoT devices, automobiles, broadband carrier access, switches, network processors, and

13   wireless connectors.

14   11.   The principals of Bell Semic all worked at Bell Labs' Allentown facility,

15   and have continued the rich tradition of innovating, licensing, and helping the industry

16   at large since those early days at Bell Labs. For example, Bell Semic's CTO was an

17   LSI Fellow and Broadcom Fellow. He is known throughout the world as an innovator

18   with more than 300 patents to his name, and he has a sterling reputation for helping

19   semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus

20   from the semiconductor world to work with Nortel Networks in the telecom industry

21   during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel

22   retirees and employees. In addition, several Bell Semic executives previously served

23   as engineers at many of these companies and were personally involved in creating the

24   ideas claimed throughout Bell Semic's extensive patent portfolio.

25   12.   On information and belief, NXP has a place of business in this District at

26   Innovation Drive, Suite 150, San Diego, CA 92128. On information and belief, NXP

27   develops, designs, and/or manufactures products in the United States, including in this

28   District, according to the '259 patented process/methodology; and/or uses the '259

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patented process/methodology in the United States, including in this District, to make products; and/or distributes, markets, sells, or offers to sell in the United States and/or imports products into the United States, including in this District, that were manufactured or otherwise produced using the patented process. Additionally, NXP introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

JURISDICTION AND VENUE

13.   This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

14.   This Court has personal jurisdiction over NXP under the laws of the State of California, due at least to its substantial business in California and in this District. NXP has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of California, and in this District by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of California and in this District, NXP, directly or through intermediaries:(i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the '259 patented process/methodology; (iii) distributes, markets, sells, or offers to sell products formed according to the '259 patented process/methodology; and/or (iv) imports products formed according to the '259 patented process/methodology.

15.   On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because NXP has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, NXP maintains a regular and established place of business at Innovation Drive, Suite 150, San Diego, CA 92128.

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COMPLAINT

16.   Currently, NXP is advertising 32 jobs at its San Diego location. These positions include those that relate to the '259 patented technology, such as positions for a Senior Firmware Manager, SoC Hardware Architect – Security, Principal System Integration Engineer, Principal Verification Engineer, Principal Digital Design Engineer, and SoC Hardware Architect. *See* https://nxp.wd3.myworkdayjobs.com/careers?Location_Country=bc33aa3152ec42d4995f4791a106ed09&locations=98d67abaaa8a100fa6344859d7d49369 (last visited April 25, 2022).

17.   Venue is also convenient in this District. this is at least true because of this District's close ties to this case—including the technology, relevant witnesses, and sources of proof noted above—and its ability to quickly and efficiently move this case to resolution.

18.   On information and belief, Bell Semic's cause of action arises directly from NXP's circuit design work and other activities in this District. Moreover, on information and belief, NXP has derived substantial revenues from its infringing acts occurring within the State of California and within this District.

U.S. PATENT NO. 7,007,259

19.   Bell Semic is the owner by assignment of the '259 patent. The '259 patent is titled "Method for Providing Clock-Net Aware Dummy Metal Using Dummy Regions." The '259 patent issued on February 28, 2006. A true and correct copy of the '259 patent is attached as Exhibit A.

20.   The inventors of the '259 patent are Vikram Shrowty and Santhanakrishnan Raman.

21.   The application that resulted in the issuance of the '259 patent was filed on July 31, 2003. The '259 patent claims priority to July 31, 2003.

22.   The '259 patent generally relates to "methods for patterning dummy metal to achieve planarity for chemical-mechanical polishing of integrated circuits,

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1   and more particularly to a dummy fill software tool that provides clock-net aware

2   dummy metal using dummy regions." Ex. A at 1:7–11.

3   23.   The background section of the '259 patent identifies the shortcomings of

4   the prior art. More specifically, the specification describes that the prior circuit design

5   methodology was disadvantageous because it was "often impossible to insert enough

6   dummy metal into a tile to meet the required minimum density without reducing the

7   large dummy-to-clock distance." Ex. A at 2:3–10. Use of this design process meant

8   that a second run of the metal-fill tool was often required in order to meet the density

9   requirements for all of the tiles. Ex. A at 2:10–14. Having to rerun the tool to meet the

10   density requirements made the design process an "involved, iterative process[,]"

11   which could "significantly impact the design schedule." Ex. A at 2:14–18.

12   24.   In light of the drawbacks of the prior art, the Inventors recognized the

13   need to "minimize[] the negative timing impact of dummy metal on clock nets, while

14   at the same time achieving minimum density in a single run." Ex. A at 2:19–23. The

15   inventions claimed in the '259 patent addresses this need.

16   25.   The '259 patent contains three independent claims and 37 total claims,

17   covering a method and computer readable medium for circuit design. Claim 1 reads:

18   1.   A method for inserting dummy metal into a circuit design, the

19   circuit design including a plurality of objects and clock nets, the method

20   comprising:

21   (a)   identifying free spaces on each layer of the circuit design

22   suitable for dummy metal insertion as dummy regions, and

23   (b)   prioritizing the dummy regions such that the dummy regions

24   located adjacent to clock nets are filled with dummy metal last,

25   thereby minimizing any timing impact on the clock nets.

26   26.   This claim, as a whole, provides significant benefits and improvements to

27   the function of the semiconductor device, *e.g.,* minimizing the negative timing impact

28   of dummy metal on clock nets while also reducing the opportunity for dishing and

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1 erosion that could result in inaccurate transfer of patterns during lithography,

2 suboptimal layouts/designs, inaccurate timing, reduced signal integrity, crosstalk

3 delay, noise issues, increased probability of failure, and ultimately defective or

4 underperforming devices. *See, e.g.*, Ex. A at 6:11–15.

5   27.   The claims of the '259 patent also recite inventive concepts that improve

6 the functioning of the fabrication process, particularly as to dummy filling. The

7 claims of the '259 patent disclose a new and novel solution to specific problems

8 related to improving semiconductor fabrication. As explained in detail above and in

9 the '259 patent specification, the claimed inventions improve upon the prior art

10 processes by prioritizing dummy regions such that the dummy regions located

11 adjacent to clock nets are filled with dummy metal last. This has the advantage of

12 reducing the impact of dummy metal on signal and clock lines and increasing the

13 efficiency, yield, and design/layout miniaturization and flexibility of the

14 manufacturing process. The claimed inventive processes also increase performance

15 and signal integrity, while reducing crosstalk delay, noise issues, probability of

16 failure, and defective and/or underperforming devices.

17 **COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,007,259**

18   28.   Bell Semic re-alleges and incorporates by reference the allegations of the

19 foregoing paragraphs as if fully set forth herein.

20   29.   The '259 patent is valid and enforceable under the United States Patent

21 Laws.

22   30.   Bell Semic owns, by assignment, all right, title, and interest in and to the

23 '259 patent, including the right to collect for past damages.

24   31.   A copy of the '259 patent is attached at Exhibit A.

25   32.   On information and belief, NXP has and continues to directly infringe

26 pursuant to 35 U.S.C. § 271(a) one or more claims of the '259 patent by using the

27 patented methodology to design one or more semiconductor devices, including as one

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COMPLAINT

1   example the NXP LS1043A Quad-Core Networking Processor chips, in the United

2   States.

3   33.   On information and belief, NXP employs a variety of design tools, for

4   example, Cadence, Synopsys, and/or Siemens tools, to insert dummy metal into a

5   circuit design (the "Accused Processes") as recited in the '259 patent claims. As one

6   example, NXP's Accused Processes perform a method for inserting dummy metal

7   into a circuit design, where the circuit design includes a plurality of objects and clock

8   nets as required by claim 1 of the '259 patent. NXP does so by employing a design

9   tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to insert

10   dummy metal into a circuit design for its NXP LS1043A Quad-Core Networking

11   Processor chips. The NXP LS1043A Quad-Core Networking Processor chips' design

12   include a plurality of objects, such as cells, interconnects, signal nets, and clock nets.

13   34.   NXP's Accused Processes also identify free spaces on each layer of the

14   circuit design suitable for dummy metal insertion as dummy regions. NXP does so by

15   employing a design tool, such as at least one of the Cadence, Synopsys, and/or

16   Siemens tools, to identify free spaces on each layer of its NXP USA, Inc. chips'

17   circuit designs suitable for dummy metal insertion as dummy regions.

18   35.   NXP's Accused Processes also prioritize the dummy regions such that

19   the dummy regions located adjacent to clock nets are filled with dummy metal last,

20   thereby minimizing any timing impact on the clock nets. NXP does so by employing

21   a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to

22   prioritize dummy regions such that those adjacent to clock nets are filled with

23   dummy metal last. For example, the Accused Processes assign a "high cost" to

24   adding metal fill near the clock nets and "lower cost" to adding metal fill near signal,

25   power, and ground nets. Assigning "cost" in this way fills dummy regions adjacent to

26   clock nets last and minimizes any timing impact on the clock nets. An exemplary

27   infringement analysis showing infringement of one or more claims of the '259 patent

28   is set forth in Exhibit B. The declaration of Lloyd Linder, an expert in the field of

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Los Angeles, CA

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1 semiconductor device design, is attached at Exhibit C and further describes NXP's

2 infringement of the '259 patent.

3   36.   NXP's Accused Processes infringe and continue to infringe one or more

4 claims of the '259 patent during the pendency of the '259 patent.

5   37.   On information and belief, NXP has and continues to infringe pursuant to

6 35 U.S.C. § 271, *et. seq.*, directly or indirectly, either literally or under the doctrine of

7 equivalents, by using the Accused Processes in violation of one or more claims of the

8 '259 patent. NXP has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*,

9 directly or indirectly, either literally or under the doctrine of equivalents, by making,

10 selling, or offering to sell in the United States, or importing into the United States

11 products manufactured or otherwise produced using the Accused Processes in

12 violation of one or more claims of the '259 patent.

13   38.   NXP's infringement of the '259 patent is willful and deliberate, entitling

14 Bell Semic to enhanced damages and attorneys' fees. NXP's infringement of the '259

15 patent was, and continues to be, done with knowledge of the '259 patent and with

16 knowledge of Bell Semic's contention that NXP is infringing the '259 patent. On

17 February 28, 2022, John Veschi of Bell Semic sent an email to Changhae Park of

18 NXP informing Mr. Park that Bell Semic is the owner of US Patent No. 7,007,259 to

19 Shrowty and that Bell Semic has evidence of infringement of the '259 in NXP's

20 semiconductor products, such as NXP's processors and power management ICs.

21 NXP's infringement of the '259 patent is thus willful and deliberate, entitling Bell

22 Semic to enhanced damages and attorneys' fees.

23   39.   NXP's infringement of the '259 patent is exceptional and entitles Bell

24 Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C.

25 § 285.

26   40.   Bell Semic has been damaged by NXP's infringement of the '259 patent

27 and will continue to be damaged unless NXP is enjoined by this Court. Bell Semic

28 has suffered and continues to suffer irreparable injury for which there is no adequate

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1   remedy at law. The balance of hardships favors Bell Semic, and public interest is not

2   disserved by an injunction.

3   41.   Bell Semic is entitled to recover from NXP all damages that Bell Semic

4   has sustained as a result of NXP's infringement of the '259 patent, including without

5   limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

7   WHEREFORE, Bell Semic respectfully requests that this Court enter judgment

8   in its favor as follows and award Bell Semic the following relief:

9   (a)   a judgment declaring that NXP has infringed one or more claims of the

10   '259 patent in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;

11   (b)   an award of damages adequate to compensate Bell Semic for

12   infringement of the '259 patent by NXP, in an amount to be proven at

13   trial, including supplemental post-verdict damages until such time as

14   NXP ceases its infringing conduct;

15   (c)   a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting NXP

16   and its officers, directors, employees, agents, consultants, contractors,

17   suppliers, distributors, all affiliated entities, and all others acting in

18   privity with NXP, from committing further acts of infringement;

19   (d)   a judgment requiring NXP to make an accounting of damages resulting

20   from NXP's infringement of the '259 patent;

21   (e)   enhanced damages for willful infringement;

22   (f)   the costs of this action, as well as attorneys' fees as provided by 35

23   U.S.C. § 285;

24   (g)   pre-judgment and post-judgment interest at the maximum amount

25   permitted by law;

26   (h)   all other relief, in law or equity, to which Bell Semic is entitled.

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McKool Smith Hennigan, P.C.
Los Angeles, CA

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DEMAND FOR JURY TRIAL

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Plaintiff hereby demands a jury trial for all issues so triable.

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Dated: April 27, 2022

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COMPLAINT

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LOS ANGELES, CA

EXHIBIT A

US007007259B2

(12) **United States Patent** (10) **Patent No.:** **US 7,007,259 B2**
Shrowty et al. (45) **Date of Patent:** **Feb. 28, 2006**

(54) **METHOD FOR PROVIDING CLOCK-NET AWARE DUMMY METAL USING DUMMY REGIONS**

(75) Inventors: **Vikram Shrowty**, Fremont, CA (US); **Santhanakrishnan Raman**, Fremont, CA (US)

(73) Assignee: **LSI Logic Corporation**, Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 260 days.

(21) Appl. No.: **10/632,622**

(22) Filed: **Jul. 31, 2003**

(65) **Prior Publication Data**

US 2005/0028121 A1 Feb. 3, 2005

(51) **Int. Cl.**
G06F 9/45 (2006.01)
G06F 17/50 (2006.01)
(52) **U.S. Cl.** **716/10**; 716/2; 716/6
(58) **Field of Classification Search** .... None
See application file for complete search history.

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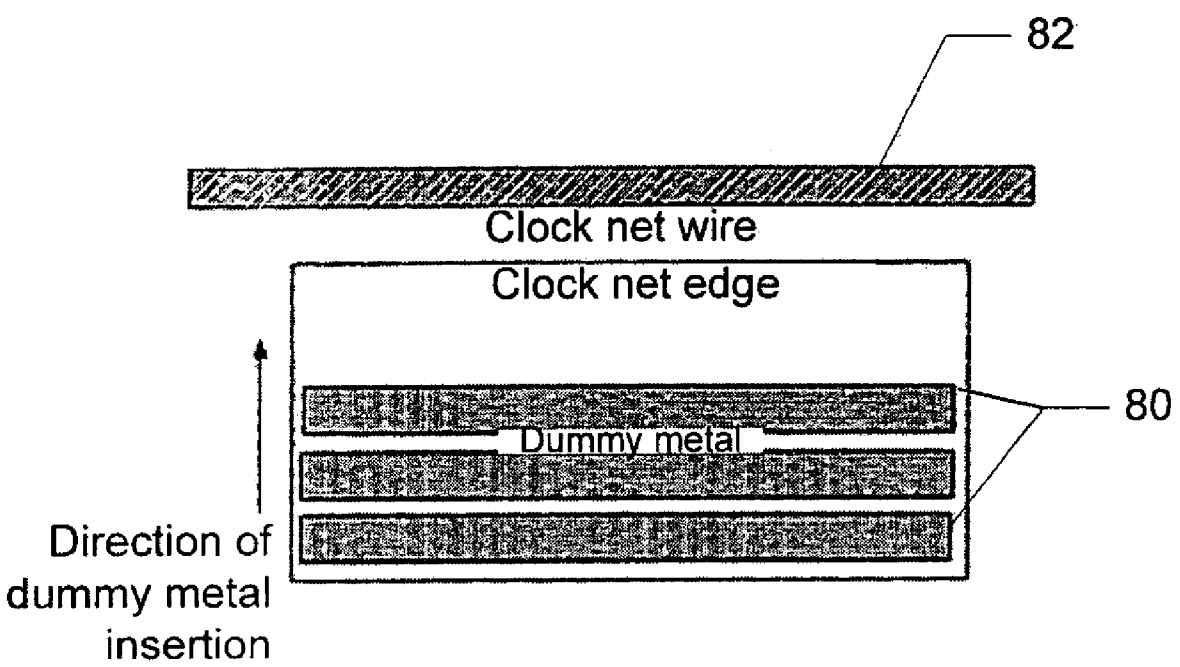|			
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Primary Examiner—Leigh M. Garbowski
(74) *Attorney, Agent, or Firm*—Sawyer Law Group LLP

(57) **ABSTRACT**

A method and system is disclosed for inserting dummy metal into a circuit design, which includes a plurality of objects and clock nets. Aspects of the invention include identifying free spaces on each layer of the chip design suitable for dummy metal insertion, wherein the free spaces are referred to as dummy regions. Thereafter, the dummy regions are prioritized such that the dummy regions located adjacent to clock nets are filled with dummy metal last. In a preferred embodiment, the dummy regions are further prioritized such that the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions that are located adjacent to narrower clock nets.
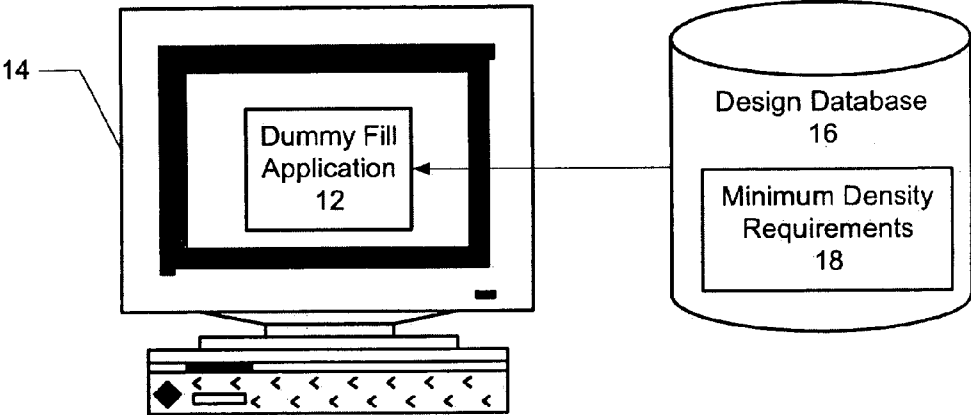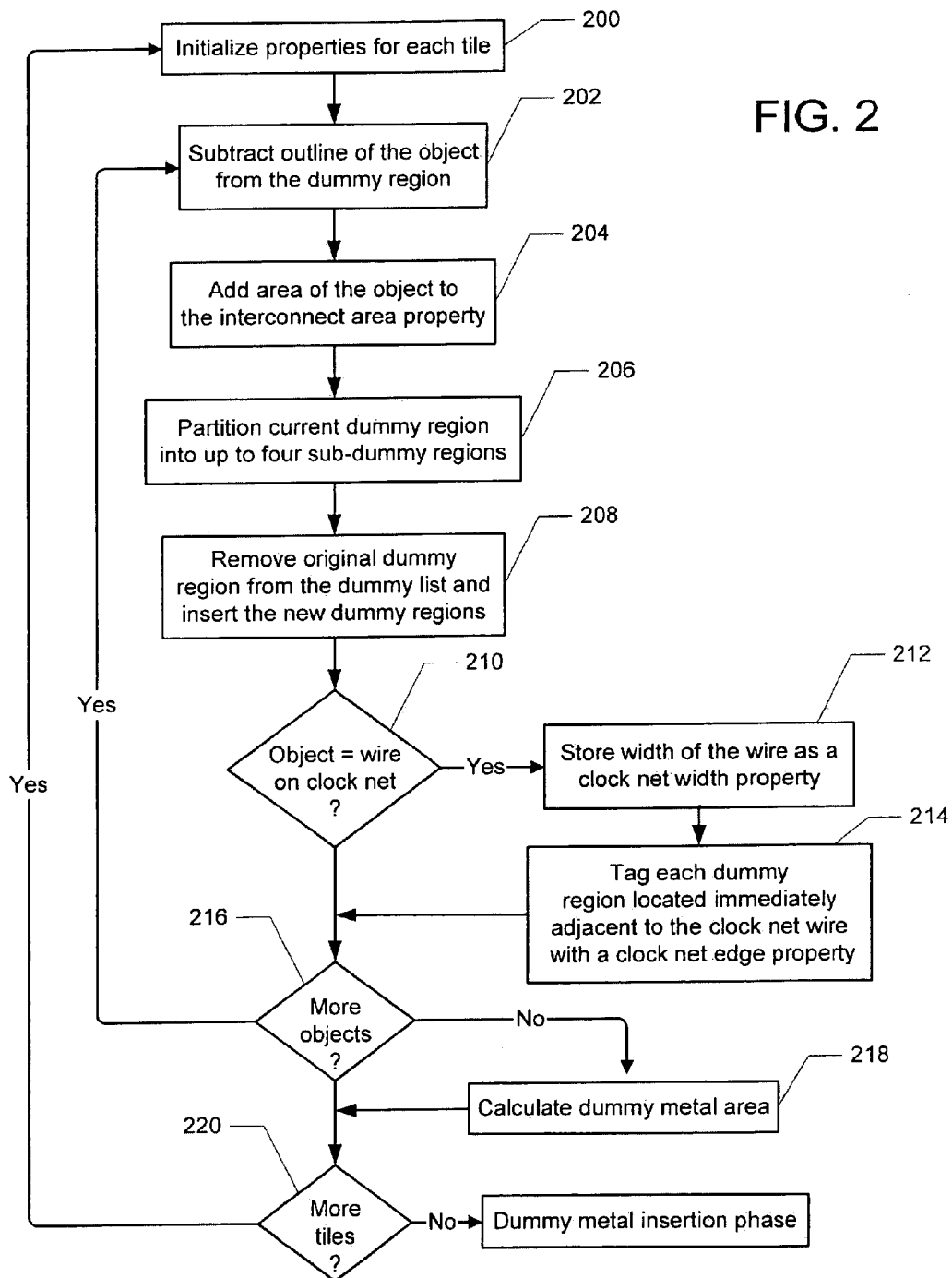
37 Claims, 5 Drawing Sheets

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Dummy Fill
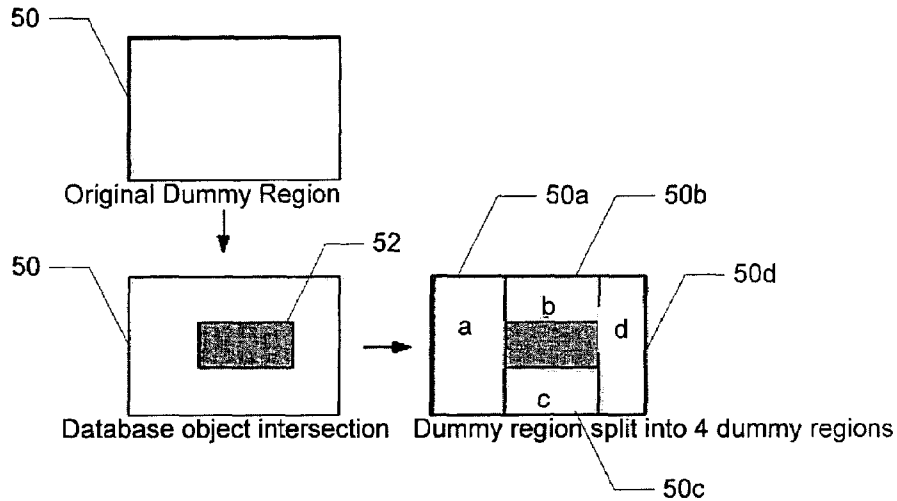Application
12

Design Database
16

Minimum Density
Requirements
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FIG. 1

FIG. 2

Initialize properties for each tile — 200

Subtract outline of the object from the dummy region — 202

Add area of the object to the interconnect area property — 204

Partition current dummy region into up to four sub-dummy regions — 206

Remove original dummy region from the dummy list and insert the new dummy regions — 208

Object = wire on clock net ? — 210

Yes

Store width of the wire as a clock net width property — 212

Tag each dummy region located immediately adjacent to the clock net wire with a clock net edge property — 214

More objects ? — 216

Yes

No

Calculate dummy metal area — 218

More tiles ? — 220

Yes

No

Dummy metal insertion phase

FIG. 3

Tile Properties

Dummy List 60			
Dummy Region	Clock Net Width	Clock Net Edge	Timing Factor
Dummy Region			Timing Factor
Dummy Region	Clock Net Width	Clock Net Edge	Timing Factor
Dummy Region			Timing Factor
Dummy Region	Clock Net Width	Clock Net Edge	Timing Factor
Dummy Region	Clock Net Width	Clock Net Edge	Timing Factor

Tile Area	Interconnect Area	Dummy Metal Area
62	64	66

FIG. 4

250

Calculate timing factor
for the dummy regions

252

Sort the dummy region list for the tile
in ascending order of the timing factor

254

Insert dummy metal into
the sorted dummy regions

256

Add the inserted area to the
interconnect area property of the tile

258

Recalculate the dummy
metal area for the tile

260

Dummy Metal
Positive
?

No

262

More
Tiles
?

Yes

No

End

FIG. 5

82

Clock net wire

Clock net edge

80

Dummy metal

Direction of
dummy metal
insertion

FIG. 6

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METHOD FOR PROVIDING CLOCK-NET AWARE DUMMY METAL USING DUMMY REGIONS

FIELD OF THE INVENTION

The present invention relates to methods for patterning dummy metal to achieve planarity for chemical-mechanical polishing of integrated circuits, and more particularly to a dummy fill software tool that provides clock-net aware dummy metal using dummy regions.

BACKGROUND OF THE INVENTION

Chemical Mechanical Polishing (CMP) is a part of the chip fabrication process that requires a uniform distribution of metal and silicon over the surface of the chip. To achieve this distribution, pieces of interconnect (metal or silicon) must be inserted into available spaces in low-density regions of the chip. This interconnect insertion is called dummy metal filling or simply dummy filling, and the inserted interconnect is called dummy metal.

Most fabrication processes require a minimum density for the interconnects on each layer of a multi-layer chip design. The interconnect density for a region is the sum total of the area of all interconnect in that region divided by the area of the region. Fabrication processes typically partition each layer of the design into rectangular regions, called tiles, and specify that the interconnect density of each tile meet a minimum density requirement.

The process of determining the number and placement of dummy metal is typically preformed by a dummy fill software tool after routing and timing closure during chip design flow. The dummy fill tool examines the tiles in each layer of the design and determines whether each tile has an interconnect density equal to or greater than the specified minimum density. If the interconnect density does not meet the minimum density, then the dummy fill tool inserts dummy metal in free regions of the tile.

Because dummy filling is one of the last steps in the chip design flow, it is important that the dummy metal is inserted into the chip in such a manner that minimizes any negative impact to timing. That is, patterning the dummy metal too close to signal nets increases capacitance between the dummy lines and the signal wires. The increased capacitance can affect the signal nets by slowing the transmission speed of signals, thereby degrading overall performance of the integrated circuit.

Therefore, a common goal of dummy filling techniques is the minimization of the parasitic capacitance introduced by the dummy metal. The parasitic capacitance introduced by a piece of dummy metal on a signal wire is inversely proportional to the distance between the two. This means that to minimize timing impact, dummy metal must be placed far away from signal nets.

Of signal nets, clock nets are of particular importance. Care must be taken to minimize the negative timing impact to clock nets. Traditionally, this has been achieved with a simplistic approach. The dummy fill tool is programmed to maintain a larger distance between wires of clock nets and the inserted dummy metal. This large dummy to clock distance is arrived at by studying the effect on timing that the inserted dummy metal has at various distances from clock nets in sample designs, and then hardcoding the distances into the dummy fill libraries for each type of process technology.

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However, hardcoding a large "stay-away" distance between dummy metal and clock nets may lead to less available space in each tile for dummy metal insertion. New process technologies increasingly demand higher minimum density values and more timing-aggresive designs. In this scenario, use of the simple large dummy-to-clock distance methodology is disadvantageous. This is because it is often impossible to insert enough dummy metal into a tile to meet the required minimum density without reducing the large dummy-to-clock distance. In this case, traditional metal-fill tools complete their run without reaching minimum density in some tiles, requiring a second run of the tool for the problematic tiles in which the dummy-to-clock distance is reduced. If there is more than one such tile requiring a rerun, and the dummy fill tool can handle only one tile at a time, multiple runs may be needed: one for each tile. Such an involved, iterative process can significantly impact the design schedule.

Accordingly what is needed is an algorithm for dummy fill that minimizes the negative timing impact of dummy metal on clock nets, while at the same time achieving minimum density in a single run. The present invention addresses such a need.

SUMMARY OF THE INVENTION

The present invention provides a method for inserting dummy metal into a circuit design, which includes a plurality of objects and clock nets. Aspects of the invention include identifying free spaces on each layer of the chip design suitable for dummy metal insertion, wherein the free spaces are referred to as dummy regions. Thereafter, the dummy regions are prioritized such that the dummy regions located adjacent to clock nets are filled with dummy metal last. In a preferred embodiment, the dummy regions are further prioritized such that the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions that are located adjacent to narrower clock nets.

According to the method and system disclosed herein, inserting dummy metal into dummy regions that are not adjacent to clock nets prior to inserting dummy metal into clock-net adjacent dummy regions will be sufficient to meet the minimum density requirement. This means that in many cases, no dummy metal (or a minimal amount) is inserted in the clock-net adjacent dummy regions, thereby minimizing the timing impact to the adjacent clock nets.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram illustrating a software and hardware environment in which the present invention may be implemented.

FIG. **2** is a flow diagram illustrating the process performed by the dummy fill application for inserting dummy metal into the chip design during a free space finding phase.

FIG. **3** is a diagram showing the handling of the dummy regions in a tile after all objects in the database have been iterated over.

FIG. **4** is a diagram illustrating the properties stored for each tile.

FIG. **5** is a flow diagram illustrating the process performed by the dummy fill application during a dummy metal insertion phase.

FIG. **6** is a diagram illustrating metal insertion in clock-net adjacent dummy regions according to preferred embodiment of the present invention.

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DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to design methodologies for dummy metal filling. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiments and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

The present invention provides a software tool for dummy metal filling of a chip design during the design phase. FIG. 1 is a block diagram illustrating a software and hardware environment in which the present invention may be implemented. The dummy fill software application 12 is preferably executed on a computer 14, which may be a workstation or a server. The dummy fill application 12 accesses a design database 16, which includes information describing all objects of a fully routed integrated circuit design, such as cells, interconnects, and signal nets. In a preferred environment, each layer of the chip is partitioned into tiles, each equal in size to a process-specified tile-size. The design database 16 also includes the minimum density requirement for the tiles. The dummy fill application 12 is one of many design flow tools, and is primarily invoked after routing and timing closure stages of a design flow.

According to the present invention, the dummy fill application 12 inserts dummy metal into the chip design in a manner that minimizes the timing impact to clock nets, while the same time achieving the minimum density requirement in a single run. The dummy fill application 12 operates in two phases. In the first phase, referred to as the free-space finding phase, the dummy fill application 12 searches each layer of the chip design for empty spaces suitable for dummy metal insertion. These empty spaces are referred to herein as dummy regions.

In the second phase, referred to as the dummy metal insertion phase, the dummy fill application 12 inserts a sufficient amount of dummy metal into the dummy regions discovered in the first phase to meet the minimum density requirement of each tile, but prior to doing so, prioritizes the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last. And, as further described below, the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions adjacent to narrower clock nets.

By prioritizing the empty spaces in this manner, the minimum density requirements of the chip can be met, while minimizing negative impact to the clock nets because the distance between the dummy metal and clock nets, especially the thicker, more important clock nets, is maximized.

FIG. 2 is a flow diagram illustrating the process for inserting dummy metal into the chip design performed by the dummy fill application 12 during the free space finding phase. The free space finding phase begins in step 200 by initializing a series of properties for each tile, including a dummy region list, interconnect area, and dummy metal area. The dummy regions are a list of free areas in the tile suitable for dummy metal. In a preferred embodiment, the dummy region list for each tile is initialized with a single rectangle corresponding to the outline of the tile. The interconnect area property will be used to specify the total amount of interconnect area included in the tile, and the

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dummy metal area property will be used to specify the total amount of dummy metal inserted into the tile.

In step 202, the dummy fill application 12 traverses the design database 16 and for each object found in the current tile, subtracts the outline of the object from the dummy region on which it lies.

FIG. 3 is a diagram showing the processing of a dummy region 50 once an object 52 is found intersecting the dummy region 50. Referring to both FIGS. 2 and 3, the area of the object 52 is added to the interconnect area property for the tile in step 204. In step 206, the current dummy region is partitioned into up to four sub-dummy regions 50a–50d around the subtracted area. In a preferred embodiment, each sub-dummy region 50a–50d is formed between one of the edges of the object 52 and the corresponding edge of the current dummy region 50. Therefore, if the object 52 is located along one edge of the original dummy region 50, then only three sub-dummy regions 50a–50c will be created. In step 208, the original dummy region 50 is removed from the dummy list and the new dummy regions 54 are inserted into the list. The result of this process is a list of dummy regions 50 that represent free spaces in the tile suitable for dummy metal.

According to the present invention, objects in the design database 16 representing wires on clock nets are treated specially. If it is determined in step 210 that the current object is a wire on a clock net, then in step 212, the width of the wire is stored as a clock net width property of the region 50 created by its outline. Also, the sub-dummy regions 50a–50c located immediately adjacent to the clock net wire are tagged with a clock net edge property as well as the clock net width property in step 214 so as to be identifiable later. The sub-dummy regions 50a–50c replace their parent (50) on the dummy list.

In step 216, it is determined if the current tile includes additional objects, and if so, the database traversal continues.

FIG. 4 is a diagram illustrating the properties stored for each tile after all the objects have been found. The properties include the dummy region list 60, the tile area 62, the interconnect area 64, and the dummy metal area 66. Also maintained for each clock net region is a timing factor 72, which is calculated during the second phase. In addition, several properties may also be maintained for each of the dummy regions 50 in the dummy region list 60 including a clock net edge 70 property, which identifies the region as being adjacent to a clock net, and a clock net width 68 property, which identifies the width of the adjacent clock net wire.

Referring again to FIG. 2, according to one aspect of the present invention, the dummy metal area 66 that needs to be inserted to meet minimum density is calculated in step 218 for the current tile is as follows:

$$\text{Dummy Metal Area}=(\text{Minimum Density}*\text{Tile Area})-\text{Interconnect Area}$$

In step 220, it is determined whether there are more tiles to process. If there are more tiles, the process continues. Otherwise, the free space finding phase is complete and the dummy fill application 12 executes the dummy metal insertion phase.

FIG. 5 is a flow diagram illustrating the process performed by the dummy fill application 12 during the dummy metal insertion phase. The dummy metal insertion phase begins in step 250 in which the timing factor 72 is calculated for each dummy region 50 in the list 60 that has a clock net width 68 property. The timing factor 72 attempts to capture

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the timing criticality of a dummy region **50**. In a clock tree, the width of a wire is indicative of its order in a hierarchy. A wide wire is likely to be supplying current to more branches than a thinner wire, and is therefore more timing critical.

In a preferred embodiment, the timing factor **72** is calculated using the formula:

$$\text{Timing Factor}=\text{Clock Net Width}*\text{Clock Net Criticality}$$

According to one aspect of the present invention, the clock net criticality is an integral value that the user can specify to control the timing factor **72** assigned to the dummy regions. In a preferred embodiment, the criticality factor is assigned to the entire clock net and is inherited by all wires on that clock net. Also in a preferred embodiment, the clock net criticality values are stored in the form of lookup table in file and provides the user control over relative treatment of clock nets. More critical clock nets can be given higher values. In the absence of a user-specified value, the clock net criticality for a clock net is assigned some default value, e.g., '1'.

The table below illustrates an example Clock Net Criticality Lookup table:	
Clock Nets	Clock Net Criticality
Clock_Net_A	2
Clock_Net_B	3

In a preferred embodiment, all dummy regions **50** not adjacent to a clock-net wire are assigned a Timing Factor of 0.

Referring again to FIG. **5**, after the timing factors **72** have been calculated in step **252**, the dummy region list **60** for each tile is sorted in ascending order of the timing factor **72**. According to the present invention, this establishes a prioritization for the dummy regions **50** in which dummy regions **50** adjacent to clock nets are placed on the list **60** after dummy regions **50** that are not adjacent to clock nets. Within the sub-list of clock-net adjacent dummy regions **50**, the dummy regions **50** adjacent to wider wires of a clock net are listed after the dummy regions **50** adjacent to narrower wires of the same clock net. Between two dummy regions **50** adjacent to clock net wires of the same width, the dummy region **50** that is adjacent to a net having a higher criticality value is listed after the other.

After the sorting, the dummy that application **12** in step **254**, begins inserting dummy metal into the sorted dummy regions **50**, starting with the first dummy region **50** on the list. After each insertion, the inserted area is added to the interconnect area **64** property of the tile in step **256**, and the dummy metal area **66** for the tile is recalculated in step **258**.

This process is continued in step **260** until the dummy metal area **66** becomes negative. Thereafter, the process continues with the next tile in step **262** until all tiles are processed.

In most cases, the value for the dummy metal area **66** will become negative before traversal of the dummy region list **60** reaches the clock-net adjacent dummy regions **50**. This means that in many cases, no dummy metal (or a minimal amount) is inserted in the clock-net adjacent dummy regions **50**, thereby minimizing the timing impact to the adjacent clock nets.

If metal insertion is required in any of the clock-net adjacent dummy regions **50**, then the metal insertion may be

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performed starting with the edge opposite the clock-net adjacent edge, using the clock net edge **70** property. FIG. **6** is a diagram showing the insertion of dummy metal in a clock-net adjacent dummy region, starting with the edge opposite to the one identified by the clock net edge **70** property. According to this aspect of the present invention, if the value for the dummy metal area **66** becomes negative before the clock-net adjacent dummy region **50** is completely filled, the spacing between the dummy metal **80** and the clock net wire **82** is the maximum possible.

A dummy fill application **12** has been described that provides a simple and efficient method for dummy metal insertion that minimizes the timing impact to clock nets and at the same time guarantees reaching minimum density in a single pass.

The present invention has been described in accordance with the embodiments shown, and one of ordinary skill in the art will readily recognize that there could be variations to the embodiments, and any variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

We claim:

1. A method for inserting dummy metal into a circuit design, the circuit design including a plurality of objects and clock nets, the method comprising:
   (a) identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions; and
   (b) prioritizing the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets.

2. The method of claim **1** wherein step (b) further includes the step of: prioritizing the dummy regions such that the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions that are located adjacent to narrower clock nets.

3. The method of claim **2** further including the step of: allowing a user to specify a clock net criticality value for the clock nets.

4. The method of claim **3** wherein step (b) further includes the step of: in an absence of a user-specified clock net criticality value for any of the clock nets, assigning a default value.

5. The method of claim **4** wherein step (b) further includes the step of: prioritizing the dummy regions such that between two dummy regions located adjacent to clock net wires of the same width, the dummy region that is adjacent to a clock net having a higher criticality value is filled with dummy metal after the other dummy region.

6. The method of claim **5** wherein step (b) further includes the step of: calculating a timing factor for each dummy region located adjacent to a clock net by multiplying a width of the clock net wire by the clock net criticality value.

7. The method of claim **6** wherein step (b) further includes the step of: assigning a timing factor value of 0 to all dummy regions not adjacent to a clock-net wire.

8. The method of claim **7** further including the step of: maintaining a dummy region list for each tile in the design.

9. The method of claim **8** wherein step (b) further includes the step of: sorting the timing factors assigned to each of the dummy regions in the list in order to prioritize the dummy regions in the tile.

10. The method of claim **9** wherein step (b) further includes the step of: inserting dummy metal into the dummy

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<table>
<tr><td>7</td><td>8</td></tr>
</table>

regions starting with the first dummy region on the list until a minimum density requirement for the tile is met.

11. The method of claim **10** wherein step (b) further includes the step of: after each dummy metal insertion, adding the area of the inserted dummy metal to an interconnect area property of the tile.

12. The method of claim **11** wherein step (b) further includes the step of: calculating a dummy metal area that needs to be inserted in the tile to meet a minimum density requirement as:

Dummy Metal Area=(Minimum Density*Tile Area) −Interconnect Area.

13. The method of claim **1** wherein step (a) further includes the step of: initializing a dummy region list for each tile as a single rectangle corresponding to the outline of the tile.

14. The method of claim **13** wherein step (a) further includes the step of: traversing a design database and for each object found in the current tile, subtracting an outline of the object from the dummy region on which it lies.

15. The method of claim **14** wherein step (a) further includes the step of: once an object is found intersecting a particular dummy region,

(i) adding an area of the object to an interconnect area property for the tile,

(ii) partitioning the dummy region into sub-dummy regions,

(iii) removing the dummy region from the dummy region list, and

(iv) adding the sub-dummy regions to the dummy region list.

16. The method of claim **15** wherein step (a) further includes the step of: if a particular object is a wire on a clock net, storing a width of the wire as a clock net width property of the dummy region created by an outline of the object, and tagging an edge of each dummy region located immediately adjacent to the clock net wire with a clock net edge property.

17. The method of claim **16** wherein step (b) further includes the step of: calculating a timing factor for each dummy region in the list that has a clock net width property, and sorting the dummy regions based on the timing factors.

18. A computer-readable medium containing program instructions for inserting dummy metal into a circuit design, the circuit design including a plurality of objects and clock nets, the program instructions for:

(a) identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions; and

(b) prioritizing the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets.

19. The computer-readable medium of claim **18** wherein instruction (b) further includes the instruction of: prioritizing the dummy regions such that the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions that are located adjacent to narrower clock nets.

20. The computer-readable medium of claim **19** further including the instruction of: allowing a user to specify a clock net criticality value for the clock nets.

21. The computer-readable medium of claim **20** wherein instruction (b) further includes the instruction of: in an absence of a user-specified clock net criticality value for any of the clock nets, assigning a default value.

22. The computer-readable medium of claim **21** wherein instruction (b) further includes the instruction of: prioritizing the dummy regions such that between two dummy regions located adjacent to clock net wires of the same width, the dummy region that is adjacent to a clock net having a higher criticality value is filled with dummy metal after the other dummy region.

23. The computer-readable medium of claim **22** wherein instruction (b) further includes the instruction of: calculating a timing factor for each dummy region located adjacent to a clock net by multiplying a width of the clock net wire by the clock net criticality value.

24. The computer-readable medium of claim **23** wherein instruction (b) further includes the instruction of: assigning a timing factor value of 0 to all dummy regions not adjacent to a clock-net wire.

25. The computer-readable medium of claim **24** further including the instruction of: maintaining a dummy region list for each tile in the design.

26. The computer-readable medium of claim **25** wherein instruction (b) further includes the instruction of: sorting the timing factors assigned to each of the dummy regions in the list in order to prioritize the dummy regions in the tile.

27. The computer-readable medium of claim **26** wherein instruction (b) further includes the instruction of: inserting dummy metal into the dummy regions starting with the first dummy region on the list until a minimum density requirement for the tile is met.

28. The computer-readable medium of claim **27** wherein instruction (b) further includes the instruction of: after each dummy metal insertion, adding an area of the inserted dummy metal to an interconnect area property of the tile.

29. The computer-readable medium of claim **28** wherein instruction (b) further includes the instruction of: calculating a dummy metal area that needs to be inserted in the tile to meet a minimum density requirement as:

Dummy Metal Area=(Minimum Density*Tile Area) −Interconnect Area.

30. The computer-readable medium of claim **18** wherein instruction (a) further includes the instruction of: initializing a dummy region list for each tile as a single rectangle corresponding to the outline of the tile.

31. The computer-readable medium of claim **30** wherein instruction (a) further includes the instruction of: traversing a design database and for each object found in the current tile, subtracting an outline of the object from the dummy region on which it lies.

32. The computer-readable medium of claim **31** wherein instruction (a) further includes the instruction of: once an object is found intersecting a particular dummy region,

(i) adding an area of the object to an interconnect area property for the tile,

(ii) partitioning the dummy region into sub-dummy regions,

(iii) removing the dummy region from the dummy region list, and

(iv) adding the sub-dummy regions to the dummy region list.

33. The computer-readable medium of claim **32** wherein instruction (a) further includes the instruction of: if a particular object is a wire on a clock net, storing an width of the wire as a clock net width property of the dummy region created by an outline of the object, and tagging an edge of each dummy region located immediately adjacent to the clock net wire with a clock net edge property.

34. The computer-readable medium of claim **33** wherein instruction (b) further includes the instruction of: calculating

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a timing factor for each dummy region in the list that has a clock net width property, and sorting the dummy regions based on the timing factors.

35. A method for inserting dummy metal into a circuit design, the circuit design including a plurality of objects and clock nets, the method comprising:

(a) identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions;

(b) determining which of the dummy regions are located adjacent to clock nets;

(c) assigning a timing factor to each dummy region based on an width of an adjacent clock net wire;

(d) sorting the dummy regions based on the timing factors; and

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(e) inserting dummy metal into the sorted dummy regions such that the dummy regions located adjacent to increasingly wider clock nets are filled last, thereby minimizing any timing impact on the clock nets.

36. The method at claim 35 wherein step (c) further includes the steps of: assigning the timing factor based on the width of the adjacent clock net wire and a user-specified timing criticality value assigned to the clock net.

37. The method of claim 36 wherein step (e) further include the step of: inserting dummy metal into the sorted dummy regions one by one until a minimum density requirement for a current tile is met.

*   *   *   *   *

EXHIBIT B

BELL SEMICONDUCTOR LLC'S ANALYSIS OF INFRINGEMENT

U.S. Patent No. 7,007,259 – NXP

Exemplary Claim 1

Bell Semiconductor ("Bell Semic") provides evidence of infringement of exemplary claim 1 of U.S. Patent No. 7,007,259 ("the '259 patent") in the following claim chart.

"Accused Products" as used herein refers to the NXP circuit designs and/or semiconductor products, including at least the NXP LS1043A Quad-Core Networking Processor, that are made, produced, and/or processed by a design tool, such as a Cadence Design Systems, Inc.("Cadence"), Synopsys, Inc. ("Synopsys"), and/or Siemens Digital Industries Software (formerly Mentor Graphics) ("Siemens") tool,[1] by inserting dummy metal into a circuit design where dummy regions are prioritized such that the dummy regions located adjacent to clock nets are filled with dummy metal last. On information and belief, these design tools all function similarly with respect to the functionality described herein. For simplicity, the Cadence tool will be the primary tool cited herein to illustrate infringement of the claimed methods. These claim charts demonstrate infringement by comparing each element of the asserted claims to corresponding components, aspects, and/or features of the Accused Products. These claim charts are not intended to constitute an expert report on infringement. These claim charts include information provided by way of example, and not by way of limitation.

The analysis set forth below is based only upon information from publicly available resources regarding the Accused Products, as NXP and relevant third parties have not yet provided any non-public information. An analysis of non-public technical documentation may assist in further identifying all infringing features and functionality. Accordingly, Bell Semic reserves the right to supplement this infringement analysis once such information is made available to Bell Semic. Furthermore, Bell Semic reserves the right to revise this infringement analysis, as appropriate, upon issuance of a court order construing any terms recited in the asserted claims or as other circumstances so merit.
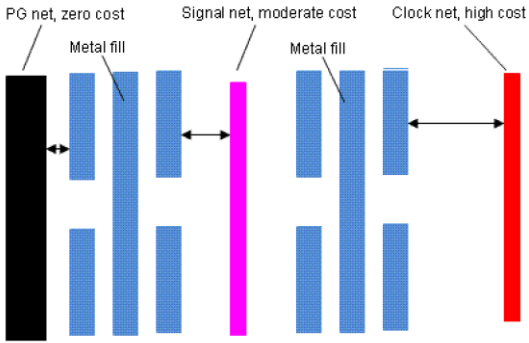
Bell Semic contends that each element of each claim asserted herein is literally met, and would also be met under the doctrine of equivalents, as there are no substantial differences between the Accused Products and the elements of the patent claims in function, way, and result. If NXP attempts to argue that there is no literal infringement and/or if NXP attempts to draw any distinction between the claimed functionality and the Accused Products, then Bell Semic reserves the right to rebut the alleged distinction as a matter of literal infringement and/or as to whether any such distinction is substantial under the doctrine of equivalents.

Unless otherwise noted, the cited evidence applies across each of NXP's products that were made, produced, or processed from a circuit design using clock aware dummy fill, including but not limited to the NXP LS1043A Quad-Core Networking Processor. Bell Semic reserves the right to amend this infringement analysis based on other products made, produced, or processed in the same or similar manner to that identified herein.

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[1]   NXP is a customer of at least Cadence and Siemens, as demonstrated here: https://www.cadence.com/en_US/home/multimedia.html/content/dam/cadence-www/global/en_US/videos/solutions/lars_reger_nxp_role_of_semiconductor_industry_in_automotive_innovation_1080p1; https://news.synopsys.com/2017-10-18-Synopsys-and-NXP-Extend-Multiyear-Automotive-Center-of-Excellence-Collaboration-for-NXP-S32-Automotive-Processing-Platform.

CLAIM CHARTS
CADENCE CUSTOMER NXP
U.S. Patent No. 7,007,259

Claim 1	Infringing Instrumentalities
1. A method for inserting dummy metal into a circuit design, the circuit design including a plurality of objects and clock nets, the method comprising:	To the extent the preamble is limiting, the Infringing Instrumentalities are produced by performing a method for inserting dummy metal into a circuit design, the circuit design including a plurality of objects and clock nets. The Accused Products are made, produced, and/or processed by design tools from at least one of Cadence, Synopsys, and Siemens to insert dummy metal into a circuit design, where the circuit design includes a plurality of objects and clock nets. **Timing-Aware Metal Fill** When it adds a timing-aware metal fill, the Innovus software avoids adding the fill near clock and signal nets and adds more near the power and ground nets. The software assigns a high cost to adding a metal fill near clock nets, a moderate cost to adding it near signal nets, and zero cost to adding it near power and ground nets. It adds the fill, based on the cost, to achieve the preferred metal density with the least effect on timing. The software adds timing-aware metal fill by default. *See Innovus User Guide product version 20.10, March 2020, page 709.*

CLAIM CHARTS
CADENCE CUSTOMER NXP
U.S. Patent No. 7,007,259

	## Integration While regular planarization is critical, metal fill can also negatively affect timing due to increased coupling capacitance in the nearby nets. So, it is paramount for the designer to consider the metal fill without impacting timing-critical nets. In order to overcome this shortcoming, the fill needs to be timing-aware, which is also needed when an engineering change order (ECO) arrives late in the design cycle—the ECOs make it indispensable for the designer to change the layout and fill around the affected area. Thus, it is imperative that the fill method should allow easy removal of and re-insertion without violating timings of the nearby nets. *See https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf , page 2.*

CLAIM CHARTS
CADENCE CUSTOMER NXP
U.S. Patent No. 7,007,259

Figure 4. Metal Fill steps in timing closure flow

CLAIM CHARTS
CADENCE CUSTOMER NXP
U.S. Patent No. 7,007,259

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The solution to this is to allow the ECO steps to ignore the existing dummy metal fill geometries allowing them to cause shorts and/or DRC violations, then repair those violations. Also, where original signal geometries were removed due to deletions in the ECO process, dummy metal fill can be added to get those areas back to

the desired metal density. This improves the ECO flow in two ways:

a.) Timing characteristics in areas that were not affected by the ECO are unchanged during the repair process.

b.) The overall time to complete the ECO including handling of the metal fill effects is reduced, both because the steps themselves are faster and the reduction in iterations from improvement in a).

See X.Dong; et. al., <u>New Metal Fill Considerations For Nanometer Technologies</u>, ASICON 2005 (6th International Conf.), page 807.

Xiaopeng Dong, Inhwan Seo and William Kao

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Cadence Design Systems Inc., 555 River Oaks Parkway, San Jose, CA 95134

These same steps are carried out by Synopsys and Siemens :
1. *See IC Compiler II Implementation User Guide , Version Q-2019.12-SP4, June 2020, page 544.*
2. *See <u>https://www.synopsys.com/content/dam/synopsys/implementation&signoff/white-papers/icv_signoff_metalfill_wp.pdf</u> , page 3.*
3. *See <u>https://www.synopsys.com/content/dam/synopsys/implementation&signoff/white-papers/icv_signoff_metalfill_wp.pdf</u> , page 4.*
4. *See <u>http://soiconsortium.eu/wp-content/uploads/2018/10/2017_0616_GF-Fill-Flows-with-Calibre-DAC2017_v1.4-FINAL.pdf</u> , page 11-13.*
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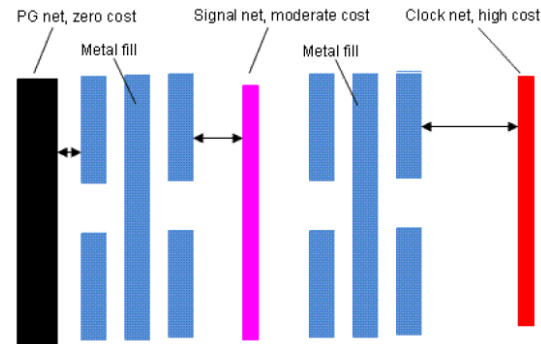|	
	For example, NXP creates a circuit design for the NXP LS1043A Quad-Core Networking Processor , which was made, produced, or processed from that circuit design created using one of the above-identified and described design tools to insert dummy metal into a circuit design, where the circuit design includes a plurality of objects and clock nets. As shown below, the NXP LS1043A Quad-Core Networking Processor includes a plurality of objects, dummy metal identified by the blue arrow, and a clock net identified by the green arrow.
(a) identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions; and	The Accused Products are made, produced, or processed from a circuit design that identifies free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions. The software uses parameters specified in the LEF file or the fill commands to analyze the density and determine the size and position of the fill. It divides the design into windows and adds metal or cuts to the open areas in each window until the metal and cut densities meet the density requirements. *See Innovus User Guide product version 20.10, March 2020, page 705.*
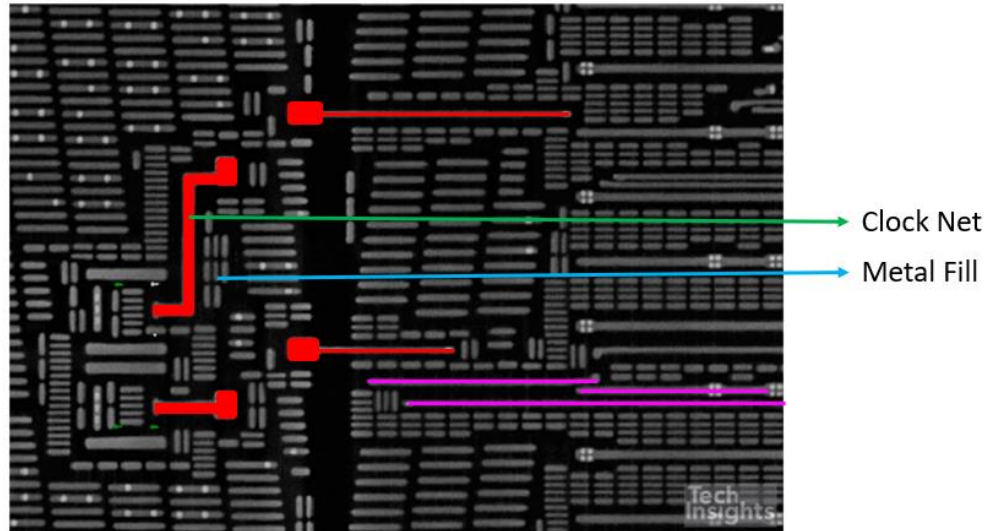
CLAIM CHARTS
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Timing-Aware Metal Fill

When it adds a timing-aware metal fill, the Innovus software avoids adding the fill near clock and signal nets and adds more near the power and ground nets.

The software assigns a high cost to adding a metal fill near clock nets, a moderate cost to adding it near signal nets, and zero cost to adding it near power and ground nets. It adds the fill, based on the cost, to achieve the preferred metal density with the least effect on timing.

PG net, zero cost   Signal net, moderate cost   Clock net, high cost

Metal fill   Metal fill

The software adds timing-aware metal fill by default.

See Innovus User Guide product version 20.10, March 2020, page 709.

Pegasus Verification's Incremental Metal Fill/Incremental Quantus Extraction's RC Extraction

When the initial signoff metal fill generation, RC extraction, timing analysis, and ECO are performed, some wiring patterns disappear, while some new patterns are generated. The newly added wiring pattern will cause a DRC violation between the initial metal fill and may be required to be removed. So, it is also essential to add metal fill to the empty spaces of the disappearing patterns of wires.

See https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf , page 4.

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	In this approach we assign different costs to different set of nets according to timing criticality. Fills not close to any nets or close to regular nets have the lowest cost. Next fills with proximity to power/ground nets will have higher costs. Finally fills close to clock nets or critical nets will have the highest costs. Based on this cost system we can minimize the parasitic impact from metal fill for both same layer and interlayer. In addition a tight integration with a	

timing engine is built in to use the critical nets information combined with the timing aware to feed the critical nets information into timing aware metal fill. Figure 1 shows a simple layout to illustrate the cost based timing aware metal fill. In this figure the fill candidate that is closest to clock net CLK has been assigned the highest cost of three. The fill candidate close to a power net VDD has been assigned a relative lower cost of two and the fill candidate that is far away from both power and clock nets has been assigned the lowest cost of one. The fill with lowest cost of one will be picked first and then the fill candidate with cost of two and lastly the one with cost of three which will be avoided if minimum density is met.
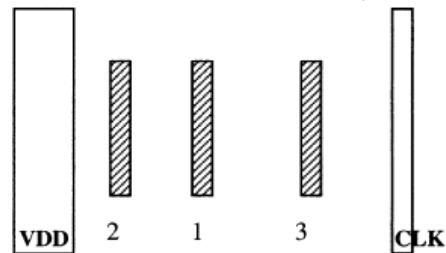

Figure 1. Cost based timing aware metal fill

See X.Dong; et. al., New Metal Fill Considerations For Nanometer Technologies, ASICON 2005 (6th International Conf.), page 805.

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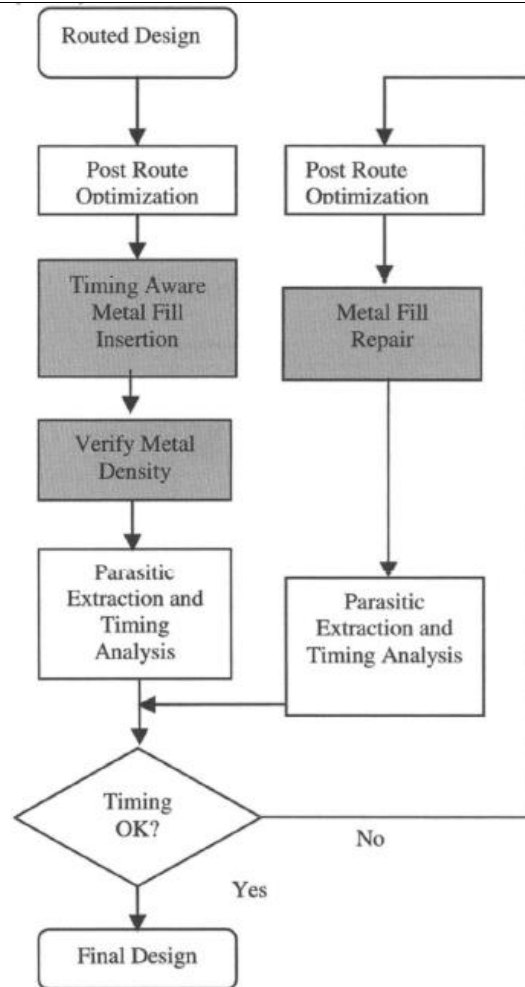U.S. Patent No. 7,007,259

Figure 4. Metal Fill steps in timing closure flow

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<table>
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The solution to this is to allow the ECO steps to ignore the existing dummy metal fill geometries allowing them to cause shorts and/or DRC violations, then repair those violations. Also, where original signal geometries were removed due to deletions in the ECO process, dummy metal fill can be added to get those areas back to

the desired metal density. This improves the ECO flow in two ways:

a.) Timing characteristics in areas that were not affected by the ECO are unchanged during the repair process.

b.) The overall time to complete the ECO including handling of the metal fill effects is reduced, both because the steps themselves are faster and the reduction in iterations from improvement in a).

See X.Dong; et. al., New Metal Fill Considerations For Nanometer Technologies, ASICON 2005 (6th International Conf.), page 807.

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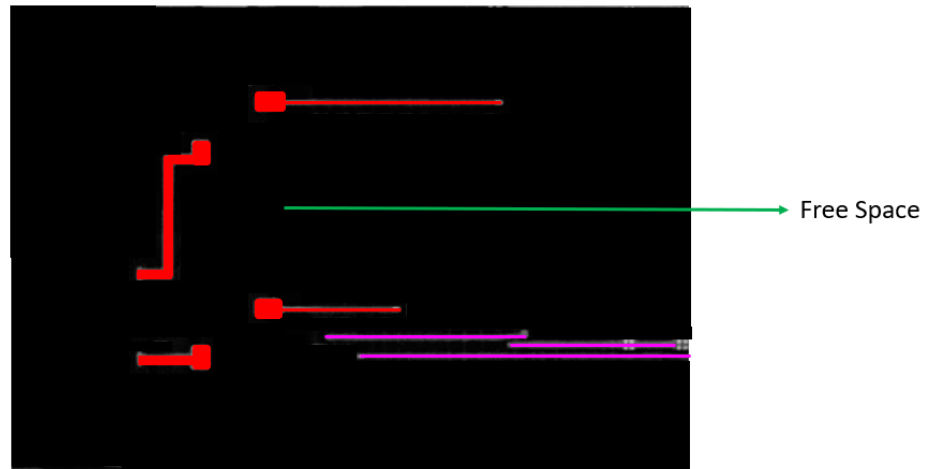
These same steps are carried out by Synopsys:
1. *See IC Compiler II Implementation User Guide , Version Q-2019.12-SP4, June 2020, page 544-545.*
2. *See* https://www.eetimes.com/in-design-metal-fill-key-to-physical-verification-turnaround-time-for-advanced-ic-designs/

These same steps are carried out by Siemens:
See http://soiconsortium.eu/wp-content/uploads/2018/10/2017_0616_GF-Fill-Flows-with-Calibre-DAC2017_v1.4-FINAL.pdf , page 11-13.

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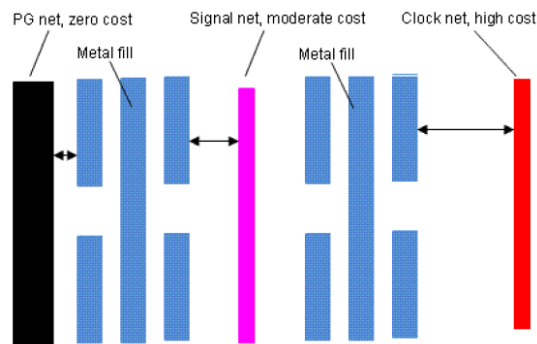|	
	For example, NXP creates a circuit design for the NXP LS1043A Quad-Core Networking Processor , which was made, produced, or processed from that circuit design created using one of the above-identified and described design tools such that free spaces are identified on each layer of the circuit design suitable for dummy metal insertion as dummy regions. As shown below and as explained by semiconductor expert Lloyd Linder ("Linder") in Exhibit C cited herein, in the NXP LS1043A Quad-Core Networking Processor the placement of dummy fill first requires the identification of locations suitable to receive the fill. *See* Ex. C at ¶¶ 35, 57–60, 62. These locations are identified by the green arrow.
(b) prioritizing the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets.	The Accused Products are made, produced, or processed from a circuit design that prioritizes the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets.

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Timing-Aware Metal Fill

When it adds a timing-aware metal fill, the Innovus software avoids adding the fill near clock and signal nets and adds more near the power and ground nets.

The software assigns a high cost to adding a metal fill near clock nets, a moderate cost to adding it near signal nets, and zero cost to adding it near power and ground nets. It adds the fill, based on the cost, to achieve the preferred metal density with the least effect on timing.

The software adds timing-aware metal fill by default.

- To add a non-timing aware metal fill, type the following command:
  ```
  addMetalFill   -timingAware off
  ```

- To use the Innovus common timing engine (CTE) for static timing analysis (STA), type the following command:
  ```
  addMetalFill -timingAware sta -slackThreshold  value
  ```

  If the timing graph is already built, the software adjusts the costs as a function of the slack (nets with the worst slack have the highest cost). For more information, see Timing Analysis.

  When you run the software in the STA mode, it assigns costs to four categories of nets:

- Clock nets are assigned the highest cost.

- Signal nets that have a slack value less than the threshold are assigned a moderate cost. You can use `-slackThreshold` and `-extraCriticalNet` to choose critical signal nets.

- Non-critical signal nets are assigned a small cost.

- Power and ground nets (nets marked `+ USE POWER` or `+ USE GROUND` in the DEF file) are assigned zero cost.

See Innovus User Guide product version 20.10, March 2020, page 709-710.

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A novel cost based timing aware metal fill algorithm has been implemented to minimize the timing impact from metal fill while meeting minimum density requirements.
In the current metal fill algorithm we do:
   For each region
      For each layer: Do until target density is met
         Generate metal fill candidate
         Calculate cost for each candidate.
            Cost = C (aSp, W, L)
         Sort metal fill candidates by cost.
         Select candidate
      End for each layer
   End for each region

In this approach we assign different costs to different set of nets according to timing criticality. Fills not close to any nets or close to regular nets have the lowest cost. Next fills with proximity to power/ground nets will have higher costs. Finally fills close to clock nets or critical nets will have the highest costs. Based on this cost system we can minimize the parasitic impact from metal fill for both same layer and interlayer. In addition a tight integration with a

In this approach we assign different costs to different set of nets according to timing criticality. Fills not close to any nets or close to regular nets have the lowest cost. Next fills with proximity to power/ground nets will have higher costs. Finally fills close to clock nets or critical nets will have the highest costs. Based on this cost system we can minimize the parasitic impact from metal fill for both same layer and interlayer. In addition a tight integration with a

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timing engine is built in to use the critical nets information combined with the timing aware to feed the critical nets information into timing aware metal fill. Figure 1 shows a simple layout to illustrate the cost based timing aware metal fill. In this figure the fill candidate that is closest to clock net CLK has been assigned the highest cost of three. The fill candidate close to a power net VDD has been assigned a relative lower cost of two and the fill candidate that is far away from both power and clock nets has been assigned the lowest cost of one. The fill with lowest cost of one will be picked first and then the fill candidate with cost of two and lastly the one with cost of three which will be avoided if minimum density is met.
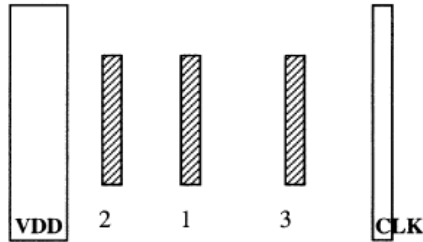

Figure 1. Cost based timing aware metal fill

See X.Dong; et. al., New Metal Fill Considerations For Nanometer Technologies, ASICON 2005 (6th International Conf.), page 805.

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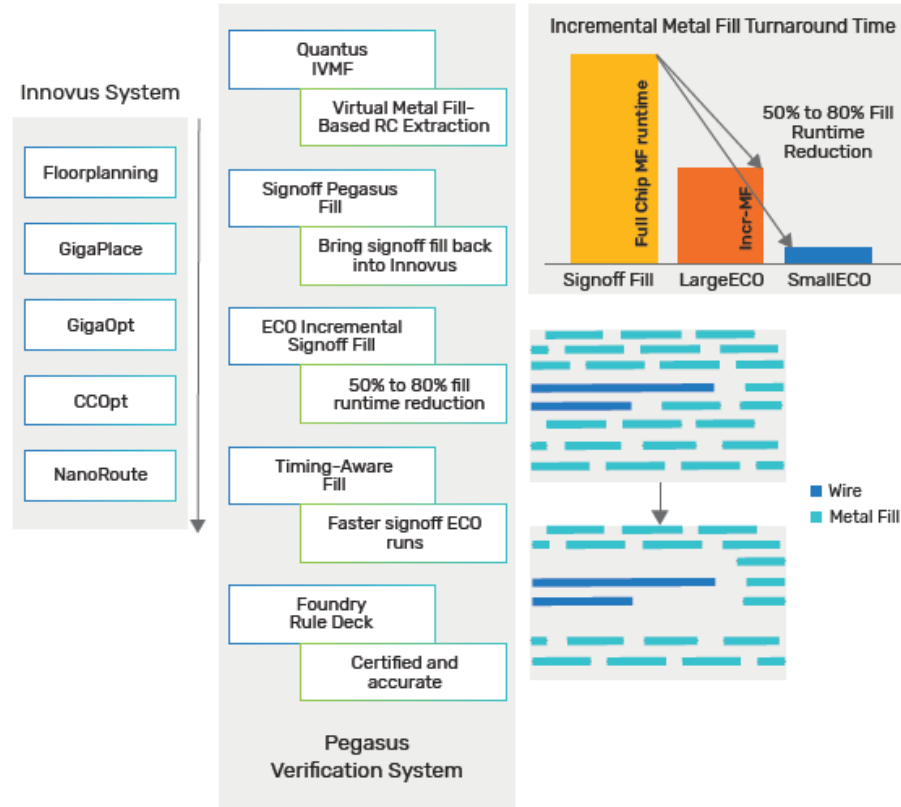CADENCE CUSTOMER NXP
U.S. Patent No. 7,007,259

Figure 3: The timing-aware, integrated metal fill design flow

See https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf , page 3.

These same steps are carried out by Synopsys:
1. *See IC Compiler II Implementation User Guide , Version Q-2019.12-SP4, June 2020, page 544-546*
2. *See https://www.synopsys.com/content/dam/synopsys/implementation&signoff/white-papers/icv_signoff_metalfill_wp.pdf , page 4*

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3. See https://www.eetimes.com/in-design-metal-fill-key-to-physical-verification-turnaround-time-for-advanced-ic-designs/

These same steps are carried out by Siemens:
1. See http://soiconsortium.eu/wp-content/uploads/2018/10/2017_0616_GF-Fill-Flows-with-Calibre-DAC2017_v1.4-FINAL.pdf , page 11-13.

For example, NXP creates a circuit design for the NXP LS1043A Quad-Core Networking Processor , which was made, produced, or processed from that circuit design created using one of the above-identified and described design tools to prioritize the dummy regions using "cost" such that the dummy regions located adjacent to clock nets are filled with dummy metal last because they are assigned a "high cost" compared to other regions that are assigned lower "cost." The prioritization of clock nets such that adjacent dummy regions are filled with dummy metal last is apparent from visual inspection of the integrated circuit layers, as shown below. See Ex. C at ¶¶ 35, 57–60, 67–68. The NXP LS1043A Quad-Core Networking Processor includes a clock net identified by the green arrow and dummy metal identified by the blue arrow. This minimizes any timing impact on the clock nets.
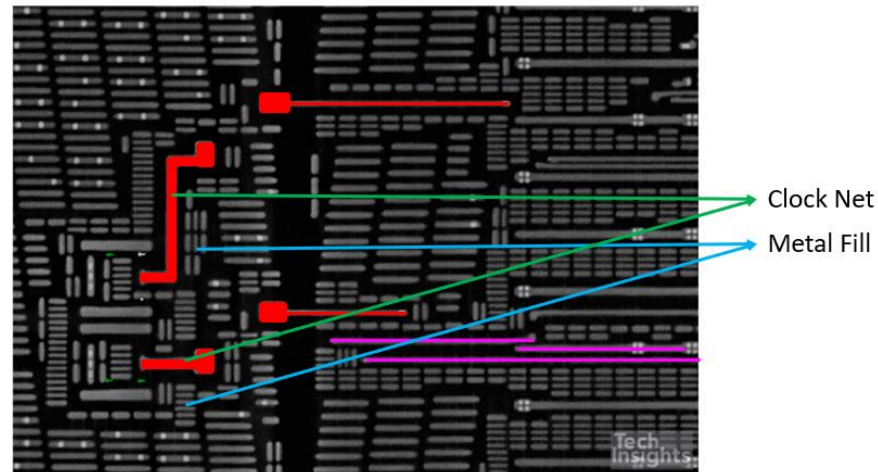
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Caveat: The notes and/or cited excerpts utilized herein are set forth for illustrative purposes only and are not meant to be limiting in any manner. For example, the notes and/or cited excerpts, may or may not be supplemented or substituted with different excerpt(s) of the relevant reference(s), as appropriate. Further, to the extent any error(s) and/or omission(s) exist herein, all rights are reserved to correct the same.

EXHIBIT C

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   Attorneys for Plaintiff
20

21   IN THE UNITED STATES DISTRICT COURT
22   FOR THE SOUTHERN DISTRICT OF CALIFORNIA

23 BELL SEMICONDUCTOR, LLC,

24   Plaintiff,   Case No. **'22 CV594 BEN KSC**

25   v.   **DECLARATION OF LLOYD F.**
                                   LINDER
26 NXP USA, INC.,

27   Defendants.   **DEMAND FOR JURY TRIAL**
28

   DECLARATION OF LLOYD F. LINDER

1. I make this declaration on behalf of Bell Semiconductor, LLC ("Bell Semic"). I understand that Bell Semic will offer my declaration as evidence in support of the above-captioned patent infringement lawsuit against NXP USA, Inc. ("NXP").

2. My qualifications to testify concerning the relevant technology are set forth in my curriculum vitae, which is attached hereto as **Exhibit 1**.

3. I received my Bachelor of Science degree in Electrical Engineering (BSEE) from UCLA in 1985. I received my Master of Science degree in Electrical Engineering (MSEE), also from UCLA, in 1987. Thereafter, I continued studying Electrical Engineering at USC, where I received an Engineer's Degree in 1989 and researched and completed my thesis towards a doctoral degree in 2002. Following the completion of my BSEE, I began work at Hughes Aircraft, for 12 years.

4. When Hughes Aircraft was acquired by Raytheon in 1997, my title was "Senior Scientist."   At Hughes Aircraft, I was the technical lead for RF/analog/mixed signal IC development and was a subject matter expert (SME) in integrated circuits, serving as a company-wide resource for review of integrated circuit designs and technical support of new business.

5. My next position was as an Engineering Fellow at Raytheon from 1997–2002, where I again was the technical lead for RF/analog/mixed signal IC development and was a subject matter expert (SME) in integrated circuits, serving as a company-wide resource for review of integrated circuit designs and technical support of new business.

6. In February 2002, I began a role as Director of Technology at TelASIC Communications, a company that I also founded. In this role, I served as the technical lead for the development of state-of-the-art ADC (analog-to-digital converter) and DAC (digital-to-analog converter) commercial products for the cellular base station market.

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DECLARATION OF LLOYD F. LINDER

7.   In 2006, I began working under "Lloyd Linder Consulting" as an Independent Integrated Circuit Design, Systems, Intellectual Property, and Wireless Consultant, a role that continues to this day. In this role, I have served as a consultant to over 100 companies in the commercial and military contractor semiconductor component market space and have served as an expert witness in semiconductor cases and invalidity analyses.

8.   From 2008–2009, overlapping with my consulting, I took a position at Menara Networks for approximately 10 months, where I was involved with the development of an electronic dispersion compensation (EDC) IC and the development of quad transceiver for next-generation 10 Gb/s ASICs with integrated FEC / EFEC in CMOS.

9.   I have received various honors over the course of my education and career. In 1985, I was named UCLA's most outstanding senior electrical engineering student, graduating Phi Beta Kappa and Summa Cum Laude. I am an IEEE Senior Member and served as a Judge for the San Fernando Valley Section Entrepreneurial Business Plan Competition in 2008. I am a named inventor on over 100 issued United States Patents (with several currently pending) and over 300 international patents, and have published over a dozen journal and conference papers focusing on semiconductor design and layout. I am a two-time Hughes Aircraft Division Patent Award Winner, and was named by Hughes as a Masters Fellow, Engineers Fellow, and Doctoral Fellow.

10.   I have reviewed U.S. Patent No. 7,007,259 to Shrowty ("Shrowty '259) asserted in the Complaint, and its file history (in which the Patent Office allowed the application as-filed on the first office action), and the claim charts accompanying the Complaint supported by this Declaration.

11.   My college education over 15 years and 35 years of knowledge and experience in integrated circuit design, layout, and fabrication provides the

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DECLARATION OF LLOYD F. LINDER

1   necessary experience to support my stated conclusions set forth below.

2   **Background on Integrated Circuit Design and Layout Process Flow**

3   12.   I have created the image below, which provides a simplified schematic

4   showing, at a high level, a commonly-used integrated circuit design flow process

5   that is representative of many (if not most) process flows in current use:

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DECLARATION OF LLOYD F. LINDER

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TYPICAL DESIGN FLOW

-4-

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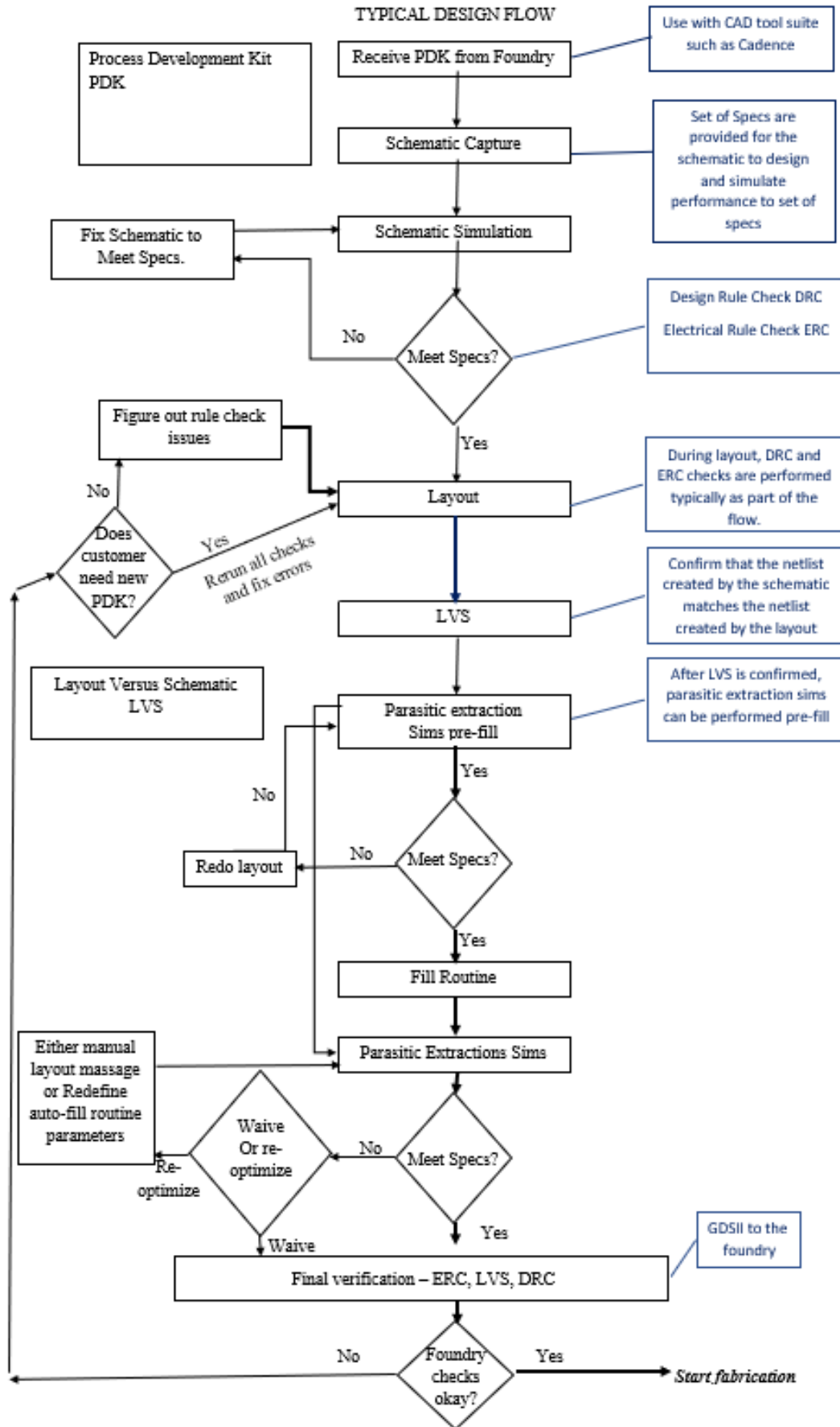
13.   The integrated circuit design flow process includes a design engineer, using design tools, to create a design for an integrated circuit to be processed.

14.   Design tools from vendors such as Cadence, Synopsys, or MentorGraphics (now Siemens) will then be used to design, simulate, and lay out integrated circuits. The typical design tool suite includes[1] schematic capture, simulation, layout, verification (layout versus schematic (LVS) and design rule check (DRC)), and fill generation routines. These fill routines can be automated or manual, and can be provided by the design tool company in whole or in part.

15.   To be sure, the precise capabilities of each design tool available to a particular design engineer may differ within a company (based on what options in the design suite are available to a particular user or on a particular device), and between different design tool suites. However, based on my experience, at a high level, the design tools used by design engineers in the semiconductor industry, all operate in substantially similar fashion for schematic capture, simulation, layout, verification, design rule check, and fill-generation. In particular, based on my experience as a consultant, the design tools commonly used in the industry to place dummy fill operate in substantially similar fashion in providing timing-aware fill generation for integrated circuit layouts.

16.   In the design process, the schematic is created first. The layout design tool is used to place and route all of the active (i.e., transistors) and passive components (i.e., resistors, capacitors, and inductors), and the interconnections between devices (represented as wires) in the schematic. It represents the circuit function that is to be physically implemented in the silicon. The schematic is created and simulated, using the CAD tools, to confirm that the circuit functions to a desired specification.

---

[1] Sometimes electrical rule check (ERC) is also included in design tool suite capabilities.

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DECLARATION OF LLOYD F. LINDER

17.   Once that performance specification is confirmed from the schematic simulation, the layout of the circuit is performed to physically place each of the individual elements necessary to implement the circuit functions set forth in the schematic.   During layout, layout rules for active and passive devices must be followed, but conformance is not checked until a DRC is run (typically at least as part of the final verification, though it can be run at any point or points in the layout process).

18.   Once the layout is completed, it is compared to the schematic of the circuit using layout-versus-schematic (LVS) tool to confirm that the two are identical.   From the schematic, a netlist (a list of devices and the associated nodes) is generated. From the netlist, the schematic could be re-generated by hand by drawing the devices and connecting the device nodes.   From the layout of devices and associated nodes, a corresponding netlist is generated, from which a similar schematic could be generated by hand by drawing the devices and connecting the device nodes from the layout netlist.   Then the schematic netlist is compared to the layout netlist using the LVS tool. The LVS tool compares the netlist from the schematic to the netlist for the layout to see if they match—i.e., whether they contain the same devices connected in the same fashion. If they do not match, the discrepancies between the two must be found and corrected, and LVS re-run.   Any violations of layout rules must be corrected and DRC re-run for the layout.

19.   After passing LVS, the process of performing parasitic extraction simulations before the fill has been placed (pre-fill) can be performed on an extracted netlist created from the layout. If parasitic simulations are performed prior to the fill placement, the designer can get an idea of the impact on circuit performance from the basic layout parasitics pre-fill.   From the layout, a netlist is extracted that includes any of parasitic resistance (R), parasitic inductance (L), parasitic capacitance (C), or any combination of the three.   Additionally, the

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DECLARATION OF LLOYD F. LINDER

1 parasitic extraction can include what is termed "coupled" capacitance (parasitic

2 capacitance between metal lines) as well as the parasitic capacitance to the

3 substrate. The extracted netlist, with the selected added parasitics, can be used to

4 run simulations on the baseline layout to determine if there is any performance

5 degradation due to the baseline layout routing.

6   20.   The simulated performance of the layout, which includes the

7 parasitics, needs to be as close as possible to the specification that was already

8 satisfied by the schematic. That is why parasitic extraction is performed, and why

9 it is iterated pre-fill and post-fill. So if there is performance degradation due to the

10 baseline layout, the layout is redone until its performance is at acceptable

11 parameters.   Ideally, the extracted simulation results match the schematic

12 simulation results, which means that the layout parasitics had no impact on the

13 circuit performance.

14   21.   Once the layout passes pre-fill, the design tool is used to insert dummy

15 fill at appropriate locations in the layout that do not contain devices or other

16 features. As is well-known in the industry, the purpose of adding dummy fill is to

17 achieve a higher and more uniform density of interconnect across the surface of

18 each layer of the chip, to improve the outcomes of the chemical-mechanical

19 polishing/planarization (CMP) step during fabrication. This lowers the likelihood

20 of defects caused by the CMP process step and thus improves the yield of modern

21 integrated circuits.

22   22.   As the pre-fill step confirms that parasitics of the baseline layout, pre-

23 fill, do not degrade the performance of the integrated circuit, it is desirable that the

24 fill likewise does not degrade performance. However, depending on its placement,

25 dummy fill can also degrade the performance of the integrated circuit, which is

26 undesirable. To minimize this, the design suites include timing-aware fill tools that

27 minimize, if not prevent, any degradation to circuit performance caused by dummy

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DECLARATION OF LLOYD F. LINDER

fill insertion.

23.   Based on my experience, use of such timing-aware fill tools has become standard practice in designing modern integrated circuits. In fact, modern integrated circuit designs are required to have fill included as part of the database submitted for fabrication. Due to the complicated nature of these designs, such as SoCs and highly integrated circuits with many layers, the fill process cannot be manual at least for the practical reason of there being far too many locations to designate by hand for fill insertion. Moreover, the chip has many critical nets, so there is a need for the fill-placement to be aware of any impact on the timing and resulting performance impact of the circuit. Timing-aware fill tools are used to attempt to meet interconnect density and timing closure requirements simultaneously, but they are not guaranteed to do so 100% of the time. When this occurs, a decision must be made to compromise performance at the expense of yield, or vice-versa.

24.   Once the fill routine is completed, the fill checks are done, and final verification is performed again (LVS, DRC). The fill checks are performed based on percentage requirement on a specified area in the layout.

25.   Once the layout database has been verified, it is sent for fabrication in the form of a Graphic Design System (GDSII) database, which is the industry standard format for delivery of the chip database. As previously mentioned, fill is required to be included as part of the GDSII database.

26.   The design resource is provided with a process design kit (PDK), which includes all of the information necessary to capture a schematic, run a simulation, do a layout, and perform all of the checks on the layout to make sure that the final GDSII is in an acceptable form to be ready for fabrication. It is the design resource / customer's responsibility to make sure that the designed chip meets all of the expected requirements for fabrication and bears the risk of failing

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DECLARATION OF LLOYD F. LINDER

1   to follow any steps in the design flow. For example, if the circuit does not work,

2   that is the customer's responsibility. If the layout does not match the schematic, that

3   is the customer's responsibility. The GDSII does have to meet all of the DRCs in

4   order to be fabricated.

5   27.   In order to develop an integrated chip product, tools are needed to

6   develop the schematic, the layout, verification of the layout, and the final GDSII

7   database for fabrication. Many companies use different tools (from different

8   vendors) to accomplish this process either typically due to cost or preference of

9   internal proprietary tools. Regardless of the process and specific tools that are used,

10 the GDSII database goes through an internal DRC after it is received and before

11 fabrication of the integrated chip:

    a. The design resource receives a PDK that contains all of the information
       is included to create a GDS database to release for fabrication. This
       includes circuit symbols for the creation of the schematic, models for
       the circuit symbols to run simulation, and associated layout devices
       that have been created with all of the process layers needed.

    b. Additionally, there are what are known as "rule decks" in the PDK that
       allow for LVS and DRC. A rule deck is typically a file that specifies
       all of the available rules, (for example, minimum line width), the layers
       to process on each rule, and the parameters of each rule. The LVS
       deck compares the schematic to the layout, and the DRC deck covers
       all of the design rules for placing and routing devices. For LVS, a
       netlist of the layout is created. This netlist is compared to a netlist
       created for the schematic. The LVS tool compares the two to determine
       if they match or not.

    c. Additionally, there is a parasitic extraction deck that extracts all of the
       parasitics of the layout that is used to run simulations to close timing

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or to confirm that the layout still meets all of the chip requirements.

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d. There can also be an electrical rule check (ERC) deck as well, depending on the fabrication involved.

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28. If the DRC rules at pre-fabrication do not match those at the design resource, it is possible that there will be DRC errors. This could be due to a number of reasons, including the DRC in the provided process design kit (PDK) is not up to date, and so the PDK will be updated with the updated DRC and the design resource will have to redo everything and fix the DRC errors, providing a new GDSII database before fabrication can begin. These DRC checks at pre-fabrication will include checks for the fill on all layers to confirm that the fill requirement is met, on a granular level, for all "boxes" at the chip boundary level.

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Dummy Fill is Required in Design and Layout of Multi-Layer Semiconductor Chips

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29. To the best of my knowledge, adding dummy fill is a requirement for every integrated circuit using the latest technology nodes. Certain older nodes still in fabrication (>350nm) may not require fill, but I believe that even some of these older technology nodes have incorporated fill requirement to enhance yield.

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30. As mentioned above, it is required that the GDS database include fill within the database submitted for fabrication. In particular, most fabrication processes used in modern semiconductor chip designs require a minimum density for the interconnects (i.e., pieces of metal or semiconductor) placed on each layer of a multi-layer chip design. This is the case both for the layer as a whole and for individual subunits of each layer, and is fundamental to the creation of consistent fabrication of multi-layer devices with minimal defects.

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31. Fabrication processes typically partition each layer of the chip design into rectangular regions called tiles, each of which must also meet a minimum density requirement. For any given region of the chip, the interconnect density is

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the area of all of the interconnect in that region divided by the total area of that region.

32.   Sufficient interconnect density and substantial uniformity of interconnect are required for the chemical mechanical polishing (CMP) portion of the chip fabrication process. CMP is crucial to achieve planarity, which allows for multi-layer chip designs and high yield of functional devices. Insufficient interconnect density and/or insufficient uniformity of interconnect between various regions will increase the likelihood of defects during the chip manufacturing process, which will resultantly degrade the yield.

33.   Once the functional features of the chip design (such as power lines, signal nets, vias, and the like) have been laid out as needed in the first instance, there will usually be substantial portions of the chip design that have insufficient interconnect density to permit CMP without incurring substantial likelihood of defects.

34.   To increase the interconnect density of the layer as a whole, and of regions within each layer, pieces of interconnect are inserted into available space in low-density regions of the chip until the minimum interconnect density specified for the particular fabrication process is achieved for each tile. Because these pieces of interconnect are not intended to carry signal or power, but instead are added to provide structural stability to the chip architecture, they are generally known as "dummy fill."

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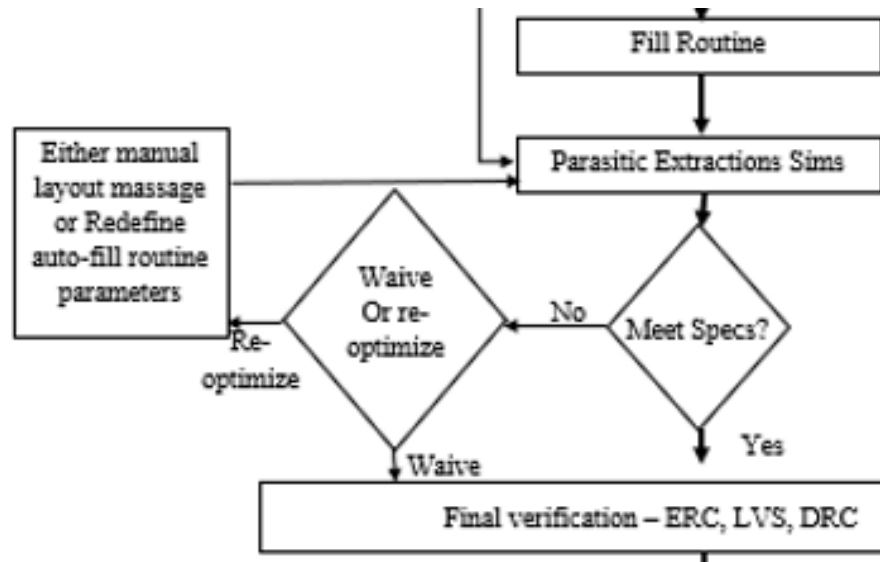
11   35.   Placement of dummy fill is typically performed by a dummy fill
12   software tool, and is one of the last steps in the chip design flow, with its extent and
13   placement typically occurring after routing and timing closure. The dummy fill
14   software tool examines the tiles in each layer of the design, and if the interconnect
15   density in each tile does not meet (or exceed) the specified minimum interconnect
16   density for the fabrication process, the dummy fill tool inserts dummy fill into free
17   regions of that tile where no interconnect is present.

18   36.   For large integrated circuits, commonly called system-on-a-chip (SoC)
19   with either large analog content and small digital content ("big A, little D") or large
20   digital content and small analog content ("big D, little A"), it is not practical to
21   manually add dummy fill, so automated fill routines are almost always used.
22   Because there are so many critical signals in a large SoC, the process cannot be
23   done manually due to the time it would require. Thus, the design timelines and
24   practical realities require that the automated fill routines are used instead.

25   37.   However, placing the dummy fill too close to signal nets increases
26   capacitance between the signal wires and the dummy fill, which in turn slows the

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transmission speed of signals and degrades the overall performance of the integrated circuit. This effect is undesirable and is known as "parasitic capacitance."

38. The added parasitic capacitance will degrade parameters, such as operating frequency and rise/fall time, for a critical clock or signal, and this must be avoided in order for the circuitry to work properly.

39. The parasitic capacitance is inversely proportional to the distance between the dummy fill and the signal wire. Thus, parasitic capacitance from dummy fill will be minimized if the dummy fill is placed far from signal nets.

40. Prior to Shrowty '259, the traditional solution to minimizing the parasitic capacitance effect of dummy fill was the "simplistic approach" of hardcoding a large "stay-away" distance from crucial signal nets, essentially establishing a defined "exclusion zone" (or "keep-out area"), essentially a "moat" around those circuit elements that would be designated categorically unsuitable to receive dummy fill when the dummy fill software tool was utilized. The distance was typically derived empirically for each design by studying the effect on timing from dummy fill inserted at various distances from clock nets in sample designs and was then manually hardcoded in the dummy fill libraries for each type of process technology.

41. The result of using these keep-out zones was that potentially the chip would have poor yield. Since this was a manual time-consuming process, with limited time available, the result would typically be that the fill requirements could possibly not be met, and a waiver would be requested before fabrication would begin, with any resulting yield degradation being accepted by the customer..

42. By excluding dummy fill from being placed within a certain distance of crucial signal nets, its parasitic capacitance can be bounded below a particular value and its effect on circuit timing can be minimized. However, hard-coding a large "stay-away" distance between dummy fill and signal nets, creating a region in

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1   which dummy fill cannot be placed, will also reduce the space available for dummy

2   fill insertion and thus limit the overall interconnect density that can be achieved.

3   43.   In other words, the higher the required interconnect density, the closer

4   it must be placed to signal nets, with increasingly higher parasitic capacitance and

5   negative impact on timing and circuit performance. Conversely, the more sensitive

6   the timing requirements for the circuit, the less the parasitic capacitance can be

7   tolerated near crucial signal nets and the lower the interconnect density can be for

8   tiles that include such signal nets. This tradeoff is further complicated when

9   multiple metal layers are involved, which can be ten or even more.

10   44.   It may be that the timing requirements cannot be met without a revision

11   to the fill placement and re-extraction of the layout parasitics to determine if the

12   timing requirements are met. If they are not, then a decision would have to be made

13   to continue the iteration process or apply for a waiver and bear the risk of lower

14   yield, or accept decreased performance

15   45.   Balancing this tradeoff started to become particularly problematic by

16   the early 2000s, as new processing technologies with smaller and smaller features

17   demanded increasingly higher minimum interconnect density values at the same

18   time that chip designs became much more aggressive in the circuit timing

19   requirements. In such cases, it was often impossible to insert sufficient dummy fill

20   into a tile such that the higher minimum density requirements could be met without

21   also reducing the large "stay-away" distance, and thereby raising the timing impact

22   of the dummy fill to levels that affected the performance of the chip. One potential

23   solution was for the chip designer to waive the minimum interconnect density

24   specified by a particular fabrication process. However, because invoking this

25   waiver would not comply with the fabrication process requirements, the yield of the

26   produced devices would not be guaranteed in such cases, which rendered this

27   alternative not viable in practice.

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46.   Traditional dummy fill software tools of that time often completed their run through the tiles of each layer without reaching minimum interconnect density in some cases. In such cases, it would be necessary to re-run the dummy fill tool for those problematic tiles with a lowered "stay-away" distance. If, as frequently occurred, more than one such tile lacked sufficient interconnect density and required (at least) a second run of the dummy fill tool with the revised "stay-away" distance parameters, multiple runs could be needed if, as was typical, the dummy fill tool could only handle one tile at a time.

47.   This iterative process, with manual adjustments of the "stay-away" distance and requiring multiple runs for each such affected tile was an involved, time-consuming process that can and did significantly impact design schedules.

**Explanation of Shrowty '259**

48.   Thus, multiple iterations of manually adjusting the "stay-away" distance in each tile were, prior to Shrowty '259, typically required to meet design demands and process requirements for dummy fill insertion of newer chip designs in an involved, time-consuming, and *ad hoc* fashion.

49.   In place of this methodology, Shrowty '259 teaches a dynamic method of placing dummy fill that, in a single run, achieves the required minimum interconnect density while simultaneously minimizing the negative timing impact of the inserted dummy fill on clock nets. (Shrowty '259 at 2:19–23.) This avoids delays to the design schedule that would likely result from the use of traditional methods of dummy fill insertion in designs with high interconnect density requirements and demanding timing tolerances and produces improvements in the IC design process flow as well as reducing the design time required to complete a design.

50.   Shrowty '259 explains that to solve this problem, free spaces on each layer of the chip suitable for dummy metal insertion (known as "dummy regions")

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are first identified on each layer of the chip design suitable for dummy fill, known as the "free-space finding" phase. (2:29–32 & Fig. 2.) Thereafter, the dummy regions are prioritized such that those adjacent to clock nets are filled with dummy metal last until the minimum density requirement is met, in the second or "dummy metal insertion" phase. (2:32–43 & Fig. 5.) In some embodiments, the dummy regions are further prioritized such that those adjacent to wider clock nets are filled with dummy metal after regions that are located adjacent to narrower clock nets. (2:35–38.)
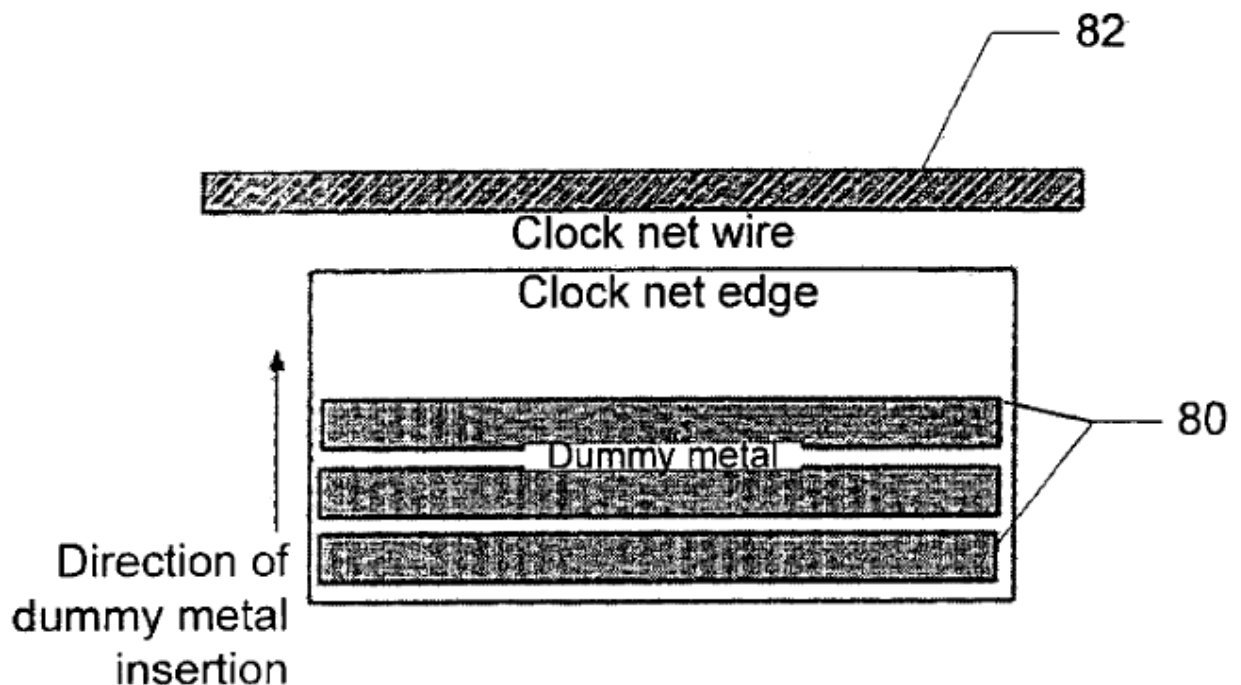
51.   Shrowty '259 also teaches that when an existing object intersects a dummy region, its area is added to the interconnect area property for the region, and it may be partitioned into up to four sub-dummy regions around the subtracted area, with the newly-created sub-dummy regions replacing the originally-designated dummy region in the list of areas in the tile suitable for dummy fill insertion. (4:7– 23 & Fig. 3.)
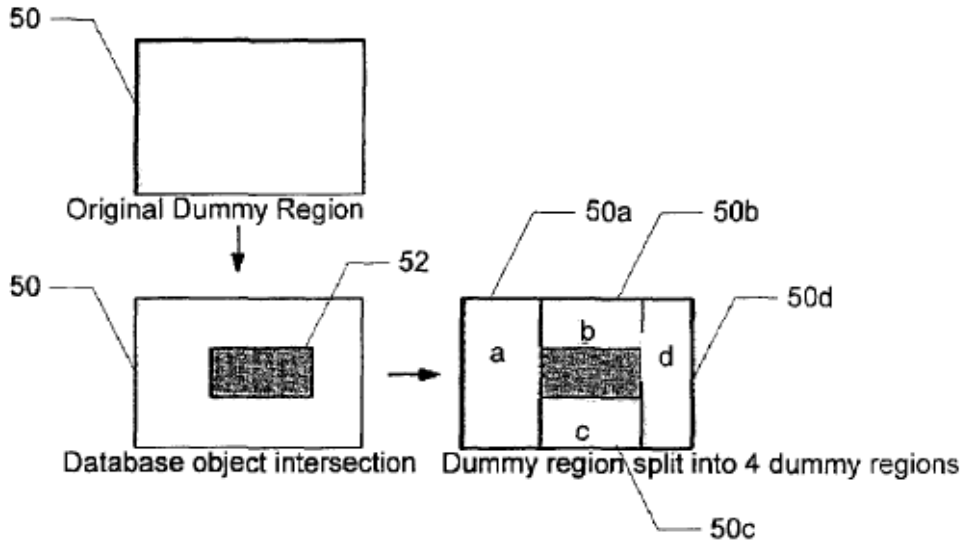
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FIG. 3

12   52.   Shrowty '259 explains that, as a result, minimal dummy fill (if any) is inserted into clock net-adjacent dummy regions, thereby minimizing the timing impact to the adjacent clock nets. (2:43–47.) As would have been clear to a POSITA, this would improve the performance of the resulting integrated circuit both in terms of minimizing the likelihood of manufacturing defects arising from CMP and minimizing the negative impact of parasitic capacitance on timing and transmission speed.

19   53.   The minimization of timing impact on clock nets from dummy fill as taught by Shrowty '259 is expressly recited in every claim of Shrowty '259. Specifically, it is recited in every independent claim, i.e., in element (b) of independent claims 1 and 18, and in element (e) of independent claim 35. Thus, it also applies to all of their dependent claims as well.

24   54.   I have also reviewed the prosecution history of Shrowty '259, which the USPTO allowed on the first office action. The Examiner's Notice of Allowance recognized that the prior art, whether alone or in combination, did not disclose or

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1   suggest that dummy regions are prioritized such that those located adjacent to clock

2   nets are filled with dummy metal last, nor that those adjacent to increasingly wider

3   clock nets are filled last. Based on my experience in semiconductor layout and

4   design, as set forth above, I agree with the Examiner's characterization of the

5   contents of the prior art in the Notice of Allowance.

6   55.   Moreover, based on my experience in semiconductor layout and

7   design, it was not well-understood, routine, or conventional at the time of Shrowty

8   '259 to fill dummy regions located adjacent to clock nets last, in a dynamic fashion.

9   As both the Examiner and Shrowty '259 recognized, the conventional methodology

10 at the time was to hardcode a fixed "stay-away" distance from or "exclusion zone"

11 surrounding clock nets, and, if necessary, to manually adjust that for individual tiles

12 that failed to meet the minimum interconnect density requirements for a particular

13 process. Based on my experience in semiconductor layout and design, I agree that

14 the claimed inventions of Shrowty '259 were not, to the best of my knowledge,

15 well-understood, routine, or conventional activity at the time of Shrowty '259. This

16 is true not only in an ordered combination of the elements, but also as an individual

17 claim element.In particular, the de-prioritization of tiles adjacent to clock nets as

18 locations suitable for dummy fill, as recited in element (b) of claims 1 and 18 and

19 element (e) of claim 35, was not, to the best of my knowledge, well-understood,

20 routine, or conventional activity at the time of Shrowty '259, either on its own or in

21 an ordered combination with the other elements of the independent claims.

22 **Claim Charts**

23   56.   I have reviewed the Complaint supported by this Declaration, along

24 with the Claim Chart (Exhibit B) showing infringement of Shrowty '259 by AMD

25 For the reasons set forth below, I agree that this Claim Chart establishes use of at

26 least one of the methods recited by the claims of Shrowty '259.

27   57.   I have used design tools from different vendors in my career. As a

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consultant, I use the tools to review schematics and layouts. Based on the requirements for the latest process technology nodes, and the yield requirements for these technologies, the latest fill tools are used by designers use timing-aware fill routines to meet timing as well as yield requirements simultaneously. As I have done as a consultant, I can review either layouts post-fill or reverse engineering ("RE") of semiconductor die to confirm that these tools have been used to construct the layout or the die.

58.   From the RE of an integrated circuit, it can be seen that timing-aware fill routines have been used in the layout simultaneous optimization of the fill and timing requirements. The RE shows that the critical nets have been prioritized with regards to the placement of fill for a given metal layer, in order to prevent, as much as possible, critical timing signal paths from degrading performance. This is obvious by inspection to one of skill in the art, such as myself, who can immediately see by eye that this was performed.

59.   In particular, based on my experience, information that a company is using a design tool suite—such as the Cadence Virtuoso and Innovus layout tools produced by Cadence Design Systems, and those produced by Synopsys or Siemens (formerly MentorGraphics)—indicates to me whether, from the layout of the produced devices and/or a detailed functional block diagram of the circuit in conjunction with the performance characteristics of that integrated circuit, that timing-aware dummy fill routines were used as recited in Shrowty '259.

60.   In particular, these layouts indicate visually, based on my experience in semiconductor layout and design, that dummy metal is laid out relative to clock nets as set forth in Shrowty '259, such that dummy regions are prioritized so that dummy fill is inserted last in dummy regions located adjacent to clock nets. As explained in greater detail above, it is always necessary to identify the locations where dummy fill may be inserted before the fill is inserted.

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61.   Even when the circuit layout is not available, the performance characteristics of modern integrated circuits, in combination with a detailed functional block diagram, allow me to determine whether timing-aware fill routines were used. That is because timing-aware fill tools are widely used, and modern timing requirements and processing steps would be impractical (if not impossible) to meet without the use of such automated tools. In addition, modern integrated circuit processes, with lower technology nodes, are needed to implement these complicated, highly integrated SOCs, even when seen from a block diagram perspective, and based on my experience, timing-aware fill is a required step in order to achieve commercially viable yields. Thus, in my experience, it can be assumed with a high level of confidence that such tools are used to place fill in every complicated integrated circuit.

62.   Based on my experience in semiconductor design and layout, all layout design tools necessarily identify free space on each layer of the circuit design suitable for dummy metal insertion as part of the dummy fill insertion process. In order for dummy fill to be inserted by such a tool, the locations suitable for insertion must first be identified and then designated as dummy regions. Thus, the use of a layout tool to insert dummy fill necessarily includes, and presupposes, the identification of the locations where that fill is to be inserted, and it necessarily exists on a layer prior to insertion of dummy fill. In other words, the existence of dummy fill on a metal layer, and its placement there by a layout design tool, indicates that free space suitable for insertion of the dummy fill was first identified and designated as an appropriate dummy region.

63.   In my experience, these tools operate by, among other things, maintaining a dummy region list for each tile in the design. Without maintaining such a list for each tile, the layout tool would not be able to ensure that each tile met the minimum interconnect density or that no more fill would be added once the

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interconnect density requirement was met.

64.   Based on my experience in semiconductor design and layout, such lists are initialized by the layout design tool for each tile as a single rectangle corresponding to the outline of the tile.

65.   Such layout design tools also step through the design database and subtract the outline of each object found within the current tile from the dummy region on which it lies, as has been standard for such design tools for some time. Likewise, such design tools, upon removing an object from the dummy region, partition the remaining area into sub-dummy regions, which are added to the dummy region list in place of the original dummy region containing an object.

66.   Based on my experience in semiconductor layout and design, timing-aware design tools, such as Cadence and Synopsys, at this point, will also store the wire width property as a parameter if that object has been identified / designated as a critical clock net wire, and then tag an edge of each dummy region located immediately adjacent to the clock net wire with a clock net edge property. This is so that the layout design tool can distinguish clock nets (which have a greater impact on timing even compared to other signal nets) from other nets that are much more tolerant of (or don't affect) timing variance.

67.   Similarly, based on my experience in semiconductor design and layout, the use of \step (b) of claim 1 of Shrowty '259 (and its dependent claims) is apparent to me from an examination of the circuit layout itself. In particular, the clock nets and signal nets having dummy fill located further away and/or at lower densities as compared to power and ground nets or less critical nets indicates that the dummy regions were prioritized such that those located adjacent to critical clock nets were filled with dummy metal last in order to minimize the timing impact on clock nets. These critical nets can be determined by inspection of RE.

68.   Based on my experience in using design tools for semiconductor

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1   layout and design, and my consulting work, which has included review and analysis
2   of the results of engineers using these layout design tools, they operate in certain
3   ways and all produce GDSII databases to create the physical chip, which is a
4   required step. They all operate substantially similarly with regard to placement of
5   dummy fill until the interconnect density in each tile meets what is necessary to
6   satisfy the CMP/yield requirements during processing without adding unnecessary
7   fill. In particular, at the very least, each of these tools maintains a dummy region
8   list for each tile in the design and inserts dummy metal into a circuit design by
9   identifying, as dummy regions, free space on each layer suitable for dummy metal
10 insertion and then prioritizes the dummy regions such that those located adjacent to
11 clock nets are filled with dummy metal last, in order to minimize the timing impact
12 of dummy fill on the clock nets in order to produce a GDSII database for fabrication.

13   69.   Even where reverse engineering of an integrated circuit is not
14 available, my experience in semiconductor design and layout gives me sufficient
15 basis to opine whether one or more of the methods claimed in Shrowty '259 have
16 likely been used in creating integrated circuits. In particular, for devices with high
17 complexity, high speed requirements, and low tolerance for timing adjustments, it
18 is highly likely that the dummy fill insertion was performed as recited by the
19 Shrowty '259 methods. In my experience, these methods are widely used in
20 designing modern integrated circuits, and it has become standard practice in
21 semiconductor layout and design, including through the use of layout design tools,
22 to prioritize dummy regions such that dummy fill is inserted into dummy regions
23 adjacent to clock nets only after all other dummy regions receive dummy fill.
24 Accordingly, I believe that I can determine the likelihood of such use even without
25 a reverse engineering of the physical chip layers from the circuit performance
26 specifications in conjunction with other detailed information about the device
27 design, such as a device functional block diagram and its labeling and/or associated

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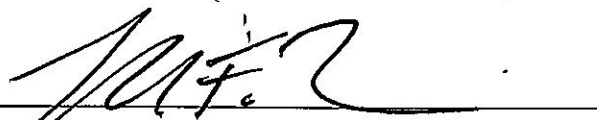
1   specifications.

2   70.   By contrast, based on my experience, I would only assume that
3   relatively simple IC designs would have been made in recent years without
4   employing at least one of the methods claimed in Shrowty '259, where the fill
5   requirement can be achieved through a manual process for small die.

6   71.   The Cadence paper "New Metal Fill Considerations for Nanometer
7   Technologies" demonstrates several things. First, the use of the word "new" is
8   justified in that it is a new approach, as documented here. Secondly, it evidences
9   that the Cadence tool suite is used for timing-aware driven decisions regarding the
10   addition of dummy fill to the layout. The paper is evidence of the tool support for
11   the principles discussed in the independent claims of Shrowty '259, particularly the
12   dummy fill insertion phase.

14   I declare under penalty of perjury under the laws of the United States of America
15   that the foregoing is true and correct.

17   Dated: April 27, 2022

21   Lloyd Linder

EXHIBIT 1

cell 818.632.9660
lflinder@yahoo.com
09/22/2021

Lloyd F. Linder

Skills summary

Extensive experience in high performance / high dynamic range analog mixed signal, custom digital, and RF integrated circuit design, layout, and test, from concept to production for commercial, military, and space IC products. Have knowledge of IC process development, characterization, and modeling. Have significant amount of experience in obtaining new military, space, and commercial IC business, as well as obtaining funding for start-up activities. Technical oversight for large IC design teams (20-40 people). Have ability to contribute creatively to the solution of difficult technical problems. Have 99 U.S. patents issued with twenty U.S. patents pending. Have 200-300 issued international patents. Have experience at the discrete analog / RF / mixed signal board level design and layout, system analysis, link budget analysis.

Specialties:

IP analysis / technical due diligence for M&A

IP portfolio management and creative contribution to new IP generation

Prior art searches and technical support for patent office action amendments

Perform simulations, review IP, and provide expertise in support of patent litigation

System Design/Architecture/Analysis/Block Specifications

New business development/capture

Winning proposals for small (SBIR Phase I and II) and large businesses

Product road maps

VC funding pursuits

Technical due diligence for VCs, angel investors, and M&A

IP creation and protection

Client deposition

Technical lead for IC design groups and product development

AMS/RFIC Design Chip/Circuit/System Architect

High speed, high performance ADC, Sample/Hold, ADC drvier amplifier, and DAC architectures

RF/AMS/SOC BIST/DFT architectures and methodologies

PLL and DDS

Digitally programmable RF transceivers/SDR/GPS/cellular/wireless transceiver architectures

RF TxRx, optical TxRx, modulator driver, LDD, TIA

Flash Ladar, active/passive imaging ROIC

regulators, high voltage/high current switches, ATE electronics

SiGe BiCMOS, CMOS, SOI, bipolar, Complementary bipolar, GaAs, InP

Digital beamforming

Cadence tools - schematic capture, SPECTRE, layout review

Solutions to production problems
Secret clearance

Objective
Looking for consulting opportunities to utilize my experience and provide technical leadership in all aspects of analog / mixed signal / RF integrated circuit and discrete circuit design: architectural conception, design, simulation, layout, test, and measurement / simulation correlation.

Experience
April 2006 – Present
Lloyd Linder Consulting
Consultant
Black Forest Engineering / Luminar Colorado Springs, CO.
  - Architecture development for next generation automotive lidar ROIC
Strategic IP Initiatives Inc.   Morgan Hill, CA.
  - Review of patent portfolio for PIC applications in SFP optical modules
GreyB Service Pte Ltd   Shaw Centre, Singapore.
  - Provide expertise for many different invalidity cases for many different clients
Upwork   Santa Clara, CA.
  - Technical writer for application notes and VNA user's guide
Syrnatec Inc.   Newington, CT.
  - Consult on ROICs for SBIR proposals
Kenney&Sams, P.C.   Boston, MA.
  - Expert witness in software defined radio development case
Microchip Technology Inc.   Burnaby, Canada
  - Participated in ADC architecture study for 28 and 56 GBps SERDES products.
  - Did webinar for world-wide IC design staff on ADC design issues.
ElevATE Semiconductor   Carlsbad, CA.
  - Write white paper on ATE products.
GoodIP GmbH   Munich, Germany
  - Review and analysis of GaN and LED patent portfolio for potential acquisition.
  - Spoke as the GaN / LED IP expert at webinar to discuss IP auction.
Nevada Nanosystems Inc.   Reno, NV.
  - Review and analysis of ASIC architecture and requirements in support of MEMS control circuitry. Evaluate IC design houses in the down-select process.
Axzon Inc.   Austin, TX.
  - Contribute to the analysis and review of CMOS transceiver architecture for UHF RFID reader.
Microcosm Inc.   Torrance, CA.
  - Architect the discrete RF transceiver and analog base band signal processing solution for digital beamformer. Develop packaging concepts for the beamfomer and interface to the antenna elements.
Otava Inc.   Moorestown, NJ.
  - Contribute to the definition of overall transceiver and circuit architectures for 5G beam formimg solution for 28-40 GHz 5G applications.
Analog Circuit Works   Boston, Mass.
  - Review of specification for fiber optic SOC application. Contribute to system level analysis and architecture.
Second Sight Medical   Sylmar, CA.

- Debug of current eyewear for blind people. Contribute to reduction of noise and coherent spurs in current product.

Linear Microsystems   Irvine, CA.

- Architect for high volume SOC for VR headset application. System analysis for SOC proposal for fiber optic communications applications.

Teqnovations   Colorado Springs, CO.

- System level architect for receiver for phased array radar applications.

Analog Devices Inc.   Colorado Springs, CO.

- Work with design team on a DAC buffer IC to improve performance in the lab and remove oscillation. Review existing architecture for redesign and developed new architecture.

Facebook   Woodland Hills, CA.

- Schematic and board layout reviews of electronics for flight system

GHB Intellect   San Diego, CA.

- Review of Patent claims for client for multiple issued patents in the wireless communications area.

BINJ Labs   Scituate, MA.

- Definition of top level Software Defined Radio architecture for wide band operation. Work with board development effort and SDR development company.

Sentinel Monitoring Systems Inc.   Tucson, AZ.

- Schematic review of high speed data converter and timing board schematic.

FlexPowerControl   Woodland Hills, CA.

- Consultation on system level requirements document in-home energy control product development. Develop IP for the company.

SpectraResearch   Dayton, OH.

- Consultation on integration considerations for discrete X-band and Ka / Ku-band transponder architecture for SWAP-C improvements.

McKool Smith   Dallas, TX.

- Perform simulations of IP for RFIC receiver, and provide expert opinion for patent litigation in a report for case :2:15-cv-00011-JRGRSP in the United States District Court for the Eastern District of Texas.

Quantum Semiconductor LLC   San Jose, CA.

- Consultation on architecture and simulations for proprietary ADC architecture.

Maven Research   San Francisco, CA.

- Consultation on use of design house by third party for products.

Faraday Technology Corporations   Santa Clara, CA.

- Review of third party transceiver RFIC schematic design, layout, and testability.

Irunway   Dallas, TX.

- Review of IP for legal firm in patent litigation. Simulation of IP for transceiver RFIC. Simulation results included in expert report.

Alphacore Inc.   Phoenix, AZ.

- Architecture review and enhancements of high speed CMOS ADC and visible monolithic imaging chips. Develop DROIC architectures for SBIR proposal pursuits.

Brady Worldwide Inc.   Milwaukee, WI.

- IP review of start-up for potential investment / acquisition. Develop sensitivity analysis for present products and future CMOS technology scaling.

InPhi Corporation   Westlake Village, CA.

- Review and contribute to architecture refinements for single channel and multi-channel EAM drivers for 2 level and 4 level PAM. Perform architecture study for low power EAM driver.

DRS RSTA Inc.   Cypress, CA.

- Help with EDA methodology for AMS design for ROICs.

Ridgetop Group   Tuscon, AZ

- Architected wide band RF front end for multiple current SBIR proposals.

Space Micro   San Diego, CA

- Review of 0.18 μm CMOS quadrature DAC design and layout.

Teradyne   Agoura Hills, CA

- Analog DFT / BIST / testability architect for 40 nm CMOS SOC for next generation Teradyne tester. Architect transistor level circuit solutions for power supply IC for DUT testing. Investigate high voltage CMOS and complementary bipolar process technologies for internal design development with unique current clamping architecture. Define baseline circuit topology and perform simulations.

Lockheed Martin   Moorestown, New Jersey

                                       Littleton, Colorado

                                       Deer Creek, Colorado

- Involved in high voltage driver IC development for GaN PA.

- Involved in architecture development and review of wide band band receiver integrated circuits from DC to Ka / Ku in SiGe.

- Involved in overall ADC architecture development and definition, and transistor level circuit architectures, for next generation RFIC transceivers and data converters. Architect of next generation transceiver architectures for SOC / heterogeneous applications. Involved in study for government customer of data converter architectures for next generation digital beam forming applications. Architecture review and development for high voltage analog driver array. Involved in architecture for multiple receiver RFIC developments for S, C, and Ka bands.

HRL   Malibu, CA

- Perform market survey of component technologies for multi-mode, multi-mode commercial software defined radio applications. Summarize capability for data converters, front end modules, antennas, transceivers, and base band processors. Compare the available technology to an architecture based on custom chip development for the solution.

Micrel   San Jose, CA

- Involved in the testing, debug, and redesign of a 65 nm CMOS 2.4 G / 5 G WiFi transceiver product. Provide technical guidance for redesign of RF front end and the 2.4 G / 5 G LO clock distribution.

Key2Mobile   Westlake Village, CA

- Developed RF transceiver concepts for multi-band, multi-mode remote radio head system. This is included transceiver architectures based on digital beam-forming and direct RF sampling and direct RF synthesis data converters.

Hittite Microwave   Colorado Springs, CO

- Consultant on the architecture for the high dynamic range, high speed IBM SiGe 8HP BiCMOS DAC and complementary bipolar ADC driver amplifier products for the cellular base station market.

Semtech   Redondo Beach, CA

- Technical consultant on IBM SiGe 8HP BiCMOS interleaver IC and IBM 32 nm SOI monolithic coherent detection transceiver SOC for 100G coherent optical detection systems. Involved at the architectural level for the SOI interleaver, 8

bit, 64 GSPS ADC, and 8 bit 64 GSPS DAC circuits, and overall system calibration.

- Developed concepts for 10-12 bit, 4-8 GSPS ADC architectures for digital array radar and digital beam-forming applications, as well as high performance sample and hold architecture for military applications.

FBI   Westwood, CA

- Technical consultant on matters of national security. Awarded medal for service to the country.

Nu-Trek Inc.   San Diego, CA

- Developed an RF BIST architecture for characterization of a RF transceiver. Helped the company win Air Force Phase I and Phase II awards.

- Involved with test evaluation of pipeline ADC for cryogenic applications, L1 / L2 band GPS receiver, and Universal Reliability SOC development for lifetime testing of X-Band and L-Band transceivers.

- Responsible for the development of the company's product roadmaps.

- Contributed to SBIR and STTR proposals on nonlinear coupled oscillators for active array applications, active sonar signal processing, high dynamic range ADC, GPS, RFIC transceivers, RIICs, and ROICs. Involved in testing of ADCs for ROICs, and architecture development for RF BIST.

FLIR Electro-Optical Components   Ventura, CA

- Technical lead for the development on ROIC architectures for NASA, Navy, Air Force, MDA, and Army SBIR Phase I and Phase II programs. Development of novel active and passive unit cell architectures.

SYS Technologies / Kratos Defense   San Diego, CA

- Review of SiGe BiCMOS class E power amplifier design to improve reliability of operation. Reviewed circuit, simulation results, test results (dynamic and DC), and performed thermal analysis based on self-heating.

- Review of schematic and layout for small form factor PCB that contains GPS transceiver RFIC and companion digital ASIC. Review of schematic and layout for PLL, IF / baseband test chip evaluation boards. Suggestions for characterization / test debug.

- Review Transmitter and Receiver schematics and block layouts of GPS transceiver IC in IBM 7HP 0.18 μm SiGe BiCMOS for redesign effort. Review of improved receiver IC design.

- Review of test results for the evaluation board and suggestions for characterization and debug. Review of board design and layout revisions for improved electrical and thermal drift performance for successful demo. Help with board yield and manufacturing issues.

Aerius Photonics LLC   Ventura, CA

- Technical lead for STTR Phase I ROIC circuit design partner.

- Developed ROIC architectures for laser vibrometer SBIR Phase I proposal.

LinearChip Inc.   Aliso Viejo, CA

- Developed complete single chip CMOS 802.11 a/b/g/n/ac transceiver architecture, with on-chip T/R switch, for proposal to commercial test equipment house.

- Developed CMOS MSK transmitter for patient temperature monitor and medical equipment tracking ASIC. Developed overall quadrature transmitter architecture, circuit topologies for the DAC, active filter, quadrature mixer, power amplifier, and temperature stabilized reference oscillator. Performed noise / distortion budgets, duty-cycled power calculations for extended battery life, determined PLL phase noise requirements, and defined the circuit block specifications.

Technical lead for the circuit simulations in XFAB XH018 0.18μm CMOS RF process.

- Participating in pursuit of new IC design business. Development of PHEMT TIA gain block concept, satellite receiver / de-multiplexer architecture, CMOS and SiGe RF receiver architectures, and CMOS analog AFE for hand-held controller for telescope, including 16 bit audio DAC architecture. Involved with multiple RFIC proposals for military and commercial applications. Developed multi-channel AM/FM receiver for location positioning application.

- Developed unique TIA / AGC / output amp circuit concept for cable TV over fiber market based on JAZZ 0.18μm SBCH18XL SiGe BiCMOS process.

- Review of battery charger circuit architectures for XFAB XC06 0.6 μm CMOS IC. Architecture suggestions for capacitor charging loop and low battery indicator circuit.

Wistron Corporation   Taipei, Taiwan

- Contributed to discrete quadrature receiver architecture for a new module business proposal to DirectTV.

- Involved with review of existing ODU L-Band module specifications, and application to new digital L-Band module. Contribute to the definition of ASIC requirements and discrete component requirements for new ODU architecture.

Arete Associates   Sherman Oaks, CA

- Phase I and internal IRAD programs for advanced TIA architecture development for high speed laser pulse return processing.

- Review of schematics, simulation results, and layout floor plan, and layout for a 64 channel TIA / OTA wavelength converter in IBM 5HPE 0.5μm SiGe BiCMOS. Function is to receive 1 ns laser pulse and provide linear gain for retransmission. Made suggestions for additional simulations for design robustness and concerns, as well as improved performance based on layout changes. Also made layout suggestions for improved isolation and performance.

- Developing unique 3D FPA and digitally programmable ROIC pixel unit cell architectures for inclusion in STTR proposal.

- Review of 2 TIA input / 128 channel output VCSEL driver, 2 GHz pulsed sampling IC in IBM 7WL 0.18 μm SiGe BiCMOS.

Raytheon Corp.   Dallas, Tx. / El Segundo, CA

- Involved in the development of 40 GSPS ADC architecture in 32 nm IBM SOI.

- Involved in development of on-chip mechanical stress measurement circuit for thermal imaging sensor IC in IBM 9SF 90 nm CMOS process. Submitted patent disclosure on stress sensor circuit. Reviewed the pixel circuit design and the overall ROIC circuitry and timing.

- Participated in winning MDREX proposal effort to AFRL to develop high performance 10 bit, 2.2 GSPS ADC, 14 bit, 3 GSPS DDS, and 1:4 DMUX ICs in IBM 8HP 0.12μm SiGe BiCMOS, and integrate these functions with 8HP receiver and transmitter circuits developed by AFRL, as well as 8HP bias and control circuits developed by Raytheon. Involved with Phase I kick-off meeting.

- Participate in SBIR proposals development with partners Nu-Trek and Crossfield. Developed design methodology for CMOS GPS SOC integration. Developed sub-threshold CMOS RF circuits for low power GPS receiver concept. Generated phase adjust circuit for RF clock distribution for antenna array electronics, and submitted patent disclosure. Contributed write-up on high speed, high performance DAC topologies for DDS proposals. 1 Phase I SBIR proposal awarded.

- Schematic and layout review of IBM 7HP 0.18μm SiGe BiCMOS digital control and bias regulation circuits for MMIC common leg circuit. Reviewed regulator loading problems, solutions, and simulation results. Made simulation recommendations for verification of design robustness. Reviewed metal mask fixes.

- Review of test data, process parameters, and circuit design for production HRL G1.5 2μm InP band-pass Σ-Δ IC for yield enhancement. Developed vendor RFQ for multi-phase IC redesign effort.

- Involved in metal mask effort for 14 bit, 3 GSPS DDS / DAC IC in IBM 7HP 0.18μm SiGe BiCMOS through the Trusted Foundry program. Contributed to design, layout changes in the high speed digital DLL section to improve performance for higher clock applications. Documented circuit design limitations for future redesign for clock rate enhancement.

- Analyzing test data, PCM data for the metal mask DDS chip. Correlate sensitivity of test results to process parameters, and simulation results, to improve yield on future fabrications. Investigate design improvements for possible new mask set. Provide suggestions for performance improvements at the board level. Involved in improvements of the DLL section for next all-layer mask release.

- Member of team analyzing radiation induced latch-up effects in commercially available data converter for space application. Involved in focused laser beam testing to create single events in the converter. Analyzing radiation data, reliability data, and design guides for end-of-life DC power estimates for ICs designed in NS 0.8μm ABIC-IV BiCMOS, MAXIM GST-1 bipolar, IBM 5SF CMOS, and Honeywell HX3000 SOI.

- Review of link budget and block performance for IF and base-band ICs implementing high dynamic range receiver, including IF amp, mixer, VGA / attenuator, and ADC driver amp in IBM 5HPE 0.5μm SiGe BiCMOS. Made architectural suggestions for improved performance. Reviewed test results, and made suggestions for debug.

- Design review of IBM 5HPE 0.5μm SiGe BiCMOS IF receiver ASIC including mixer, gain control amp, and ADC buffer amplifier. Review of measurements for test circuits.

- Jitter analysis for ADC module clock path using divider circuits.

- Design reviews of IBM 5DM 0.5μm SiGe BiCMOS L1 / L2 GPS dual channel receiver IC: LNA1, LNA2, RF amp, RF mixer, IF mixer / AGC, gain calibration loop, baseband amp, PLL, and ADC. Defined layout floor plan, channel layout isolation techniques, and package requirements to meet isolation requirements. Reviewed final GPS receiver layout and developed plan for simulation of layout, package, and external component parasitics. Contributed to correlation of test results. Review of socketed test board layout.

- Review of quad channel IQ detector hybrid design and layout. Made suggestions for debugging of existing hybrid oscillation and improved performance. Review of TI BiCOM-2 0.7μm CBiCMOS IQ IC performance and correlation to hybrid measurement.

- Review of simulations and test results for IBM 8HP 0.12μm SiGe BiCMOS millimeter wave transceiver chipset module performance from outside vendor.

- Review of M/N PLL hybrid design. Review of TI BiCOM-2 0.7 μm CBiCMOS M/N PLL IC performance and correlation to hybrid measurement.

- Performed BOL and EOL noise analysis to estimate the jitter of on-chip clock receiver circuits for the SPT7760 ADC IC based on the MAXIM GST-1 process parameters, and off-chip COTS components for satellite application.

Menara Networks   Irvine, CA

- Reviewed schematics and simulation results for high frequency, multi-GHz active RF low pass filter in JAZZ SBC18HXL 0.18μm SiGe BiCMOS. Involved in top level layout review of first generation EDC IC.

- Contributing to the development of Nyquist 10 GSPS sample / hold circuit, for hold mode feed-through reduction, low distortion, and low power. Contributed to the DC AGC circuit to generate coefficients for Gilbert multiplier as well as developed a new summing circuit for the sampled signals in the analog sampled FIR filter. Involved in solving layout-induced performance problems.

- Involved in the clock distribution architecture and feedback loop to reduce DC offset effects on zero crossing. Review of regulator circuit power-up issues. Created new ADC-based residue architecture to generate the appropriate transfer function for a phase detector circuit for consideration on a higher performance, lower power version of the existing Fiber Optic Receiver IC in JAZZ SBC18HXL 0.18μm SiGe BiCMOS.

- Preliminary review of third party design of 10 Gb/sec CDR PLL schematic blocks for SOC application in STM 0.13μm SiGe BiCMOS. Reviewed metal mask circuit design changes.

MOSIS / ISI   Marina del Rey, CA

- Review of MOSIS website. Provide report consisting of ways to improve technical and business information on the website, as well as customer support. Used client questionnaire to provide additional insight into website, technical information, customer service and support.

Tangea Semiconductor   Manhattan Beach, CA

- Participated in business plan development, facility requirements, engineering manpower requirements, technical concepts, and potential investor meetings.

Technoconcepts Inc. / Terocelo   Van Nuys, CA

- Involved in the design, development, and review of RF receiver and transmitter ICs for multi-band, multi-mode applications using JAZZ SBC18HXL 0.18 μm SiGe BiCMOS. Versions of the Receiver IC include RF VGA, mixer, RZ (Return-to-Zero) and NRZ (non-Return-to-Zero) 6 GSPS 1 bit Σ-Δ ADC, with 2 feedback DAC and 3 feedback DAC versions, PLL, 1:16 DMUX, and base band decimation and filtering. Activities include circuit-level architectures to improve existing performance, schematic and simulation reviews, top level layout floor-planning, layout review, and evaluation board review.

- Involved in testing and correlation of packaged part performance, to simulation, for noise density, harmonic distortion, and intermodulation distortion products. Involved in architecture improvements and enhancements, based on test results, for a metal mask effort. Improvements include extension of VGA architecture to extend the input 1 dB compression point, IIP3, and bandwidth. Added provision to sample very low input frequencies. Improved the dynamic range of the transconductance amplifiers in the modulator. Added dither DAC at the comparator input to improve idle tone performance. Extended the dynamic range of the present RZ Σ-Δ design. Improved the DAC settling and noise response. Added an LNA, and a single-ended to differential converter to interface to the existing VGA.

- Development and layout of test chips for the TSMC 90nm CRN90LP CMOS RF process. Designs include single-ended, wideband and tuned versions of high IIP3 LNA architectures using novel distortion cancellation techniques for operation in the 1- 6 GHz frequency bands. Also developing versions of a 1.8V bidirectional, tri-stated CMOS / LVDS I/O driver with resistive and active back terminations,

and a single input, multi-band, multiple output, switched / tuned RF front end. Involved with CASCADE probing, and correlation to simulation results.

- Development of a wide-band, software defined, multi-band, multi-mode, receiver chip for the TSMC 65nm CRN65GP mixed signal / RF process. Architected the circuits for the wideband LNA with novel AGC and attenuator, the RF DMUX / on-chip RF filter bank, the RF MUX / single-ended-to-differential converter, the quadrature mixer with AGC, RSSI log amp, and the programmable base-band filters. All the RF blocks utilize IM3 cancellation. Target services include AM, FM, DTR, DTV, WiFi, and WiMAX for automotive application for Japanese customer. Involved in the link budget analysis, block specifications, and the requirements for the associated base band ADC and PLLs for the high band LO, low band LO, and ADC LO ICs. Also proposed this architecture for NSF proposal in order to obtain additional development funding.

- Involved in the design, layout, and review of customer demonstration board, based on existing transceiver chipset, for WiMAX applications, using Picochip base-band processor.

- Developing transceiver architecture concepts for multi-service / simultaneous /switched reception off of single multi-band antenna, diversity, and MIMO with self-calibration. Developed low power architecture for multi-service receiver summing into single ADC. Developed transmit / receive architecture for multi-band, multi-mode military radio. Architectures are baseline for new business opportunities.

- Developed IBM 0.12μm 8HP SiGe BiCMOS low power LNA topologies for 10-20 GHz for SBIR proposal. Developed RF interference cancellation architecture for SBIR proposal.

Red Dot Wireless   Milpitas, CA

- Performed transceiver architecture study for TD-SCDMA / EVDO / WiFi / MIMO WiMAX application. Involved in presentations to investors.

Ubidyne   Ulm, Germany

- Schematic, simulation, and layout review of IHP SG25H1 SiGe BiCMOS S1.0 Receiver RFIC. Review of characterization test results.

- Schematic, simulation, and layout review of JAZZ SBCH18XL SiGe BiCMOS S2.0 receiver, transmitter, and PA driver IC designs. Schematic and layout review of Toshiba 90nm CMOS high speed custom digital IC design.

- Review of test data and circuit design for S2.0 receiver to determine yield issues.

Dynamic Research Corporation   San Diego, CA

- Review of existing top level IC issues and proposed packaging approach for GPS transceiver in IBM 7HP 0.18 μm SiGe BiCMOS.

Q3Web Wideband Wireless Inc.   Harbor City, CA

- Constructed white paper on the development of IP libraries in the IBM CMOS and SiGe BiCMOS technologies for use by military contractors. Being submitted to government for funding consideration.

August 2009 – May 2011   Aerius Photonics   Ventura, CA.
Senior Systems Engineer

- Directly responsible for winning new SBIR business for ROIC development. Captured $2.6M of ROIC development money. Have written multiple winning proposals for Army, Navy, MDA, NASA, Air Force, and NSF SBIR Phase I efforts. Have won Navy and ARMY Phase II efforts. Additionally, supported other proposal wins for other technology developments.

- Responsible for the development of new and novel circuit concepts for CMOS and SiGe BiCMOS passive and active imaging ROICs. Have found and engaged ROIC design partnerships. Involved in new business development.
- Have defined ROIC specifications and system requirements in conjunction with BALL Aerospace, Sensor Creations, Raytheon, BAE Systems, Arete and Associates, Tetravue, IDEO, Microvision, Velodyne, and other military and commercial contract partners.
- Technical lead for the conceptual phases of the following ROIC developments: JAZZ SBC35 ROIC for laser vibrometry, ON Semiconductor C5 0.5μm ROIC for 3-D FLASH LADAR for beach zone / surf zone applications, ON Semiconductor C5 0.5μm CMOS ROIC for dual well application (patent pending), JAZZ SBC18 CMOS monolithic imaging ROIC with integrated SiGe APD, and ON Semiconductor 0.18μm CMOS 1920 X 1080 SWIR ROIC.
- Contributed to the development of new laser range finder receiver architecture with unique time programmable gain.
- Developed digitally programmable pixel architecture and specifications for linear direct / coherent detect ROIC for STTR Phase I effort.
- Technical lead in development of single pixel discrete board level customer demo for STTR Phase I LADAR application, and board developments for: 10 Gb/second hexagonal InGaAs detector array, custom ROSA and CDR, 4 X 4 array with fan-out electronics in support of sub-ns laser returns, and new laser range finder receiver.

April 2008- January 2009   Menara Networks   Irvine, CA
Director of ASIC Development

- Involved in simulations of existing Electronic Dispersion Compensation (EDC) IC to correlate to measured performance to define metal mask effort for JAZZ SBC18HXL 0.18μm SiGe BiCMOS IC. Helped define testing for chip characterization.
- Patent application on interleaved FIR with unique sample / hold for extended high dynamic range over previous implementations.
- Contributed to architectural improvements for low power version of EDC IC in IBM 8HP 0.13 μm SiGe BiCMOS.
- Performed simulation trade-off study to compare circuit performance for transmitter application in TSMC CMN65LP 65 nm CMOS, IBM 10LPE 65 nm CMOS, and IBM 8HP 0.12μm SiGe BiCMOS.
- Simulation and design of transmitter pre-driver and output driver for quad 10 Gb/s transceiver with integrated EFEC in IBM 10LPE 65 nm CMOS.
- Simulated low power EML driver concept in IBM 8HP 0.12μm SiGe BiCMOS.
- Involved in the investigation and development of new architectures in support of 100 Gbit/s optical links.
- Review of board schematics and layouts for EDC IC evaluation board, OTN XFP module, and OTN 300 pin module.

February 2002- April 2006   TelASIC Communications   El Segundo, CA
Director of Technology / Founder

- Technical lead for next generation single supply (+5V) data converter ICs in IBM 0.5 μm 5AM SiGe BiCMOS: RF sampling 10 bit, 1 GSPS ADC, on-chip sample / hold, and up-converter IC with integrated 14 bit, 1 GSPS DAC, IF amplifier / mixer. Developed self-heating error correction for quantizer preamp.

- Technical lead for new business pursuits in military and commercial integrated circuits. These included RF handset transceivers, spot BTS, fiber optics, analog transmit cancellation receiver for Gigabit Ethernet, automotive radar, data converters, sample / hold, FPA imaging sensor readout, and arbitrary waveform generators. Technical lead in new business pursuits in board-level DPD-based transceivers based on COTS components. Involved in proposals with Raytheon for DARPA programs, including RHBD (Rad Hard by Design) and Team Phase II.

- Technical advisor for the conception, development, and commercial production of the TC2412 14 bit, 737 MSPS DAC IC and TC1412 14 bit, 250 MSPS ADC IC in IBM 5AM (data sheets available at www.telasic.com/website/products). Architectural contributor to base station transceiver chipset concept. Data converter IC products are being sold to PMC for the NTT DoCoMo base station market. Involved in development of IBIS models of DAC and ADC IC for customer board level simulations.

- Technical contributions to various IC designs including IBM 5AM ADC driver amps, Re-sampler, IBM 7HP test chips, including sample / hold, amplifier, mixer, ring oscillator, and 14 bit, 3 GSPS DDS. IBM 8T chips including re-sampler and 3 bit / 40 GSPS sample / hold / Quantizer / DAC.

- First version of the ADC IC developed, TC1411, received analogZone 2003 Product of the Year Award.

- Involved in business plan development, process to obtain first round of funding.

- Performed technical due diligence on potential new investments for venture fund.

1999– February 2002   Raytheon Advanced Products   El Segundo, CA
Engineering Fellow

- Technical lead for new business pursuits in military / commercial ICs, working with organizations across the company. Programs won include: SIMBAW, TEAM, ADRT, ULTRACOMM, ACN, 3D Flash Ladar image sensor, and APLA.

- Involved in FPA multi-sampling ROIC developments in AMI 0.5μm CMOS: 10 X 10, 64 X 48 arrays. Unit cell development in IBM 0.13 μm CMOS for 256 X 256 array. Developed fan-out concept to maintain small cell pitch while allowing for multi-sampling analog architecture. Evolved multi-sampling concepts for programmable sample time stamp and number of samples.

- Technical advisor for integrated circuit development across Raytheon. This includes design review / debug of existing IC developments.

- Involved in the design and development of data converters, IBM 5HP IF sampling Band-pass Σ-Δ, compact DDS, and RF transceivers for the military and commercial markets. Circuit concepts include fast frequency hopping PLLs, active biquad filters, and a sine weighted DAC.

- Developed Tondelayo 802.11a half duplex transceiver chipset in IBM 5HP for start-up (Systemonic) acquired by Philips. The transceiver demonstrated 802.11a frequency bands in the 5- 6 GHz frequency range using a PCMCIA format.

- Technical contributor to conversion of 0.6μm to 0.5μm NS CMOS for 14 bit, 10 MSPS radiation hard, algorithmic ADC. Involved in design and review process.

- Cooperative effort with LUCENT for next generation design improvements and completed plastic / ceramic package performance evaluation trade-off of CSP1152A CMOS 14 bit, 65 MSPS ADC for Sirius radio application.

- Technical evaluator for BOEING 0.35μm CMOS 1.0625 Gbit/sec Multi-channel Fibre Channel Transceiver for Raytheon AESA application. Contributed to

design reviews, layout reviews, design changes / iterations, suggested simulations to run, and evaluated test results.

- Developed concepts for the integration and packaging of RF MEMS devices with integrated circuits. Circuit architectures included RF front ends with tunable capacitors, tunable RF band-pass and notch filters, as well as active MUX circuits for frequency hopping between filters.

1993–1999   Hughes Communications Products   El Segundo, CA
Senior Staff Engineer / Senior Scientist

- Technical lead of the development ICs for the Digital Receiver Program. This included NS ABIC-IV 0.8μm BiCMOS ICs with the following functions: LNA, mixer, LO driver, DAGC, fractional frequency hopping low phase noise PLL, IF amplifier, video amplifier, serial interface, log detection / blanking, and control logic, and a LUCENT CBIC-V2 summing amplifier IC. Involved in the packaging and test of plastic packaged parts. Digital Receiver board contained 2 chip UHF receiver, single chip GPS receiver IC, and master PLL IC.

- Technical lead for research and development of RF and analog ICs in CMOS, Hughes NB SOS / SOI, silicon (NS ABIC-IV, V, MAXIM SHPi), and IBM SiGe bipolar / BiCMOS process technologies. Functions included LNAs, RF LNA, mixer, VCO, ring oscillator, video amplifier, IF amplifier, sample / hold, high speed 10 bit ECL-to-CMOS translator / latch, 12 bit DAC, and LP Σ-Δ.

- Development of AM / FM LNAs in IC Delco 1.2μm CMOS for automotive radio.

- Involved in the chipset development for NS for the 1.0625 Gbit/sec ANSI X3T11 8B/10B standard using ABIC-IV process. Involved in laser diode driver, TZA, SIPO, PISO, Transceiver ICs.

- Involved with process development / modeling for CMOS, SOS, and silicon / SiGe BiCMOS process technologies.

- Team member of the NS ABIC-IV ADC chip development based on requirements for the ICO satellite system

- Involved in the debug, characterization, and production of hybrids and modules for airborne radar and AMRAAM missile applications.

1991–1993   Radar Systems Group, Hughes Aircraft El Segundo, CA
Staff Engineer

- Lead the IC development of high performance data converter components including sample / hold, summing amplifier, timing generator, band-gap, ADC reference amplifier, video amplifier, DAC, flash quantizers, and buffer amplifier in LUCENT CBIC-U / U2 and MAXIM SHPi and CPi processes.

- Involved in the development of mixer ICs for high dynamic range radar using HRL InP, AlGaAs, and Litton and Hughes D-MESFET technologies.

Fall Semester 1990   Electrophysics Department, USC   Los Angeles, CA
Lecturer

- Taught EE448, Senior Electronics. Generated syllabus, created homework problems, tests, and solutions. Handed out final grades.

1986–1991   Radar Systems Group, Hughes Aircraft El Segundo, CA
Member of Technical Staff

- Involved in the design of components for high performance data converters.

- Contributed to the design of high dynamic range buffer amplifiers, sample / holds, integrators, and gain stages in Hughes 2 μm CBiCMOS, Fairchild 1.25 μm Fast-Z Fineline, and NS Aspect-II, Aspect-III, and ABIC-IV.
- Designed 2 bit adaptive threshold ADC IC in ORBIT 2μm CMOS for EPLRS radio.
- Contributed to architecture for Hughes NB 2 μm CMOS gate array ASIC.
- Involved with process development / modeling for bipolar, complementary bipolar, CMOS, BiCMOS, CBiCMOS.
- Generated analog tile array for the Hughes Carlsbad CBiCMOS process.

July 1985–1986   Radar Systems Group, Hughes Aircraft El Segundo, CA
Member of Technical Staff

- Involved in design of high speed digital ICs for the VHSIC (Very High Speed Integrated Circuit) program using Fairchild Fast-Z Fineline 1.25μm bipolar.
- Involved in design of high speed 64 X 16, 124 X 24, and 1K X 24 SRAM ICs.
- Contributed to the merged junction bipolar SPICE model.
- Designed current mode logic for UHSBL (Ultra High Speed Bipolar Logic) cell library in NS Aspect-III. Cells used in high speed MUX, DMUX, and DDS ICs.
- Developed digital IC architectures for high speed radar signal processing.

Education   1980-1985   UCLA   Westwood, CA

- BS Electrical Engineering Summa Cum Laude, Phi Beta Kappa
- UCLA's Most Outstanding Senior Electrical Engineering Student

1985-1987   UCLA   Westwood, CA

- MS Electrical Engineering

1987-1989   USC   Los Angeles, CA

- Engineer's Degree Electrical Engineering

1990-Present   USC   Los Angeles, CA

- PHD Candidate under the advisement of Prof. John Choma Jr.
- Completed Thesis: "Nonlinear Error Correction for the Bipolar Canonic Cells."
- Designed, fabricated, and DC wafer probed amplifier circuits in MAXIM SHPi bipolar process to verify theory developed.

Publications

- M. Chambers and L. Linder, "A Precision Monolithic Sample- And-Hold for Video Analog-to-Digital Converters," ISSCC Feb. 1991.
- B. Felder, et al., "A Low Noise 13 Bit 10 MSPS ADC Hybrid with High Dynamic Range," GOMAC 1994.
- W. Cheng, et al., "A 3 Bit, 40GSPS ADC- DAC in 0.12μm SiGe," ISSCC Feb. 2004.
- O. Panfilov, et al., "Direct Conversion Transceivers as a Promising Solution for Building Future Ad-hoc Networks," International Conference on Next Generation Tele-traffic and Wired / Wireless Advanced Networking September 2007.
- O. Panfilov, et al., "Test Results of the Direct Conversion Transceiver Demo Board", November 2007 SDR Forum Technical Conference.

- O. Panfilov, et al., "Overcoming Challenges of Direct Conversion Software Radio," IEEE International Design and Test Workshop December 2007.
- A. Varghese and L.F. Linder, "Software Defined Radios for Wireless Handsets," April 2008 Wireless Design & Development Magazine.
- S. Elahmadi, et al., "A Monolithic One-Sample / Bit Partial-Response Maximum Likelihood SiGe Receiver for Electronic Dispersion Compensation of 10.7 GB / s Fiber Channels," OFC / NFOEC March 2009.
- S. Elahmadi, et al., "A 50 dB Dynamic Range, 11.3 GSPS, Programmable Finite Impulse Response (FIR) Equalizer in 0.18μm SiGe BiCMOS Technology for High Speed Electronic Dispersion Compensation (EDC) Applications," RFIC Symposium, June 2009.
- J. Edwards, et al., "A 12.5 Gbps Analog timing Recovery System for PRML Optical Receivers," RFIC Symposium, June 2009.
- D. Baranauskas, et al., "A 6th Order 1.6 to 3.2 GHz Tunable Low-Pass Linear Phase gm-C Filter for Fiber Optic Adaptive EDC Receivers," RFIC Symposium, June 2009.
- S. Elahmadi, et al., "An Analog PRML Receiver for up to 400km of Uncompensated OC-192 Fiber-Optic Channels," ESSCIRC September 2009.
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- Montierth, D., Strans, T., Leatham, J., Linder, L., and Baker, R. J., "Performance and Characteristics of Silicon Avalanche Photo detectors in the C5 Process," 2012 IEEE Midwest Symposium on Circuits and Systems, Boise, Idaho.
- Rauch M. and Linder L., "Collaborating with Nu-Trek," 2012 HiRev Industry Day, December 2012, Los Angeles, California.

Awards / Achievements
- IEEE Senior Member
- Two-time Hughes Aircraft Division Patent Award winner
- 55 issued US patents, over 300 international patents, several US patents pending
- Numerous IC design team awards at Hughes and Raytheon
- Hughes Masters Fellow, Engineers Fellow, Doctoral Fellow
- 2008 IEEE San Fernando Valley Section Entrepreneurial Business Plan Competition Judge
- Menara Networks EDC IC Team Award – world's first error free operation over 400 km of uncompensated fiber

IC Process Experience
- CMOS, silicon / SiGe bipolar, silicon / SiGe BiCMOS, complementary bipolar, CBiCMOS, SOI, SOS, GaAs D-mode / E-mode MESFET, AlGaAs / InP HBT

Skills
- CADENCE Analog Artist Schematic Composer, Spectre Simulator

Security Clearance
- Secret clearance is presently supported by Nu-Trek.
- US Citizen