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**IN THE UNITED STATES DISTRICT COURT
FOR THE SOUTHERN DISTRICT OF CALIFORNIA**

21 BELL SEMICONDUCTOR, LLC,
22
23 Plaintiff,
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25 v.
26 MAXLINEAR, INC.,
27
28 Defendant.

Case No. '22CV1178 BAS BLM

**COMPLAINT
DEMAND FOR JURY TRIAL**

1 Plaintiff Bell Semiconductor, LLC (“Bell Semic” or “Plaintiff”) brings this
2 Complaint against Defendant MaxLinear, Inc. (“MaxLinear”) for infringement of U.S.
3 Patent No. 7,007,259 (“the ’259 patent”). Plaintiff, on personal knowledge of its own
4 acts, and on information and belief as to all others based on investigation, alleges as
5 follows:

6 **SUMMARY OF THE ACTION**

7 1. This is a patent infringement suit relating to MaxLinear’s unauthorized
8 and unlicensed use of the ’259 patent. The circuit design methodology claimed in the
9 ’259 patent is used by MaxLinear in the production of one or more of its devices,
10 including its XR9240 Compression and Security Coprocessor (“XR9240
11 Coprocessor”).

12 2. Semiconductor devices include different kinds of materials to function as
13 intended. For example, these devices typically include both metal (i.e., conductor) and
14 insulator materials, which are deposited or otherwise processed sequentially in layers
15 to form the final device. These layers—and the interconnects and components formed
16 within them—have gotten much smaller over time, increasing the performance of
17 these devices dramatically. As a result, it has become even more important to keep the
18 layers planar as the device is being built because defects and warpage can cause
19 fabrication issues and malfunctioning of the device. Manufacturers use a process
20 called Chemical Mechanical Planarization/Polishing (“CMP”) to smooth out the
21 surface of the device periodically between deposition and/or etching of each layer.
22 This allows subsequent layers to be built and connected more easily with fewer
23 opportunities for short circuits or other errors that render the device defective. CMP
24 functions best when there is a certain density and variance of the same material on the
25 surface of the chip. This is because different materials will be “polished” away at
26 different rates, leading to erosion or dishing on the surface. To reduce this problem
27 “dummy” material, also known as “dummy fill,” is typically inserted into low-density
28 regions of the device to increase the overall uniformity of the structures on the surface

1 of the layer and reduce the density variability across the surface of the device.
2 However, dummy fill can increase capacitance if it is placed too close to signal wires,
3 which slows the transmission speed of signals and degrades the overall performance
4 of the device.

5 3. Prior to development of the methodology described in the '259 patent,
6 the most widely implemented technology for insertion of dummy metal into a circuit
7 design required hardcoding a large “stay-away” distance between the dummy metal
8 and clock nets, which led to less space available for dummy metal insertion. This
9 methodology often made it impossible to insert enough dummy metal to meet the
10 required minimum density. The traditional dummy fill tools would often complete
11 their run without reaching the minimum density, thus requiring at least a second run of
12 the tool for the problem areas. In each problem area, the “stay-away” distance was
13 reduced manually. And if there was more than one problem area, the manufacturer
14 would have to make multiple runs of the tool, as it would have to address one problem
15 area at a time. This was an involved, iterative process that had the potential to
16 negatively impact the fabrication schedule and potentially the yield of the run, causing
17 costs to go up.

18 4. Vikram Shrowty and Santhanakrishnan Raman (“the Inventors”), the
19 inventors of the '259 patent, understood the drawbacks of this “stay-away” design
20 process and set out to develop a more efficient method for inserting dummy metal into
21 a circuit design. The Inventors ultimately conceived of a dummy fill procedure that
22 minimizes the negative timing impact of dummy metal on clock nets, while still
23 achieving minimum density in a single run. The claimed invention begins by
24 identifying free spaces on each layer of the circuit design suitable for dummy metal
25 insertion as dummy regions. The dummy regions are then prioritized such that the
26 dummy regions located adjacent to clock nets are filled with dummy metal last,
27 thereby minimizing any timing impact on the clock nets.
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1 5. The inventions disclosed in the '259 patent provide many advantages
2 over the prior art. In particular, they provide a simple and efficient method for dummy
3 metal insertion that minimizes the timing impact to clock nets and at the same time
4 guarantees reaching minimum density in a single pass. *See* Ex. A at 6:11–15. As
5 mentioned above, the patented invention results in the dummy regions being
6 prioritized such that the dummy regions located adjacent to clock nets are filled with
7 dummy metal last, thereby minimizing the timing impact on the clock nets. *See* Ex. A
8 at 2:29–47. Additionally, some embodiments of the patented invention further
9 prioritize the dummy regions such that the dummy regions adjacent to wider clock
10 nets are filled with dummy metal after dummy regions that are located adjacent to
11 narrower clock nets. *See* Ex. A at 2:35–39. These significant advantages are achieved
12 through the use of the patented inventions and thus the '259 patent presents significant
13 commercial value for companies like MaxLinear.

14 6. Bell Semic brings this action to put a stop to MaxLinear's unauthorized
15 and unlicensed use of the inventions claimed in the '259 patent.

THE PARTIES

17 7. Plaintiff Bell Semic is a limited liability company organized under the
18 laws of the State of Delaware with a place of business at One West Broad Street, Suite
19 901, Bethlehem, PA 18018.

20 8. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs
21 sprung out of the Bell System as a research and development laboratory, and
22 eventually became known as one of America's greatest technology incubators. Bell
23 Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was
24 widely considered one of the most important technological breakthroughs of the time,
25 earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial
26 transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its
27 transistor patents to companies throughout the world, creating a technological boom
28

1 that led to the use of transistors in the semiconductor devices prevalent in most
2 electronic devices today.

3 9. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900
4 worldwide patents and applications, approximately 1,500 of which are active United
5 States patents. This patent portfolio of semiconductor-related inventions was
6 developed over many years by some of the world's leading semiconductor companies,
7 including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI
8 Corporation ("LSI"). This portfolio reflects technology that underlies many important
9 innovations in the development of semiconductors and integrated circuits for high-
10 tech products, including smartphones, computers, wearables, digital signal processors,
11 IoT devices, automobiles, broadband carrier access, switches, network processors, and
12 wireless connectors.

13 10. The principals of Bell Semic all worked at Bell Labs' Allentown facility,
14 and have continued the rich tradition of innovating, licensing, and helping the industry
15 at large since those early days at Bell Labs. For example, Bell Semic's CTO was a LSI
16 Fellow and Broadcom Fellow. He is known throughout the world as an innovator with
17 more than 300 patents to his name, and he has a sterling reputation for helping
18 semiconductor labs improve their efficiency. Bell Semic's CEO took a brief hiatus
19 from the semiconductor world to work with Nortel Networks in the telecom industry
20 during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel
21 retirees and employees. In addition, several Bell Semic executives previously served
22 as engineers at many of these companies and were personally involved in creating the
23 ideas claimed throughout Bell Semic's extensive patent portfolio.

24 11. On information and belief, MaxLinear has its headquarters and regular,
25 established place of business in this District at: 5966 La Place Court, Suite 100,
26 Carlsbad, California 92008. On information and belief, MaxLinear develops, designs,
27 and/or manufactures products in the United States, including in this District, according
28 to the '259 patented process/methodology; and/or uses the '259 patented

1 process/methodology in the United States, including in this District, to make products;
2 and/or distributes, markets, sells, or offers to sell in the United States and/or imports
3 products into the United States, including in this District, that were manufactured or
4 otherwise produced using the patented process. Additionally, MaxLinear introduces
5 those products into the stream of commerce knowing that they will be sold and/or
6 used in this District and elsewhere in the United States.

7 **JURISDICTION AND VENUE**

8 12. This is an action for patent infringement arising under the Patent Laws of
9 the United States, Title 35 of the United States Code. Accordingly, this Court has
10 subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

11 13. This Court has personal jurisdiction over MaxLinear under the laws of
12 the State of California, due at least to its substantial business in California and in this
13 District. MaxLinear has purposefully and voluntarily availed itself of the privileges of
14 conducting business in the United States, in the State of California, and in this District
15 by continuously and systematically placing goods into the stream of commerce
16 through an established distribution channel with the expectation that they will be
17 purchased by consumers in this District. In the State of California and in this District,
18 MaxLinear, directly or through intermediaries: (i) performs at least a portion of the
19 infringements alleged herein; (ii) develops, designs, and/or manufactures products
20 according to the '259 patented process/methodology; (iii) distributes, markets, sells, or
21 offers to sell products formed according to the '259 patented process/methodology;
22 and/or (iv) imports products formed according to the '259 patented
23 process/methodology.

24 14. On information and belief, venue is proper in this Court pursuant to 28
25 U.S.C. §§ 1391 and 1400 because MaxLinear has committed, and continues to
26 commit, acts of infringement in this District and has a regular and established place of
27 business in this District. For example, MaxLinear maintains its headquarters and
28 regular, established place of business at: 5966 La Place Court, Suite 100, Carlsbad,

1 California 92008—a 45,000 square-foot facility containing labs and engineering
2 operations. *See MaxLinear Moving to Larger Headquarters in Carlsbad*, San Diego
3 Business Journal (available at: [https://www.sdbj.com/news/2013/dec/30/maxlinear-](https://www.sdbj.com/news/2013/dec/30/maxlinear-moving-larger-headquarters-carlsbad/)
4 [moving-larger-headquarters-carlsbad/](https://www.sdbj.com/news/2013/dec/30/maxlinear-moving-larger-headquarters-carlsbad/)) (last visited May 26, 2022).

5 15. Currently, MaxLinear employs more than 55 engineers in this District,
6 including a Principal Engineer, Senior Engineer, Principal ASIC Engineer, Senior
7 ASIC Engineer, Senior Staff Engineer, RF/MS IC Design Engineer and Senior IC
8 Packaging Engineer, among others. *See Current Positions, LinkedIn* (available at:
9 [https://www.linkedin.com/search/results/people/?currentCompany=%5B%2247129%](https://www.linkedin.com/search/results/people/?currentCompany=%5B%2247129%22%5D&geoUrn=%5B%22102095887%22%5D&keywords=engineer&origin=FACE)
10 [22%5D&geoUrn=%5B%22102095887%22%5D&keywords=engineer&origin=FACE](https://www.linkedin.com/search/results/people/?currentCompany=%5B%2247129%22%5D&geoUrn=%5B%22102095887%22%5D&keywords=engineer&origin=FACE)
11 [TED_SEARCH&sid=cM%3B&title=engineer](https://www.linkedin.com/search/results/people/?currentCompany=%5B%2247129%22%5D&geoUrn=%5B%22102095887%22%5D&keywords=engineer&origin=FACE)) (last visited May 26, 2022). In
12 addition, MaxLinear is advertising nearly 10 engineer positions in this District. *See*
13 *Job Openings, LinkedIn* (available at: https://www.linkedin.com/jobs/search/?f_C
14 [=47129&keywords=engineer](https://www.linkedin.com/jobs/search/?f_C)) (last visited May 26, 2022). These positions include
15 those that relate to the '259 patented technology, such as a Senior Systems
16 Engineering Manager, Digital Automation Engineer, Staff Packaging Engineer, and
17 Principal RF/MS IC Design Engineer, among others. *Id.*

18 16. Venue is also convenient in this District. This is at least true because of
19 this District's close ties to this case—including the technology, relevant witnesses,
20 and sources of proof noted above—and its ability to quickly and efficiently move this
21 case to resolution.

22 17. On information and belief, Bell Semic's cause of action arises directly
23 from MaxLinear's circuit design work and other activities in this District. Moreover,
24 on information and belief, MaxLinear has derived substantial revenues from its
25 infringing acts occurring within the State of California and within this District.

26 **U.S. PATENT NO. 7,007,259**

27 18. Bell Semic is the owner by assignment of the '259 patent. The '259
28 patent is titled "Method for Providing Clock-Net Aware Dummy Metal Using Dummy

1 Regions.” The ’259 patent issued on February 28, 2006. A true and correct copy of the
2 ’259 patent is attached as Exhibit A.

3 19. The inventors of the ’259 patent are Vikram Shrowty and
4 Santhanakrishnan Raman.

5 20. The application that resulted in the issuance of the ’259 patent was filed
6 on July 31, 2003. The ’259 patent claims priority to July 31, 2003.

7 21. The ’259 patent generally relates to “methods for patterning dummy
8 metal to achieve planarity for chemical-mechanical polishing of integrated circuits,
9 and more particularly to a dummy fill software tool that provides clock-net aware
10 dummy metal using dummy regions.” Ex. A at 1:7–11.

11 22. The background section of the ’259 patent identifies the shortcomings of
12 the prior art. More specifically, the specification describes that the prior circuit design
13 methodology was disadvantageous because it was “often impossible to insert enough
14 dummy metal into a tile to meet the required minimum density without reducing the
15 large dummy-to-clock distance.” Ex. A at 2:3–10. Use of this design process meant
16 that a second run of the metal-fill tool was often required in order to meet the density
17 requirements for all of the tiles. Ex. A at 2:10–14. Having to rerun the tool to meet the
18 density requirements made the design process an “involved, iterative process[,]”
19 which could “significantly impact the design schedule.” Ex. A at 2:14–18.

20 23. In light of the drawbacks of the prior art, the Inventors recognized the
21 need to “minimize[] the negative timing impact of dummy metal on clock nets, while
22 at the same time achieving minimum density in a single run.” Ex. A at 2:19–23. The
23 inventions claimed in the ’259 patent addresses this need.

24 24. The ’259 patent contains three independent claims and 37 total claims,
25 covering a method and computer readable medium for circuit design. Claim 1 reads:

26 1. A method for inserting dummy metal into a circuit design, the
27 circuit design including a plurality of objects and clock nets, the method
28 comprising:

- 1 (a) identifying free spaces on each layer of the circuit design
- 2 suitable for dummy metal insertion as dummy regions, and
- 3 (b) prioritizing the dummy regions such that the dummy regions
- 4 located adjacent to clock nets are filled with dummy metal last,
- 5 thereby minimizing any timing impact on the clock nets.

6 25. This claim, as a whole, provides significant benefits and improvements to
7 the function of the semiconductor device, *e.g.*, minimizing the negative timing impact
8 of dummy metal on clock nets while also reducing the opportunity for dishing and
9 erosion that could result in inaccurate transfer of patterns during lithography,
10 suboptimal layouts/designs, inaccurate timing, reduced signal integrity, crosstalk
11 delay, noise issues, increased probability of failure, and ultimately defective or
12 underperforming devices. *See, e.g.*, Ex. A at 6:11–15.

13 26. The claims of the '259 patent also recite inventive concepts that improve
14 the functioning of the fabrication process, particularly as to dummy filling. The
15 claims of the '259 patent disclose a new and novel solution to specific problems
16 related to improving semiconductor fabrication. As explained in detail above and in
17 the '259 patent specification, the claimed inventions improve upon the prior art
18 processes by prioritizing dummy regions such that the dummy regions located
19 adjacent to clock nets are filled with dummy metal last. This has the advantage of
20 reducing the impact of dummy metal on signal and clock lines and increasing the
21 efficiency, yield, and design/layout miniaturization and flexibility of the
22 manufacturing process. The claimed inventive processes also increase performance
23 and signal integrity, while reducing crosstalk delay, noise issues, probability of
24 failure, and defective and/or underperforming devices.

25 **COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,007,259**

26 27. Bell Semic re-alleges and incorporates by reference the allegations of the
27 foregoing paragraphs as if fully set forth herein.

28

1 28. The '259 patent is valid and enforceable under the United States Patent
2 Laws.

3 29. Bell Semic owns, by assignment, all right, title, and interest in and to the
4 '259 patent, including the right to collect for past damages.

5 30. A copy of the '259 patent is attached at Exhibit A.

6 31. On information and belief, MaxLinear has and continues to directly
7 infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the '259 patent by
8 using the patented methodology to design one or more semiconductor devices,
9 including as one example the XR9240 Coprocessor, in the United States.

10 32. On information and belief, MaxLinear employs a variety of design tools,
11 for example, Cadence, Synopsys, and/or Siemens tools, to insert dummy metal into a
12 circuit design (the "Accused Processes") as recited in the '259 patent claims. As one
13 example, MaxLinear's Accused Processes perform a method for inserting dummy
14 metal into a circuit design, where the circuit design includes a plurality of objects and
15 clock nets as required by claim 1 of the '259 patent. MaxLinear does so by
16 employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens
17 tool, to insert dummy metal into a circuit design for its XR9240 Coprocessor. The
18 XR9240 Coprocessor's design include a plurality of objects, such as cells,
19 interconnects, signal nets, and clock nets.

20 33. MaxLinear's Accused Processes also identify free spaces on each layer
21 of the circuit design suitable for dummy metal insertion as dummy regions.
22 MaxLinear does so by employing a design tool, such as at least one of the Cadence,
23 Synopsys, and/or Siemens tools, to identify free spaces on each layer of its XR9240
24 Coprocessor's circuit designs suitable for dummy metal insertion as dummy regions.

25 34. MaxLinear's Accused Processes also prioritize the dummy regions such
26 that the dummy regions located adjacent to clock nets are filled with dummy metal
27 last, thereby minimizing any timing impact on the clock nets. MaxLinear does so by
28 employing a design tool, such as at least one of the Cadence, Synopsys, and/or

1 Siemens tools, to prioritize dummy regions such that those adjacent to clock nets are
2 filled with dummy metal last. For example, the Accused Processes assign a “high
3 cost” to adding metal fill near the clock nets and “lower cost” to adding metal fill
4 near signal, power, and ground nets. Assigning “cost” in this way fills dummy
5 regions adjacent to clock nets last and minimizes any timing impact on the clock nets.
6 An exemplary infringement analysis showing infringement of one or more claims of
7 the ’259 patent is set forth in Exhibit B. The declaration of Lloyd Linder, an expert in
8 the field of semiconductor device design, is attached at Exhibit C and further
9 describes MaxLinear’s infringement of the ’259 patent.

10 35. MaxLinear’s Accused Processes infringe and continue to infringe one or
11 more claims of the ’259 patent during the pendency of the ’259 patent.

12 36. On information and belief, MaxLinear has and continues to infringe
13 pursuant to 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the
14 doctrine of equivalents, by using the Accused Processes in violation of one or more
15 claims of the ’259 patent. MaxLinear has and continues to infringe pursuant to 35
16 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of
17 equivalents, by making, selling, or offering to sell in the United States, or importing
18 into the United States products manufactured or otherwise produced using the
19 Accused Processes in violation of one or more claims of the ’259 patent.

20 37. MaxLinear’s infringement of the ’259 patent is exceptional and entitles
21 Bell Semic to attorneys’ fees and costs incurred in prosecuting this action under 35
22 U.S.C. § 285.

23 38. Bell Semic has been damaged by MaxLinear’s infringement of the ’259
24 patent and will continue to be damaged unless MaxLinear is enjoined by this Court.
25 Bell Semic has suffered and continues to suffer irreparable injury for which there is
26 no adequate remedy at law. The balance of hardships favors Bell Semic, and public
27 interest is not disserved by an injunction.
28

1 39. Bell Semic is entitled to recover from MaxLinear all damages that Bell
2 Semic has sustained as a result of MaxLinear's infringement of the '259 patent,
3 including without limitation and/or not less than a reasonable royalty.

4 **PRAYER FOR RELIEF**

5 WHEREFORE, Bell Semic respectfully requests that this Court enter judgment
6 in its favor as follows and award Bell Semic the following relief:

- 7 (a) a judgment declaring that MaxLinear has infringed one or more claims of
8 the '259 patent in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;
- 9 (b) an award of damages adequate to compensate Bell Semic for
10 infringement of the '259 patent by MaxLinear, in an amount to be proven
11 at trial, including supplemental post-verdict damages until such time as
12 MaxLinear ceases its infringing conduct;
- 13 (c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting
14 MaxLinear and its officers, directors, employees, agents, consultants,
15 contractors, suppliers, distributors, all affiliated entities, and all others
16 acting in privity with MaxLinear, from committing further acts of
17 infringement;
- 18 (d) a judgment requiring MaxLinear to make an accounting of damages
19 resulting from MaxLinear's infringement of the '259 patent;
- 20 (e) the costs of this action, as well as attorneys' fees as provided by 35
21 U.S.C. § 285;
- 22 (f) pre-judgment and post-judgment interest at the maximum amount
23 permitted by law;
- 24 (g) all other relief, in law or equity, to which Bell Semic is entitled.

25 **DEMAND FOR JURY TRIAL**

26 Plaintiff hereby demands a jury trial for all issues so triable.
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1 Dated: August 11, 2022

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DEMAND FOR JURY TRIAL

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Plaintiff hereby demands a jury trial for all issues so triable.

Dated: August 11, 2022

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Exhibits:

- Exhibit A: 259 patent
- Exhibit B: Claim chart for claims 1-37 of the 259 patent
- Exhibit C: Expert declaration