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16 **Pro Hac Applications forthcoming*

17 Attorneys for Plaintiff

18 **IN THE UNITED STATES DISTRICT COURT**
19 **FOR THE SOUTHERN DISTRICT OF CALIFORNIA**

20 BELL SEMICONDUCTOR, LLC,

21 Plaintiff,

22 v.

23 NXP USA, INC.,

24 Defendant.
25

Case No. '22CV1267 BEN BGS

ORIGINAL COMPLAINT

JURY TRIAL DEMANDED

1 Plaintiff Bell Semiconductor, LLC (“Bell Semic” or “Plaintiff”) brings this
2 Complaint Defendant NXP USA, Inc. (“NXP”) for infringement of U.S. Patent Nos.
3 7,149,989 (“the ’989 patent”) and 7,260,803 (“the ’803 patent”) (collectively the
4 “Lakshmanan patents”). Plaintiff, on personal knowledge of its own acts, and on
5 information and belief as to all others based on investigation, alleges as follows:

6 **SUMMARY OF THE ACTION**

7 1. This is a patent infringement suit relating to NXP’s unauthorized and
8 unlicensed use of the Lakshmanan patents. The metal design and insertion technologies
9 claimed in the Lakshmanan patents are used by NXP in the production of one or more
10 of its semiconductor chips, including its NXP LS1043A Quad-Core Networking
11 Processor.

12 2. Semiconductor devices include different kinds of materials to function as
13 intended. For example, these devices typically include both metal (*i.e.*, conductor) and
14 insulator materials, which are deposited or otherwise processed sequentially in layers
15 to form the final device. These layers—and the interconnects and components formed
16 within them—have gotten much smaller over time, increasing the performance of these
17 devices dramatically. These devices have also become exceedingly more complex with
18 increasing numbers of layers and increasingly smaller device features, all to enable
19 increasingly faster devices operating at higher clock speeds. As a result, it has become
20 more important to reduce the chance of short circuits and to keep the layers planar as
21 the device is being built because defects and warpage can cause fabrication issues and
22 malfunctioning of the device. Manufacturers use a process called Chemical Mechanical
23 Planarization/Polishing (“CMP”) to smooth out the surface of the device periodically
24 between deposition and/or etching of each layer. This allows subsequent layers to be
25 built and connected more easily with fewer opportunities for short circuits or other
26 errors that render the device defective. CMP functions best when there is a certain
27 density and variance of the same material on the surface of the chip. This is because

1 different materials will be “polished” away at different rates, leading to erosion or
2 dishing on the surface. To reduce this problem, “dummy” interconnect material, also
3 known as “dummy fill,” is typically inserted into low-density regions of the device to
4 increase the overall uniformity of the structures on the surface of the layer and reduce
5 the density variability across the surface of the device. Dummy fill is typically inserted
6 by a dummy fill tool, which checks the metal density of the device and places dummy
7 metal into regions that do not meet the metal density needed to minimize the likelihood
8 that CMP processes causes the device to malfunction.

9 3. Prior to development of the methodology described in the ’803 patent, if a
10 designer requested even a small change to a semiconductor device, the dummy fill
11 pattern must be thrown out. This is problematic because it can take up to 30 hours to
12 run the dummy fill tool to create the dummy fill pattern. By starting over, the entire
13 device design layout could be delayed by 30 hours or more. This issue is exacerbated
14 with every subsequent change that again causes the dummy fill process to begin again
15 from scratch. Such an iterative, time-consuming process negatively impacts the
16 fabrication schedule and causes costs to go up.

17 4. Viswanathan Lakshmanan, Richard Blinne, Vikram Shrowty, and Lena
18 Montecillio (“the ’803 Inventors”), the inventors of the ’803 patent, understood the
19 drawbacks of this process and set out to develop a more efficient method for inserting
20 dummy metal into a circuit design after portion(s) of it have changed. The ’803
21 Inventors ultimately conceived of a dummy fill insertion procedure that did not require
22 having to rerun the dummy fill tool whenever any change was made to the layout. The
23 claimed invention, after a portion of the design data has changed, first performs a check
24 to determining whether any dummy metal objects intersect with any other objects in
25 the design data. Then any intersecting dummy metal objects are deleted from the design
26 data, thereby avoiding having to rerun the dummy fill tool.

1 5. The inventions disclosed in the '803 patent provide many advantages over
2 the prior art. In particular, they provide a simple and efficient method for ensuring
3 dummy metal does not intersect other components such that the dummy fill tool does
4 not have to be rerun. *See* Ex. A at 2:6–22. As mentioned above, this is very beneficial
5 as it substantially reduces the run time of the dummy fill tool, shortens the overall
6 design timeline, and avoids cost overruns and delays, making it less costly to make
7 changes later in the design process. *See* Ex. A at 1:51–65. Given the aforementioned
8 increased complexity of circuit designs and the corresponding delays from ECOs and
9 layout changes, these efficiency gains have become more and more important in
10 completing the design process without affecting time-to-market. These significant
11 advantages are achieved through the use of the patented inventions and thus the '803
12 patent presents significant commercial value for companies like NXP.

13 6. The '989 patent addresses another way to minimize short circuits and
14 malfunctioning devices. When creating a semiconductor device, designers typically
15 create layout designs that contain the topological information used to identify structures
16 within several layers of the semiconductor device. These layout designs are ultimately
17 used as blueprints to create the physical semiconductor device. Prior to development of
18 the methodology described in the '989 patent, the designs would be validated at the
19 very end of the design cycle, when all components have been placed and routed.
20 However, if the validation process detects a design fault, like a short circuit, at the very
21 end of the design cycle, then the timing of the entire integrated circuit design may have
22 to be reset. In some cases, the design may have to be re-floorplanned and the entire
23 design cycle may have to be reiterated, causing delays on of several weeks or months,
24 depending on the overall complexity of the design and the process node. Similarly, it is
25 not possible to simply run the validation check early in the process to avoid this issue.
26 Doing so would cause the validation process to incorrectly identify a large number of
27 errors because the circuit design is incomplete in early stages.

1 7. Viswanathan Lakshmanan, Alan Holesovsky, Lisa Miller, and Jonathan
2 Kuppinger (“the ’989 Inventors”), the inventors of the ’989 patent, understood the
3 drawbacks of both late stage and early stage validation processes and decided to create
4 something better. The ’989 Inventors ultimately conceived of a validation procedure
5 that specifies validation checks on certain physical design rules that are specific to
6 texted metal short circuits between different signal sources in addition to power and
7 ground. The claimed invention receives a representation of an integrated circuit design
8 and a physical design rule deck that specifies rule checks to be performed on the
9 integrated circuit design. The claimed invention generates a specific rule deck from the
10 physical design rule deck, where the specific rule deck is a subset that includes only
11 physical design rules that are specific to texted metal short circuits between different
12 signal sources in addition to power and ground in the integrated circuit design. A
13 physical design validation is performed on the integrated circuit design from the
14 specific rule deck to identify texted metal short circuits between different signal sources
15 in addition to power and ground in the integrated circuit design.

16 8. The inventions disclosed in the ’989 patent provide many advantages over
17 the prior art. In particular, they provide the ability to perform an early validation process
18 that does not falsely identify a number of unfounded errors in the early stage of the
19 design. *See* Ex. B at 2:47–58. For instance, in early stages, the patented process can
20 identify violations in floorplanning, texted metal shorts, and errors in power map
21 structure. *See* Ex. B at 2:64–3:7. Early defect detection saves computer processing time,
22 avoids severe voltage droop, and allows for correction in early stages, each of which
23 would otherwise result in costly schedule delays and unacceptable turnaround time. *See*
24 Ex. B at 3:7–20. Moreover, this allows high-level power and signal-routing such that
25 individual blocks with defined pins can be finalized by the responsible members of
26 design team in parallel, at substantial decrease in design time and overall gains in
27 efficiency. These significant advantages are achieved through the use of the patented
28

1 inventions and thus the '989 patent presents significant commercial value for
2 companies like NXP.

3 9. Bell Semic brings this action to put a stop to NXP's unauthorized and
4 unlicensed use of the inventions claimed in the Lakshmanan patents.

5 **THE PARTIES**

6 10. Plaintiff Bell Semic is a limited liability company organized under the
7 laws of the State of Delaware with a place of business at One West Broad Street, Suite
8 901, Bethlehem, PA 18018.

9 11. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs
10 sprung out of the Bell System as a research and development laboratory, and eventually
11 became known as one of America's greatest technology incubators. Bell Labs
12 employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely
13 considered one of the most important technological breakthroughs of the time, earning
14 the inventors the Nobel Prize in Physics. Bell Labs made the first commercial
15 transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its
16 transistor patents to companies throughout the world, creating a technological boom
17 that led to the use of transistors in the semiconductor devices prevalent in most
18 electronic devices today.

19 12. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900
20 worldwide patents and applications, approximately 1,500 of which are active United
21 States patents. This patent portfolio of semiconductor-related inventions was
22 developed over many years by some of the world's leading semiconductor companies,
23 including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI
24 Corporation ("LSI"). This portfolio reflects technology that underlies many important
25 innovations in the development of semiconductors and integrated circuits for high-tech
26 products, including smartphones, computers, wearables, digital signal processors, IoT
27

1 devices, automobiles, broadband carrier access, switches, network processors, and
2 wireless connectors.

3 13. The principals of Bell Semic all worked at Bell Labs' Allentown facility,
4 and have continued the rich tradition of innovating, licensing, and helping the industry
5 at large since those early days at Bell Labs. For example, Bell Semic's CTO was an LSI
6 Fellow and Broadcom Fellow. He is known throughout the world as an innovator with
7 more than 300 patents to his name, and he has a sterling reputation for helping
8 semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from
9 the semiconductor world to work with Nortel Networks in the telecom industry during
10 its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees
11 and employees. In addition, several Bell Semic executives previously served as
12 engineers at many of these companies and were personally involved in creating the
13 ideas claimed throughout Bell Semic's extensive patent portfolio.

14 14. On information and belief, NXP has a place of business in this District at
15 Innovation Drive, Suite 150, San Diego, CA 92128. On information and belief, NXP
16 develops, designs, and/or manufactures products in the United States, including in this
17 District, according to the Lakshmanan patented process/methodology; and/or uses the
18 Lakshmanan patented process/methodology in the United States, including in this
19 District, to make products; and/or distributes, markets, sells, or offers to sell in the
20 United States and/or imports products into the United States, including in this District,
21 that were manufactured or otherwise produced using the patented process. Additionally,
22 NXP introduces those products into the stream of commerce knowing that they will be
23 sold and/or used in this District and elsewhere in the United States.

24 **JURISDICTION AND VENUE**

25 15. This is an action for patent infringement arising under the Patent Laws of
26 the United States, Title 35 of the United States Code. Accordingly, this Court has
27 subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

1 16. This Court has personal jurisdiction over NXP under the laws of the State
2 of California, due at least to its substantial business in California and in this District.
3 NXP has purposefully and voluntarily availed itself of the privileges of conducting
4 business in the United States, in the State of California, and in this District by
5 continuously and systematically placing goods into the stream of commerce through an
6 established distribution channel with the expectation that they will be purchased by
7 consumers in this District. In the State of California and in this District, NXP, directly
8 or through intermediaries: (i) performs at least a portion of the infringements alleged
9 herein; (ii) develops, designs, and/or manufactures products according to the
10 Lakshmanan patented process/methodology; (iii) distributes, markets, sells, or offers to
11 sell products formed according to the Lakshmanan patented process/methodology;
12 and/or (iv) imports products formed according to the Lakshmanan patented
13 process/methodology.

14 17. On information and belief, venue is proper in this Court pursuant to 28
15 U.S.C. §§ 1391 and 1400 because NXP has committed, and continues to commit, acts
16 of infringement in this District and has a regular and established place of business in
17 this District. For example, NXP maintains a regular and established place of business
18 at Innovation Drive, Suite 150, San Diego, CA 92128.

19 18. On information and belief, NXP currently employs more than 75 engineers in
20 the San Diego area. *See* Search Results for Current NXP Employees, LinkedIn
21 (available at
22 [https://www.linkedin.com/search/results/people/?currentCompany=%5B%221088%22%5D&geoUrn=%5B%22103918656%22%2C%2290010472%22%5D&keywords=e](https://www.linkedin.com/search/results/people/?currentCompany=%5B%221088%22%5D&geoUrn=%5B%22103918656%22%2C%2290010472%22%5D&keywords=engineer&origin=FACETED_SEARCH&sid=or8)
23 [ngineer&origin=FACETED_SEARCH&sid=or8](https://www.linkedin.com/search/results/people/?currentCompany=%5B%221088%22%5D&geoUrn=%5B%22103918656%22%2C%2290010472%22%5D&keywords=engineer&origin=FACETED_SEARCH&sid=or8)) (last visited August 15, 2022). In
24 addition, NXP is advertising 35 jobs at its San Diego location. These positions include
25 those that relate to the Lakshmanan patented process/methodology, such as positions
26 for a Principal Physical Design Engineer, Principal SoC Physical Design, SoC
27

1 Hardware Architect – Security, Principal System Integration Engineer, Principal
2 Verification Engineer, Principal Digital Design Engineer, and SoC Hardware Architect.
3 *See* NXP Job Listings, NXP ([available at](https://nxp.wd3.myworkdayjobs.com/careers?Location_Country=bc33aa3152ec42d4995f4791a106ed09&locations=98d67abaaa8a100fa6344859d7d49369)
4 [https://nxp.wd3.myworkdayjobs.com/careers?Location_Country=bc33aa3152ec42d49](https://nxp.wd3.myworkdayjobs.com/careers?Location_Country=bc33aa3152ec42d4995f4791a106ed09&locations=98d67abaaa8a100fa6344859d7d49369)
5 [95f4791a106ed09&locations=98d67abaaa8a100fa6344859d7d49369](https://nxp.wd3.myworkdayjobs.com/careers?Location_Country=bc33aa3152ec42d4995f4791a106ed09&locations=98d67abaaa8a100fa6344859d7d49369)) (last visited
6 August 18, 2022).

7 19. Venue is also convenient in this District. This is at least true because of
8 this District’s close ties to this case—including the technology, relevant witnesses, and
9 sources of proof noted above—and its ability to quickly and efficiently move this case
10 to resolution.

11 20. On information and belief, Bell Semic’s cause of action arises directly
12 from NXP’s circuit design work and other activities in this District. Moreover, on
13 information and belief, NXP has derived substantial revenues from its infringing acts
14 occurring within the State of California and within this District.

15 **U.S. PATENT NO. 7,149,989**

16 21. Bell Semic is the owner by assignment of the ’989 patent. The ’989 patent
17 is titled “Method of Early Physical Design Validation and Identification of Texted
18 Metal Short Circuits in an Integrated Circuit Design.” The ’989 patent issued on
19 December 12, 2006. A true and correct copy of the ’989 patent is attached as Exhibit
20 B.

21 22. The inventors of the ’989 patent are Viswanathan Lakshmanan, Alan
22 Holesovsky, Lisa Miller, and Jonathan Kuppinger.

23 23. The application that resulted in the issuance of the ’989 patent was filed
24 on September 22, 2004. The ’989 patent claims priority to September 22, 2004.

25 24. The ’989 patent generally relates to “methods of verifying an integrated
26 circuit design to ensure adherence to process rules and overall manufacturability of the
27 integrated circuit design for a specific technology.” Ex. B at 1:10–15.

1 25. The '989 patent identifies the shortcomings of the prior art. More
2 specifically, the specification describes that the prior validation methodology was
3 disadvantageous because “a design fault detected so late might reset the time schedule
4 for the entire integrated circuit design.” Ex. B at 2:42–44. In some cases, this means the
5 “design may have to be re-floorplanned, and the entire design cycle may have to be
6 reiterated.” Ex. B at 2:44–46. Existing early design validation processes resulted in
7 “substantial amount[s] of computer processing time that would severely impact the
8 product turnaround time.” Ex. B at 2:50–54. In addition, it would “falsely report” a
9 large number of design errors “due to the incomplete circuit design, making it difficult
10 to sort out the design errors that need to be corrected before the circuit design is
11 completed.” Ex. B at 2:54–58.

12 26. In light of the drawbacks of the prior art, the Inventors recognized the need
13 to “provide[] design rules that may be used in conjunction with a design rule check tool
14 and/or a layout vs. schematic tool in an early stage of the physical design to detect
15 design rule violations in floorplanning, including input/output cell placement and
16 construction and power distribution and power map structure.” Ex. B at 2:64–3:3.
17 Moreover, “texted metal short circuits may be identified most advantageously in the
18 early or evolutionary aspects of the design flow,” which reduc[es] the computer
19 processing time required to validate an integrated circuit design,” such as once layout
20 design is complete. Ex. B at 3: 3–11. The inventions claimed in the '989 patent address
21 this need.

22 27. The '989 patent contains two independent claims and 12 total claims,
23 covering a method and computer program product. Claim 1 reads:

24 1. A method comprising the steps of:

25
26 (a) receiving as input a representation of an integrated circuit
27 design;

1 (b) receiving as input a physical design rule deck that specifies rule
2 checks to be performed on the integrated circuit design;

3 (c) generating a specific rule deck from the physical design rule
4 deck wherein the specific rule deck includes only physical design
5 rules that are specific to texted metal short circuits between different
6 signal sources in addition to power and ground in the integrated
7 circuit design; and

8 (d) performing a physical design validation on the integrated circuit
9 design from the specific rule deck to identify texted metal short
10 circuits between different signal sources in addition to power and
11 ground in the integrated circuit design.

12 28. This claim, as a whole, provides significant benefits and improvements to
13 the function of the semiconductor device, *e.g.*, minimizing the potential for design-
14 based short circuits, ensuring overall manufacturability of devices, reducing probability
15 of failure, and ultimately lessening the likelihood of defective devices. *See, e.g.*, Ex. B
16 at 1:11–15; 3:3–19.

17 29. The claims of the '989 patent also recite inventive concepts that improve
18 the functioning of the fabrication process, particularly validation processes. The claims
19 of the '989 patent disclose a new and novel solution to specific problems related to end-
20 stage validation. As explained in detail above and in the '989 patent specification, the
21 claimed inventions improve upon the prior art processes by performing early-stage
22 validation on texted metal short circuits. This has the advantage of ensuring
23 manufacturability of devices, lessening the likelihood of short circuits and other defects,
24 as well as substantially reducing the time needed to finalize a circuit design. This allows
25 high-level power and signal-routing such that individual blocks with defined pins can
26 be finalized by the responsible members of design team in parallel, at substantial
27 decrease in design time and overall gains in efficiency.

28 ///

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U.S. PATENT NO. 7,260,803

1
2 30. Bell Semic is the owner by assignment of the '803 patent. The '803 patent
3 is titled "Incremental Dummy Metal Insertions." The '803 patent issued on August 21,
4 2007. A true and correct copy of the '803 patent is attached as Exhibit A.

5 31. The inventors of the '803 patent are Viswanathan Lakshmanan, Richard
6 Blinne, Vikram Shrowty, and Lena Montecillo.

7 32. The application that resulted in the issuance of the '803 patent was filed
8 on October 10, 2003. The '803 patent claims priority to October 10, 2003.

9 33. The '803 patent generally relates to "a method for performing dummy
10 metal insertion that avoids having to rerun the dummy fill software tool after the
11 integrated circuit design is changed." Ex. A at 1:6–10.

12 34. The '803 patent identifies the shortcomings of the prior art. More
13 specifically, the specification describes that the prior dummy fill methodologies were
14 disadvantageous because, when a customer requests a change, "the results of the
15 dummy fill tool are thrown out, and the dummy fill tool is rerun in order to ensure that
16 no dummy metal intersects with any of the design objects." Ex. A at 1:51–59.
17 Unfortunately, this "may delay completion of the design by another 30 hours" and may
18 "significantly impact the design schedule and result in cost overruns. Ex. A at 1:60–65.
19 This is especially true when multiple changes are requested.

20 35. In light of the drawbacks of the prior art, the Inventors recognized the need
21 to "insert[] dummy metal into an integrated circuit design after an ECO [Engineering
22 Change Order] without requiring reruns of the dummy fill tool." Ex. A at 1:66–2:1.
23 This "saves time on overall design execution" and helps manufacturers "meet
24 aggressive design schedules." Ex. B at 2:15–22; 4:52–57. The inventions claimed in
25 the '803 patent address this need.

1 36. The '803 patent contains two independent claims and 22 total claims,
2 covering a method and computer readable medium for performing dummy metal
3 insertion. Claim 1 reads:

4 1. A method for performing dummy metal insertion in design data for an
5 integrated circuit, which includes dummy metal objects inserted by a
6 dummy fill tool, comprising:

7 (a) after a portion of the design data is changed, performing a check
8 to determine whether any dummy metal objects intersect with any
9 other objects in the design data; and

10 (b) deleting the intersecting dummy metal objects from the design
11 data, thereby avoiding having to rerun the dummy fill tool.

12 37. This claim, as a whole, provides significant benefits and improvements to
13 the function of the semiconductor device, *e.g.*, minimizing the potential for design-
14 based short circuits, increasing the efficiency of the design process, and ensuring that
15 devices meet their minimum density requirements, which reduces the probability of
16 short circuits or other defects that render devices inoperable. *See, e.g.*, Ex. A at 1:24–
17 42.

18 38. The claims of the '803 patent also recite inventive concepts that improve
19 the functioning of the fabrication process, particularly dummy fill processes. The claims
20 of the '803 patent disclose a new and novel solution to specific problems related to
21 rerunning dummy fill tools after a change order is received. As explained in detail above
22 and in the '803 patent specification, the claimed inventions improve upon the prior art
23 processes by deleting dummy metal objects if a change order results in dummy metal
24 objects that intersect with other objects in the design data. This has the advantage of
25 maintaining minimum metal density without having to rerun the dummy fill tool, and
26 results in substantially reducing the time needed to finalize a circuit design due to the
27

1 ability to make late-stage ECOs and incremental changes in layout without needing to
2 re-run the dummy fill tool for the entire layer.

3 **COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,149,989**

4 39. Bell Semic re-alleges and incorporates by reference the allegations of the
5 foregoing paragraphs as if fully set forth herein.

6 40. The '989 patent is valid and enforceable under the United States Patent
7 Laws.

8 41. Bell Semic owns, by assignment, all right, title, and interest in and to the
9 '989 patent, including the right to collect for past damages.

10 42. A copy of the '989 patent is attached at Exhibit B.

11 43. On information and belief, NXP has and continues to directly infringe
12 pursuant to 35 U.S.C. § 271(a) one or more claims of the '989 patent by using the
13 patented methodology to design one or more devices, including as one example the
14 NXP LS1043A Quad-Core Networking Processor, in the United States.

15 44. On information and belief, NXP employs a variety of design tools, for
16 example, Cadence, Synopsys, and/or Siemens tools, to validate its circuit designs (the
17 "Accused Processes") as recited in the '989 patent claims. As one example, NXP's
18 Accused Processes perform a method that receives as input a representation of an
19 integrated circuit design as required by claim 1 of the '989 patent. NXP does so by
20 employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens
21 tool, into which a circuit design for its NXP LS1043A Quad-Core Networking
22 Processor is imported.

23 45. NXP's Accused Processes also receive as input a physical design rule deck
24 that specifies rule checks to be performed on the integrated circuit design. NXP does
25 so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or
26 Siemens tools, that receives various in-design verification processes for concurrent
27

1 physical design and verification of the NXP LS1043A Quad-Core Networking
2 Processor's circuit designs.

3 46. NXP's Accused Processes also generate a specific rule deck from the
4 physical design rule deck wherein the specific rule deck includes only physical design
5 rules that are specific to texted metal short circuits between different signal sources in
6 addition to power and ground in the integrated circuit design. NXP does so by
7 employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens
8 tools, that includes a "short finder," "short locator," or similar functionality that
9 identifies texted metal short circuits. For example, the Accused Processes allow
10 designers to select texted metal short circuits, which are shown by cell, text, net, layer,
11 and position. The nets may include ground, power, and other signal nets. An exemplary
12 infringement analysis showing infringement of one or more claims of the '989 patent
13 is set forth in Exhibit D. The declaration of Lloyd Linder, an expert in the field of
14 semiconductor device design, is attached at Exhibit E and further describes NXP's
15 infringement of the '989 patent.

16 47. NXP's Accused Processes infringe and continue to infringe one or more
17 claims of the '989 patent during the pendency of the '989 patent.

18 48. On information and belief, NXP has and continues to infringe pursuant to
19 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of
20 equivalents, by using the Accused Processes in violation of one or more claims of the
21 '989 patent. NXP has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*,
22 directly or indirectly, either literally or under the doctrine of equivalents, by making,
23 selling, or offering to sell in the United States, or importing into the United States
24 products manufactured or otherwise produced using the Accused Processes in violation
25 of one or more claims of the '989 patent.

1 49. NXP’s infringement of the ’989 patent is exceptional and entitles Bell
2 Semic to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C.
3 § 285.

4 50. Bell Semic has been damaged by NXP’s infringement of the ’989 patent
5 and will continue to be damaged unless NXP is enjoined by this Court. Bell Semic has
6 suffered and continues to suffer irreparable injury for which there is no adequate
7 remedy at law. The balance of hardships favors Bell Semic, and public interest is not
8 disserved by an injunction.

9 51. Bell Semic is entitled to recover from NXP all damages that Bell Semic
10 has sustained as a result of NXP’s infringement of the ’989 patent, including without
11 limitation and/or not less than a reasonable royalty.

12 **COUNT II – INFRINGEMENT OF U.S. PATENT NO. 7,260,803**

13 52. Bell Semic re-alleges and incorporates by reference the allegations of the
14 foregoing paragraphs as if fully set forth herein.

15 53. The ’803 patent is valid and enforceable under the United States Patent
16 Laws.

17 54. Bell Semic owns, by assignment, all right, title, and interest in and to the
18 ’803 patent, including the right to collect for past damages.

19 55. A copy of the ’803 patent is attached at Exhibit A.

20 56. On information and belief, NXP has and continues to directly infringe
21 pursuant to 35 U.S.C. § 271(a) one or more claims of the ’803 patent by using the
22 patented methodology to design one or more devices, including as one example the
23 NXP LS1043A Quad-Core Networking Processor, in the United States.

24 57. On information and belief, NXP employs a variety of design tools, for
25 example, Cadence, Synopsys, and/or Siemens tools, to delete intersecting dummy metal
26 objects from its circuit designs (the “Accused Processes”) as recited in the ’803 patent
27 claims. As one example, NXP’s Accused Processes perform a method of dummy metal
28

1 insertion in design data for an integrated circuit, which includes dummy metal objects
2 inserted by a dummy fill tool as required by claim 1 of the '803 patent. NXP does so
3 by employing a design tool, such as at least one of a Cadence, Synopsys, and/or
4 Siemens tool, that performs this dummy metal process for its NXP LS1043A Quad-
5 Core Networking Processor layout. The NXP LS1043A Quad-Core Networking
6 Processor includes dummy metal objects inserted by a dummy fill tool, such as an
7 “integrated” or “in-design” flow.

8 58. After a portion of the design data is changed, NXP’s Accused Processes
9 perform a check to determine whether any dummy metal objects intersect with any
10 other objects in the design data. When NXP receives an Engineering Change Order
11 (“ECO”), it employs a design tool, such as at least one of the Cadence, Synopsys, and/or
12 Siemens tools, to perform a Design Rule Check (“DRC”) to determine whether there
13 are any rule violations, including those related to metal fill geometries and layout
14 changes, in the NXP LS1043A Quad-Core Networking Processor’s design data.

15 59. NXP’s Accused Processes also delete the intersecting dummy metal
16 objects from the design data, thereby avoiding having to rerun the dummy fill tool. NXP
17 does so by employing a design tool, such as at least one of the Cadence, Synopsys,
18 and/or Siemens tools, that repairs DRC violations associated with shorts caused by
19 dummy fill geometries intersecting with other objects in the design data. For example,
20 the Accused Processes allow designers to trim metal fill geometries that cause the short
21 or DRC violation. An exemplary infringement analysis showing infringement of one or
22 more claims of the '803 patent is set forth in Exhibit C. The declaration of Lloyd Linder,
23 an expert in the field of semiconductor device design, is attached at Exhibit E and
24 further describes NXP’s infringement of the '803 patent.

25 60. NXP’s Accused Processes infringe and continue to infringe one or more
26 claims of the '803 patent during the pendency of the '803 patent.

1 61. On information and belief, NXP has and continues to infringe pursuant to
2 35 U.S.C. § 271, *et seq.*, directly or indirectly, either literally or under the doctrine of
3 equivalents, by using the Accused Processes in violation of one or more claims of the
4 '803 patent. NXP has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*,
5 directly or indirectly, either literally or under the doctrine of equivalents, by making,
6 selling, or offering to sell in the United States, or importing into the United States
7 products manufactured or otherwise produced using the Accused Processes in violation
8 of one or more claims of the '803 patent.

9 62. NXP's infringement of the '803 patent is exceptional and entitles Bell
10 Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C.
11 § 285.

12 63. Bell Semic has been damaged by NXP's infringement of the '803 patent
13 and will continue to be damaged unless NXP is enjoined by this Court. Bell Semic has
14 suffered and continues to suffer irreparable injury for which there is no adequate
15 remedy at law. The balance of hardships favors Bell Semic, and public interest is not
16 disserved by an injunction.

17 64. Bell Semic is entitled to recover from NXP all damages that Bell Semic
18 has sustained as a result of NXP's infringement of the '803 patent, including without
19 limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

- (a) a judgment declaring that NXP has infringed one or more claims of the Lakshmanan patents in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;
- (b) an award of damages adequate to compensate Bell Semic for infringement of the Lakshmanan patents by NXP, in an amount to be proven at trial, including supplemental post-verdict damages until such time as NXP ceases its infringing conduct;
- (c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting NXP and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with NXP, from committing further acts of infringement;
- (d) a judgment requiring NXP to make an accounting of damages resulting from NXP’s infringement of the Lakshmanan patents;
- (e) the costs of this action, as well as attorneys’ fees as provided by 35 U.S.C. § 285;
- (f) pre-judgment and post-judgment interest at the maximum amount permitted by law;
- (g) all other relief, in law or equity, to which Bell Semic is entitled.

1 Dated: August 26, 2022

By: /s/ Jennifer M. French

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17 **Pro Hac Applications forthcoming*

18 Attorneys for Plaintiff
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DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: August 26, 2022

By: /s/ Jennifer M. French

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