IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

POLARIS INNOVATIONS LIMITED, an Ireland limited company, Plaintiff v. NANYA TECHNOLOGY CORPORATION, Defendant.	§ § § § § § § § § § §	CIVIL ACTION NO. 2:23-cv-44 **JURY TRIAL DEMANDED**

PLAINTIFF'S COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Polaris Innovations Limited ("Polaris") files this Complaint against Defendant Nanya Technology Corporation ("NTC") for infringement of U.S. Patent No. 7,218,569 (the "'569 Patent"); U.S. Patent No. 7,405,992 (the "'992 Patent"); U.S. Patent No. 7,456,461 (the "'461 Patent"); U.S. Patent No. 7,471,547 (the "'547 Patent"); U.S. Patent No. 7,532,523 ("the '523 Patent"); and U.S. Patent No. 7,772,631 (the "'631 Patent"), collectively, the "Asserted Patents."

THE PARTIES

1. Polaris Innovations Limited is a corporation organized and existing under the laws of Ireland, with its principal place of business at 77 Lower Camden Street, Dublin D02 XE80, Ireland.

2. On information and belief, Nanya Technology Corporation is a corporation organized under the laws of Taiwan with its headquarters in Taiwan. NTC designs, imports, manufactures, markets, and sells Random Access Memory (RAM) throughout the world and in the United States. NTC conducts business in Texas and in the Eastern District of Texas, directly

or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others).

3. NTC is engaged in making, using, selling, offering for sale, and/or importing products, such as RAM, to and throughout the United States, including this District. NTC also induces its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, and customers in the making, using, selling, offering for sale, and/or importing such products to and throughout the United States, including this District. To this end, NTC and its foreign and U.S.-based subsidiaries—which act together as part of NTC's global network of sales and manufacturing emissaries—have operated as agents of, and for, one another and have otherwise acted vicariously for NTC as elements of the same business group and/or enterprise. Indeed, they work in concert and in orchestrated fashion, subject to agreements that are far nearer than arm's length, in order implement a distribution channel of infringing products within this District and the United States.

4. NTC maintains a substantial corporate presence in the United States via at least its U.S.-based sales subsidiaries, including Nanya Technology Corporation U.S.A ("NTC USA") and Nanya Technology Corporation Delaware ("NTC Delaware"). NTC U.S.A. is a California corporation with a principal place of business at 1735 Technology Drive, Suite 400, San Jose, California, 95110. NTC U.S.A. is a wholly-owned subsidiary of NTC. NTC Delaware is a Delaware corporation with a principal place of business at 20 Winter Sport Lane, Suite 105, Williston, Vermont, 05945. Defendant NTC Delaware is a wholly-owned subsidiary of NTC. NTC U.S.A. and NTC Delaware are responsible for NTC's domestic sales, offers for sale, importation, marketing, and support in North America. NTC U.S.A. and NTC Delaware are both NTC's agent, each operating at NTC's direction and control. Subject to such direction and control, NTC's U.S.-

based sales subsidiaries including, NTC U.S.A. and NTC Delaware, import and sell infringing products, such as DRAM, in the United States and this District.

5. Alone and through at least the activities of its U.S.-based sales subsidiaries (e.g., NTC U.S.A. and NTC Delaware), NTC conducts business in the United States and this District, including importing, distributing, and selling DRAM that infringes the Asserted Patents. *See Trois v. Apple Tree Auction Center, Inc.*, 882 F.3d 485, 490 (5th Cir. 2018) ("A defendant may be subject to personal jurisdiction because of the activities of its agent within the forum state…."); *see also Cephalon, Inc. v. Watson Pharmaceuticals, Inc.*, 629 F. Supp. 2d 338, 348 (D. Del. 2009) ("The agency theory may be applied not only to parents and subsidiaries, but also to companies that are 'two arms of the same business group,' operate in concert with each other, and enter into agreements with each other that are nearer than arm's length.").

6. Through importation, offers to sell, sales, distributions, and related agreements to transfer ownership of NTC's products (e.g., DRAM) with distributors and customers operating in and maintaining significant business presences in the United States, NTC does extensive business in the United States, this State, and this District.

JURISDICTION AND VENUE

7. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) and 1367.

8. This Court has specific and personal jurisdiction over NTC consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute because, *inter alia*: (i) NTC has done and continues to do business in Texas; and (ii) NTC has committed and continues to commit, directly or through intermediaries (including subsidiaries,

distributors, affiliates, retailers, suppliers, integrators, customers, and others), acts of patent infringement in this State. Such acts of infringement include making, using, offering to sell, and/or selling Accused Products (as more particularly identified and described throughout this Complaint, below) in this State and this District and/or importing Accused Products into this State and/or inducing others to commit acts of patent infringement in this State. Indeed, NTC has purposefully and voluntarily placed, and is continuing to place, one or more Accused Products into the stream of commerce through established distribution channels (including NTC Delaware's Texas offices) with the expectation and intent that such products will be sold to and purchased by consumers in the United States, this State, and this District; and with the knowledge and expectation that such products (whether in standalone form or as integrated in downstream products) will be imported into the United States, this State, and this District.

9. NTC has derived substantial revenues from its infringing acts occurring within this State and this District. It has substantial business in this State and this District, including: (i) at least part of its infringing activities alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent conduct, and/or deriving substantial revenue from infringing goods offered for sale, sold, and imported, and services provided to Texas residents vicariously through and/or in concert with its alter egos, intermediaries, agents, distributors, importers, customers, subsidiaries, and/or consumers.

10. This Court has personal jurisdiction over NTC, directly or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others) including its U.S.-based sales subsidiaries, e.g., NTC Delaware and NTC U.S.A. Through its direction and control of such subsidiaries, NTC has committed acts of direct and/or indirect patent infringement within this State and elsewhere within the United States giving rise to this

action and/or has established minimum contacts with this forum such that the exercise of personal jurisdiction over NTC would not offend traditional notions of fair play and substantial justice. NTC Delaware and NTC U.S.A. are wholly-owned subsidiaries of the NTC. The primary business of NTC Delaware and NTC U.S.A.is the marketing, support, and sale of NTC's electronic products in the United States. Upon information and belief, NTC compensates NTC Delaware and NTC U.S.A. for marketing, support, and sales services in the United States. As such, NTC has a direct financial interest in its U.S.-based subsidiaries, and vice versa.

11. NTC controls and otherwise directs and authorizes all activities of its U.S.-based sales subsidiaries, including NTC Delaware and NTC U.S.A. Such directed and authorized activities include the U.S.-based subsidiaries' using, offering for sale, selling, and/or importing the Accused Products, their components, and/or products containing the same that incorporate and/or perform the fundamental technologies covered by the Asserted Patents. NTC's U.S.-based sales subsidiaries (e.g., NTC Delaware and NTC U.S.A.) are expressly authorized to import, distribute, offer to sell, and sell the Accused Products on behalf of NTC. For example, NTC researches, designs, develops, and manufactures semiconductors, integrated circuits, MCUs, MPUs, and SoCs, and then directs its U.S.-based sales subsidiaries to import, distribute, offer for sale, and sell the Accused Products in the United States. *See, e.g., United States v. Hui Hsiung*, 778 F.3d 738, 743 (9th Cir. 2015) (finding that the sale of infringing products to third parties rather than for direct import into the U.S. did not "place [defendants'] conduct beyond the reach of United States law [or] escape culpability under the rubric of extraterritoriality"). NTC's U.S.-based sales subsidiaries also provide, on NTC's behalf, marketing and technical support services for the Accused Products from their facilities in the United States. For example, NTC Delaware and NTC U.S.A. help maintain a website that advertises the Accused Products, including identifying the applications for

which they can be used and providing related specifications. *See, e.g.*, https://www.nanya.com/en/Application and https://www.nanya.com/en/Product/. Such websites also contain user manuals, product documentation, and other materials related to NTC's products. For example, this website includes: (i) reference designs (https://www.nanya.com/en/Product/4221/NT6AP256T32AV-J1) relating to memory products, (ii) technical support documentation (https://myntc2.nanya.com/CDRM/Default.aspx?ReturnUrl=%2fCDRM%2f); (iii) reliability reports (https://myntc2.nanya.com/PRR/); and instructions on how to purchase NTC's products (https://www.nanya.com/en/Support/65/How%20to%20Buy). Thus, NTC's U.S.-based sales subsidiaries, including NTC Delaware and NTC U.S.A., conduct infringing activities on NTC's behalf.

12. On information and belief, because NTC's U.S.-based sales subsidiaries are authorized by NTC to import, distribute, offer to sell, and sell Accused Products and/or to perform the fundamental technologies covered by the Asserted Patents, NTC's U.S.-based sales subsidiaries' corporate presences in the United States give NTC substantially the same business advantages that it would enjoy if it conducted its business through its own offices and personnel.

13. In addition, NTC has knowingly induced, and continues to knowingly induce, infringement within this District by advertising, marketing, offering for sale and/or selling Accused Products (such as DRAM) that incorporate the fundamental technologies covered by the Asserted Patents. Such advertising, marketing, offering for sale and/or selling of Accused Products is directed to consumers, customers, manufacturers, integrators, suppliers, distributors, resellers, partners, and/or end users, and this includes providing instructions, user manuals, advertising,

and/or marketing materials facilitating, directing and encouraging use of infringing functionality with NTC's knowledge thereof.

14. NTC has, thus, in the multitude of ways described above, availed itself of the benefits and privileges of conducting business in this State and willingly subjected itself to the exercise of this Court's personal jurisdiction over it. Indeed, NTC has sufficient minimum contacts with this forum through its transaction of substantial business in this State and this District and its commission of acts of patent infringement as alleged in this Complaint that are purposefully directed towards this State and District.

15. Alternatively, the Court maintains personal jurisdiction over NTC under Federal Rule of Civil Procedure 4(k)(2).

16. Venue is proper in this District pursuant to 28 U.S.C. § 1391 because, among other things, NTC is not a resident of the United States, and thus may be sued in any judicial district, including this one, pursuant to 28 U.S.C. § 1391(c)(3). *See In re HTC Corp.*, 889 F.3d 1349, 1357 (Fed. Cir. 2018) ("The Court's recent decision in *TC Heartland* does not alter" the alien-venue rule.).

THE ASSERTED PATENTS

17. Polaris is the sole and exclusive owner of all right, title, and interest in the '569 Patent, the '992 Patent, the '461 Patent, the '547 Patent, the '523 Patent, and the '631 Patent and holds the exclusive right to take all actions necessary to enforce its rights in, and to, the Asserted Patents, including the filing of this patent infringement lawsuit. Polaris also has the right to recover all damages for past, present, and future infringements of the Asserted Patents and to seek injunctive relief as appropriate under the law.

18. The ’569 Patent is entitled “Memory circuit, and method for reading out data contained in the memory circuit using shared command signals.” The ’569 Patent issued May 15, 2007, and stems from U.S. Patent Application No. 11/135,212 which was filed on May 23, 2005.

19. The ’992 Patent is entitled “Method and apparatus for communicating command and address signals.” The ’992 Patent issued July 29, 2008, and stems from U.S. Patent Application No. 11/552,752, which was filed on October 25, 2006.

20. The ’461 Patent is entitled “Stacked capacitor array and fabrication method for a stacked capacitor array.” The ’461 Patent issued November 25, 2008, and stems from U.S. Patent Application No. 11/112,940 which was filed on April 22, 2005.

21. The ’547 Patent is entitled “Memory cell array.” The ’547 Patent issued December 30, 2008, and stems from U.S. Patent Application No. 11/945,437 which was filed on November 27, 2007.

22. The ’523 Patent is entitled “Memory chip with settable termination resistance circuit.” The ’523 Patent issued on May 12, 2009, and stems from U.S. Patent Application No. 11/461,380, which was filed on July 31, 2006.

23. The ’631 Patent is entitled “Method for fabricating a memory cell arrangement with a folded bit line arrangement and corresponding memory cell arrangement with a folded bit line arrangement.” The ’631 Patent issued on August 10, 2010, and stems from U.S. Patent Application 11/493,082, which was filed on July 26, 2006.

24. Polaris and its predecessors complied with the requirements of 35 U.S.C. § 287, to the extent necessary, such that Polaris may recover pre-suit damages.

25. The claims of the Asserted Patents are directed to patent eligible subject matter under 35 U.S.C. § 101. They are not directed to an abstract idea, and the technologies covered by

the claims comprise systems and/or consist of ordered combinations of features and functions that, at the time of invention, were not, alone or in combination, well-understood, routine, or conventional.

DEFENDANT'S PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENT

26. Prior to the filing of the Complaint, Polaris repeatedly attempted to engage NTC and/or its agents in licensing discussions related to the Asserted Patents:

a) On January 20, 2021, Polaris sent NTC's President, Dr. Pei Ing Lee, a letter to initiate patent licensing discussions. A copy of the letter was also emailed to Tracy Liu, an NTC employee. The letter identified certain Asserted Patents as being infringed by exemplary NTC products, and further included claim charts demonstrating how the identified products infringe the '569 Patent and '523 Patent. On information and belief, sometime after receiving this email, NTC configured its email servers to reject correspondence from Polaris.

b) On February 14, 2021, and April 14, 2021, Polaris attempted to follow up on its attempt to initiate patent licensing discussions via email to NTC employees Tracy Liu and Archi Hsu. NTC's servers rejected these emails as originating from a "banned sender."

c) On August 6, 2021, Polaris sent NTC a follow-up letter explaining the relevance of and the need to license its patent portfolio.

d) On November 1, 2021, Polaris sent NTC yet another follow-up letter identifying additional patents, including the '992 Patent, the '461 Patent, and the '631 Patent, as being infringed by exemplary NTC products.

27. NTC ignored or attempted to block Polaris' attempts to communicate and open a licensing dialogue. And when NTC eventually responded, it refused to participate in good-faith licensing discussions. As a result, Polaris was left with no other choice but to seek relief through litigation.

28. The Accused Products include, but are not limited to, the Exemplary Products identified in Polaris' letters to NTC. NTC's past and continuing sales of the Accused Products: (i) willfully infringe the Asserted Patents; and (ii) impermissibly usurp the significant benefits of Polaris' patented technologies without fairly compensating Polaris.

COUNT I

(INFRINGEMENT OF U.S. PATENT NO. of USP 7,218,569)

29. Plaintiff incorporates the preceding paragraphs herein by reference.

30. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

31. Polaris is the owner of all substantial rights, title, and interest in and to the '569 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

32. The '569 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on May 15, 2007, after full and fair examination.

33. NTC has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '569 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, NTC products, their components and processes, and/or products containing the same that incorporate the fundamental technologies

covered by the '569 Patent, including, but not limited to, its DDR4 SDRAM (collectively, the "'569 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

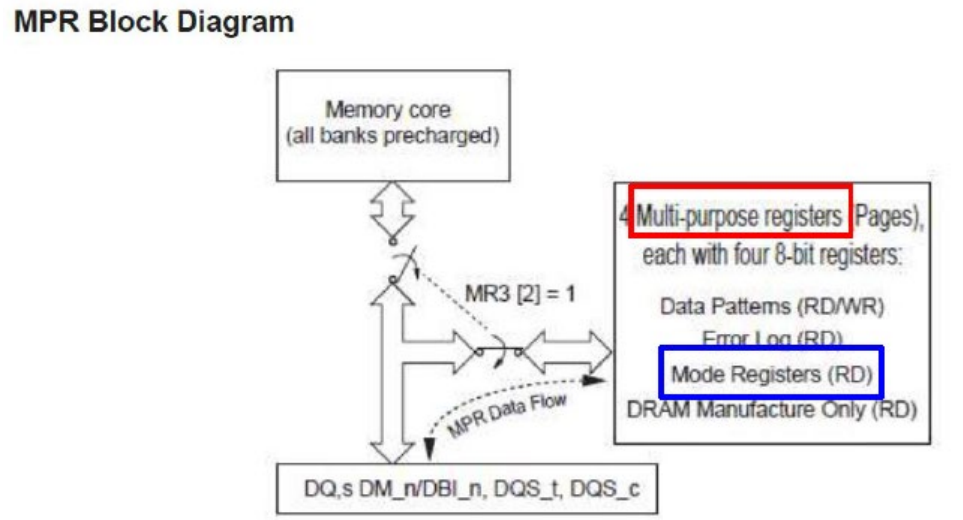
34. NTC has directly infringed and continues to directly infringe one or more claims of the '569 Patent in this District and elsewhere in Texas and the United States.

35. NTC has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 15 of the '569 Patent[1] as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '569 Accused Products. Furthermore, NTC makes and sells the '569 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '569 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '569 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, NTC directly infringes the '569 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including NTC Delaware and NTC U.S.A. Subject to NTC's direction and control, such subsidiaries conduct activities that constitute direct infringement of the '569 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '569

[1] Throughout this Complaint, wherever Polaris identifies specific claims of the Asserted Patents infringed by NTC, Polaris expressly reserves the right to identify additional claims and products in its infringement contentions in accordance with applicable local rules and the Court's case management order. Specifically identified claims throughout this Complaint are provided for notice pleading only.

Accused Products. NTC receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including NTC Delaware and NTC U.S.A.

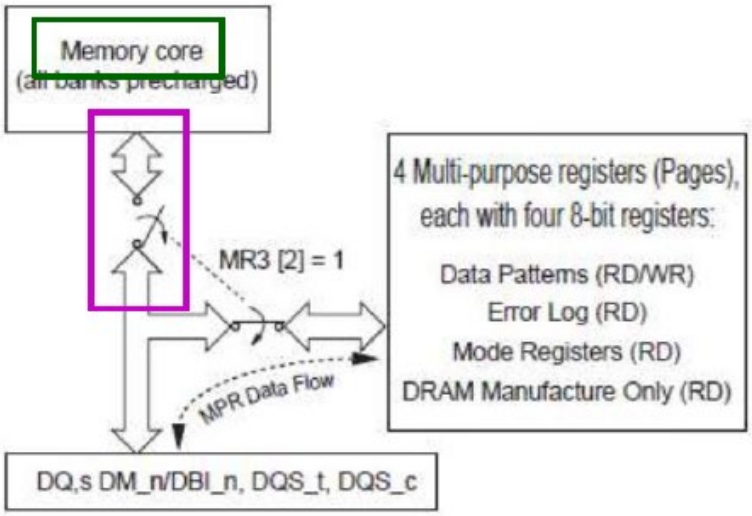
36. By way of illustration only, the '569 Accused Products include each and every element of claim 15 of the '569 Patent. The '569 Accused Products are a "memory device" that comprise the limitations of claim 15. For example, the '569 Accused Products comprise "a first memory area (red box) for storing first data (blue box)," as shown below:



Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

37. The '569 Accused Products comprise "a second memory area for storing second data." For example, the '569 Accused Products comprise a second memory area (green box) for storing second data (purple box), as shown below:

MPR Block Diagram



Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

38. The '569 Accused Products comprise "a command decoder for receiving and decoding command signals and outputting corresponding commands." For example, the '569 Accused Products comprise a command decoder for receiving and decoding command signals and outputting corresponding commands, as indicated by the orange box below:

DDR4 SDRAM Command Description and Operation

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table.
Note 5 applies to all Read/Write commands.
BG = Bank Group Address; BA = Bank Address; RA =Row Address; CA = Column Address;$\overline{BC}$ = Burst Chop;
X = Don't Care; V = Valid H or L

Symbol	Function		CKE Prev.	CKE Pres.	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG [1:0]	BA [1:0]	A12 /$\overline{BC}$	A [13,11]	A10 /AP	A [9:0]	Notes
MRS	Mode Register Set		H	H	L	H	L	L	L	BG	BA	OP code				12
WR	WRITE	Fixed BL8 or BC4	H	H	L	H	H	L	L	BG	BA	V	V	L	CA	
WRS4		BC4,on the fly	H	H	L	H	H	L	L	BG	BA	L	V	L	CA	
WRS8		BL8,on the fly	H	H	L	H	H	L	L	BG	BA	H	V	L	CA	
WRA	WRITE with auto precharge	Fixed BL8 or BC4	H	H	L	H	H	L	L	BG	BA	V	V	H	CA	
WRAS4		BC4,on the fly	H	H	L	H	H	L	L	BG	BA	L	V	H	CA	
WRAS8		BL8,on the fly	H	H	L	H	H	L	L	BG	BA	H	V	H	CA	
RD	READ	Fixed BL8 or BC4	H	H	L	H	H	L	H	BG	BA	V	V	L	CA	
RDS4		BC4,on the fly	H	H	L	H	H	L	H	BG	BA	L	V	L	CA	
RDS8		BL8,on the fly	H	H	L	H	H	L	H	BG	BA	H	V	L	CA	

Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

39. In the '569 Accused Products, while in a first mode of operation, the command decoder is configured to receive and decode a set of predetermined command signals to output a predetermined command causing the first data to be read out of the first memory area. For example, in the '569 Accused Products, while in a first mode of operation (aqua box), the command decoder is configured to receive and decode a set of predetermined command signals to output a predetermined command causing the first data to be read out of the first memory area (green box), as shown below:

MR3 definition

MPR Read Format	MPR Operation	MPR Page Selection	MPR Location
MR3[12:11]	MR3[2]	MR3[1:0]	MPR BA[1:0]

MR3 A12	MR3 A11	MPR Read Format
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

MR3 A2	MPR Operation
0	Normal Operation
1	Data flow from/to MPR

MR3 A1	MR3 A0	MPR Page Selection
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

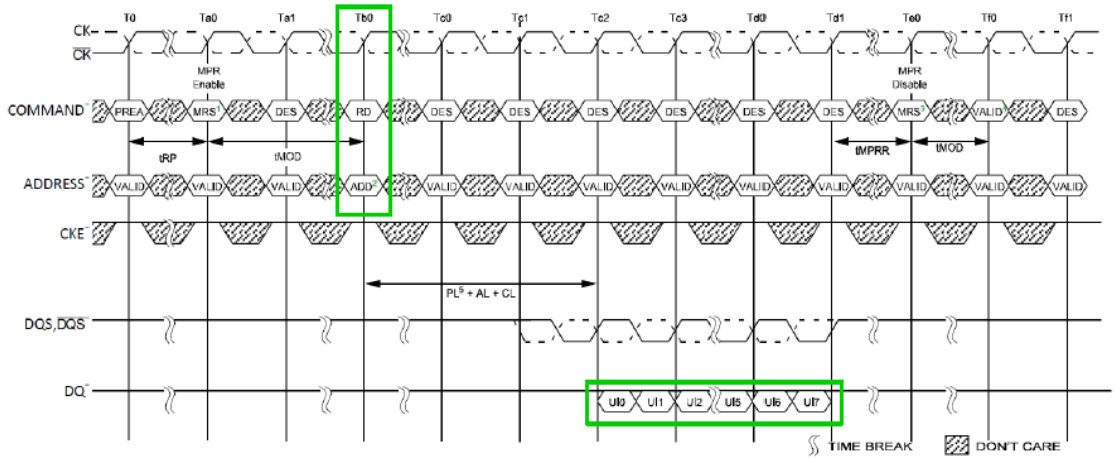
MPR BA1	MPR BA0	MPR Location
0	0	MPR0
0	1	MPR1
1	0	MPR2
1	1	MPR3

Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

DDR4-8Gb A-Die
NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4

MPR READ Timing

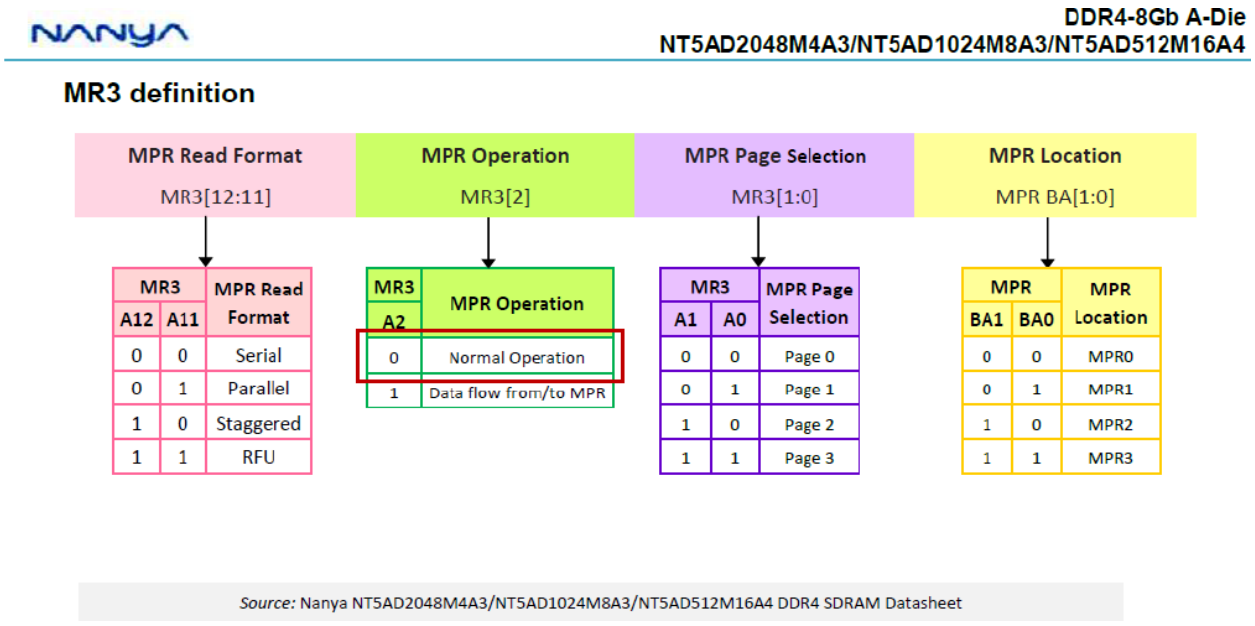
(BL = 8, PL=0, AL = 0, CL = 11, CAL = 3, Preamble = 1tCK)



Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

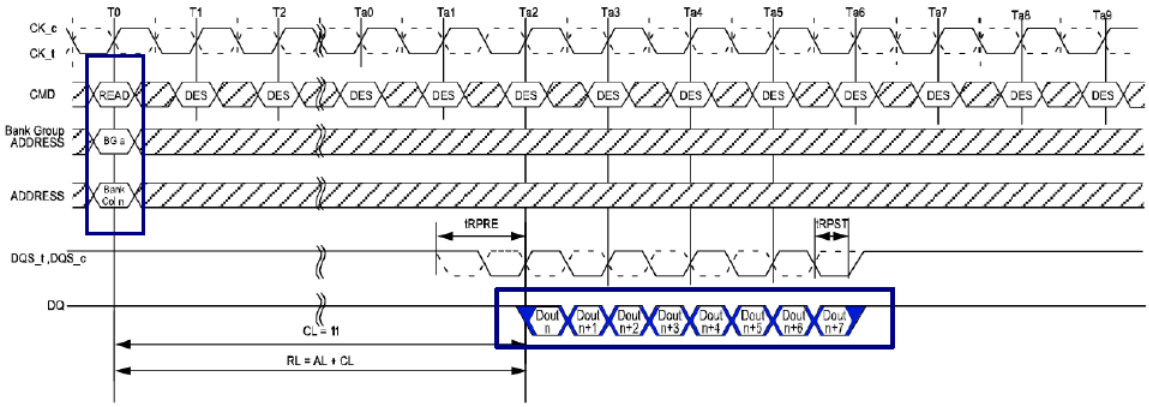
40. In the ’569 Accused Products, while in a second mode of operation, the command decoder is configured to receive and decode the set of predetermined command signals causing the second data to be read out of the second memory area. For example, in the ’569 Accused Products, while in a second mode of operation (red box), the command decoder is configured to

receive and decode the set of predetermined command signals causing the second data to be read out of the second memory area, as shown below (dark blue box):



Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

READ Burst Operation RL = 11 (AL = 0, CL = 11, BL8)



Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

41. In addition and/or in the alternative to its direct infringements, NTC has indirectly infringed and continues to indirectly infringe one or more claims of the '569 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers,

suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '569 Accused Products.

42. At a minimum, NTC has knowledge of the '569 Patent since being served with this Complaint. NTC also had knowledge of the '569 Patent since receiving a letter from Polaris providing details of its exemplary infringements prior to the filing of this Complaint. NTC also had knowledge of the '569 Patent since receiving detailed correspondence from Polaris dated January 20, 2021, alerting NTC to its infringements. Since receiving notice of its infringements, NTC has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '569 Patent. Indeed, NTC has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '569 Accused Products;[2] creating and/or maintaining established distribution channels for the '569 Accused Products into and within the United States; manufacturing the '569 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '569 Accused Products that promote their features, specifications, and applications;[3] promoting the incorporation

[2] *See, e.g.*, https://www.nanya.com/en/Product/List/450/2264 (last visited November 29, 2022).
[3] *See, e.g.*, https://www.nanya.com/en/Product/4467/NT5AD2048M4C3-JR (last visited November 29, 2022).

of the '569 Accused Products into end-user products,[4] and by providing technical support and/or related services for these products to purchasers in the United States.

Damages

43. On information and belief, despite having knowledge of the '569 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '569 Patent, NTC has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. NTC's infringing activities relative to the '569 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

44. Polaris has been damaged as a result of NTC's infringing conduct described in this Count. NTC is, thus, liable to Polaris in an amount that adequately compensates Polaris for NTC's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT II

(INFRINGEMENT OF U.S. PATENT NO. 7,405,992)

45. Plaintiff incorporates the preceding paragraphs herein by reference.

46. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

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[4] *See* https://www.nanya.com/en/Application/8/Home%20%20Entertainment (last visited November 29, 2022).

47. Polaris is the owner of all substantial rights, title, and interest in and to the '992 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

48. The '992 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on July 2, after full and fair examination.

49. NTC has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '992 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, NTC products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '992 Patent, including, but not limited to, its DDR4 SDRAM (collectively, the "'992 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

50. NTC has directly infringed and continues to directly infringe one or more claims of the '992 Patent in this District and elsewhere in Texas and the United States.

51. NTC has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the '992 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing, the '992 Accused Products. Furthermore, NTC makes and sells the '992 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '992 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '992 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

Furthermore, NTC directly infringes the '992 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including NTC Delaware and NTC U.S.A. Subject to NTC's direction and control, such subsidiaries conduct activities that constitute direct infringement of the '992 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '992 Accused Products. NTC receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including NTC Delaware and NTC U.S.A.

52. By way of illustration only, the '992 Accused Products include each and every element of claim 1 of the '992 Patent. The '992 Accused Products are a "device" that comprise the limitations of claim 1. For example, the '992 Accused Products comprise "a command bus interface comprising one or more command pins dedicated to receiving command inputs and one or more shared pins for selectively receiving address inputs and command inputs." For example, the '992 Accused Products comprise a command bus interface (shown in red below):

NANYA

DDR4-8Gb A-Die
NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4

DDR4 SDRAM Command Description and Operation

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table.
Note 5 applies to all Read/Write commands.
BG = Bank Group Address; BA = Bank Address; RA =Row Address; CA = Column Address; $\overline{BC}$ = Burst Chop; X = Don't Care; V = Valid H or L

Symbol	Function	CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG [1:0]	BA [1:0]	A12 /$\overline{BC}$	A [13,11]	A10 /AP	A [9:0]	Notes
		Prev.	Pres.												
MRS	Mode Register Set	H	H	L	H	L	L	L	BG	BA	OP code				12
REF	REFRESH	H	H	L	H	L	L	H	V	V	V	V	V	V	
SRE	Self Refresh Entry	H	L	L	H	L	L	H	V	V	V	V	V	V	7,9
SRX	Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V	
PRE	Single-Bank Precharge	H	H	L	H	L	H	L	BG	BA	V	V	L	V	
PREA	Precharge All Banks	H	H	L	H	L	H	L	V	V	V	V	H	V	
RFU	Reserved For Future Use	H	H	L	H	L	H	H	RFU						
ACT	Bank Active	H	H	L	L	Row Address(RA)			BG	BA	Row Address (RA)				

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

Further, the command bus interface comprises one or more command pins dedicated to receiving command inputs (shown in blue below):

DDR4 SDRAM Command Description and Operation

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table.
Note 5 applies to all Read/Write commands.
BG = Bank Group Address; BA = Bank Address; RA =Row Address; CA = Column Address; $\overline{BC}$ = Burst Chop;
X = Don't Care; V = Valid H or L

Symbol	Function	CKE		$\overline{CS}$	ACT	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG [1:0]	BA [1:0]	A12 /$\overline{BC}$	A [13,11]	A10 /AP	A [9:0]	Notes
		Prev.	Pres.												
MRS	Mode Register Set	H	H	L	H	L	L	L	BG	BA	OP code				12
REF	REFRESH	H	H	L	H	L	L	H	V	V	V	V	V	V	
SRE	Self Refresh Entry	H	L	L	H	L	L	H	V	V	V	V	V	V	7,9
SRX	Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V	
PRE	Single-Bank Precharge	H	H	L	H	L	H	L	BG	BA	V	V	L	V	
PREA	Precharge All Banks	H	H	L	H	L	H	L	V	V	V	V	H	V	
RFU	Reserved For Future Use	H	H	L	H	L	H	H	RFU						
ACT	Bank Active	H	H	L	L	Row Address(RA)			BG	BA	Row Address (RA)				

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

Further, the command bus interface comprises one or more shared pins for selectively receiving address inputs and command inputs (shown in green below):

DDR4 SDRAM Command Description and Operation

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table.
Note 5 applies to all Read/Write commands.
BG = Bank Group Address; BA = Bank Address; RA =Row Address; CA = Column Address; $\overline{BC}$ = Burst Chop;
X = Don't Care; V = Valid H or L

Symbol	Function	CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG [1:0]	BA [1:0]	A12 /$\overline{BC}$	A [13,11]	A10 /AP	A [9:0]	Notes
		Prev.	Pres.												
MRS	Mode Register Set	H	H	L	H	L	L	L	BG	BA	OP code				12
REF	REFRESH	H	H	L	H	L	L	H	V	V	V	V	V	V	
SRE	Self Refresh Entry	H	L	L	H	L	L	H	V	V	V	V	V	V	7,9
SRX	Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V	
PRE	Single-Bank Precharge	H	H	L	H	L	H	L	BG	BA	V	V	L	V	
PREA	Precharge All Banks	H	H	L	H	L	H	L	V	V	V	V	H	V	
RFU	Reserved For Future Use	H	H	L	H	L	H	H	RFU						
ACT	Bank Active	H	H	L	L	Row Address(RA)			BG	BA	Row Address (RA)				

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

53. The '992 Accused Products comprise "an address bus interface comprising one or more address pins dedicated to receiving address inputs and one or more shared pins for selectively receiving address inputs and command inputs." For example, the '992 Accused Products comprise an address bus, shown below in pink.

DDR4 SDRAM Command Description and Operation

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table.
Note 5 applies to all Read/Write commands.
BG = Bank Group Address; BA = Bank Address; RA =Row Address; CA = Column Address;$\overline{BC}$ = Burst Chop;
X = Don't Care; V = Valid H or L

Symbol	Function	CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG [1:0]	BA [1:0]	A12 /$\overline{BC}$	A [13,11]	A10 /AP	A [9:0]	Notes
		Prev.	Pres.												
MRS	Mode Register Set	H	H	L	H	L	L	L	BG	BA	OP code				12
REF	REFRESH	H	H	L	H	L	L	H	V	V	V	V	V	V	
SRE	Self Refresh Entry	H	L	L	H	L	L	H	V	V	V	V	V	V	7,9
SRX	Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V	
PRE	Single-Bank Precharge	H	H	L	H	L	H	L	BG	BA	V	V	L	V	
PREA	Precharge All Banks	H	H	L	H	L	H	L	V	V	V	V	H	V	
RFU	Reserved For Future Use	H	H	L	H	L	H	H	RFU						
ACT	Bank Active	H	H	L	L	Row Address(RA)			BG	BA	Row Address (RA)				

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

Further, the address bus comprises one or more address pins dedicated to receiving address inputs, shown below in orange.

DDR4 SDRAM Command Description and Operation

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table.
Note 5 applies to all Read/Write commands.
BG = Bank Group Address; BA = Bank Address; RA =Row Address; CA = Column Address;$\overline{BC}$ = Burst Chop;
X = Don't Care; V = Valid H or L

Symbol	Function	CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG [1:0]	BA [1:0]	A12 /$\overline{BC}$	A [13,11]	A10 /AP	A [9:0]	Notes
		Prev.	Pres.												
MRS	Mode Register Set	H	H	L	H	L	L	L	BG	BA	OP code				12
REF	REFRESH	H	H	L	H	L	L	H	V	V	V	V	V	V	
SRE	Self Refresh Entry	H	L	L	H	L	L	H	V	V	V	V	V	V	7,9
SRX	Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V	
PRE	Single-Bank Precharge	H	H	L	H	L	H	L	BG	BA	V	V	L	V	
PREA	Precharge All Banks	H	H	L	H	L	H	L	V	V	V	V	H	V	
RFU	Reserved For Future Use	H	H	L	H	L	H	H	RFU						
ACT	Bank Active	H	H	L	L	Row Address(RA)			BG	BA	Row Address (RA)				

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

Further the address bus comprises one or more shared pins for selectively receiving address inputs and command inputs, shown below in blue.

DDR4 SDRAM Command Description and Operation

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table.
Note 5 applies to all Read/Write commands.
BG = Bank Group Address; BA = Bank Address; RA =Row Address; CA = Column Address; $\overline{BC}$ = Burst Chop;
X = Don't Care; V = Valid H or L

Symbol	Function	CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG [1:0]	BA [1:0]	A12 /$\overline{BC}$	A [13,11]	A10 /AP	A [9:0]	Notes
		Prev.	Pres.												
MRS	Mode Register Set	H	H	L	H	L	L	L	BG	BA	OP code				12
REF	REFRESH	H	H	L	H	L	L	H	V	V	V	V	V	V	
SRE	Self Refresh Entry	H	L	L	H	L	L	H	V	V	V	V	V	V	7,9
SRX	Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V	
PRE	Single-Bank Precharge	H	H	L	H	L	H	L	BG	BA	V	V	L	V	
PREA	Precharge All Banks	H	H	L	H	L	H	L	V	V	V	V	H	V	
RFU	Reserved For Future Use	H	H	L	H	L	H	H	RFU						
ACT	Bank Active	H	H	L	L	Row Address(RA)			BG	BA	Row Address (RA)				

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

Source: Nanya NT5AD2048M4A3/NT5AD1024M8A3/NT5AD512M16A4 DDR4 SDRAM Datasheet

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

54. In addition and/or in the alternative to its direct infringements, NTC has indirectly infringed and continues to indirectly infringe one or more claims of the '992 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '992 Accused Products.

55. At a minimum, NTC has knowledge of the '992 Patent since being served with this Complaint. NTC also had knowledge of the '992 Patent since receiving a letter from Polaris providing details of its exemplary infringements prior to the filing of this Complaint. NTC also had knowledge of the '992 Patent since receiving detailed correspondence from Polaris dated November 1, 2021, alerting NTC to its infringements. Since receiving notice of its infringements, NTC has actively induced the direct infringements of its subsidiaries, distributors, affiliates,

retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '992 Patent. Indeed, NTC has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '992 Accused Products;[5] creating and/or maintaining established distribution channels for the '992 Accused Products into and within the United States; manufacturing the '992 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '992 Accused Products that promote their features, specifications, and applications;[6] promoting the incorporation of the '992 Accused Products into end-user products,[7] and by providing technical support and/or related services for these products to purchasers in the United States.

Damages

56. On information and belief, despite having knowledge of the '992 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '992 Patent, NTC has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. NTC's infringing activities relative to the '992 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such

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[5] *See, e.g.*, https://www.nanya.com/en/Product/List/450/2264 (last visited November 29, 2022).
[6] *See, e.g.*, https://www.nanya.com/en/Product/4467/NT5AD2048M4C3-JR (last visited November 29, 2022).
[7] *See* https://www.nanya.com/en/Application/8/Home%20%20Entertainment (last visited November 29, 2022).

that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

57. Polaris has been damaged as a result of NTC's infringing conduct described in this Count. NTC is, thus, liable to Polaris in an amount that adequately compensates Polaris for NTC's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT III

(INFRINGEMENT OF U.S. PATENT NO. of USP 7,456,461)

58. Plaintiff incorporates the preceding paragraphs herein by reference.

59. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

60. Polaris is the owner of all substantial rights, title, and interest in and to the '461 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

61. The '461 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on November 25, 2008, after full and fair examination.

62. NTC has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '461 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, NTC products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '461 Patent, including, but not limited to, its DDR4 SDRAM (collectively, the "'461 Accused Products").

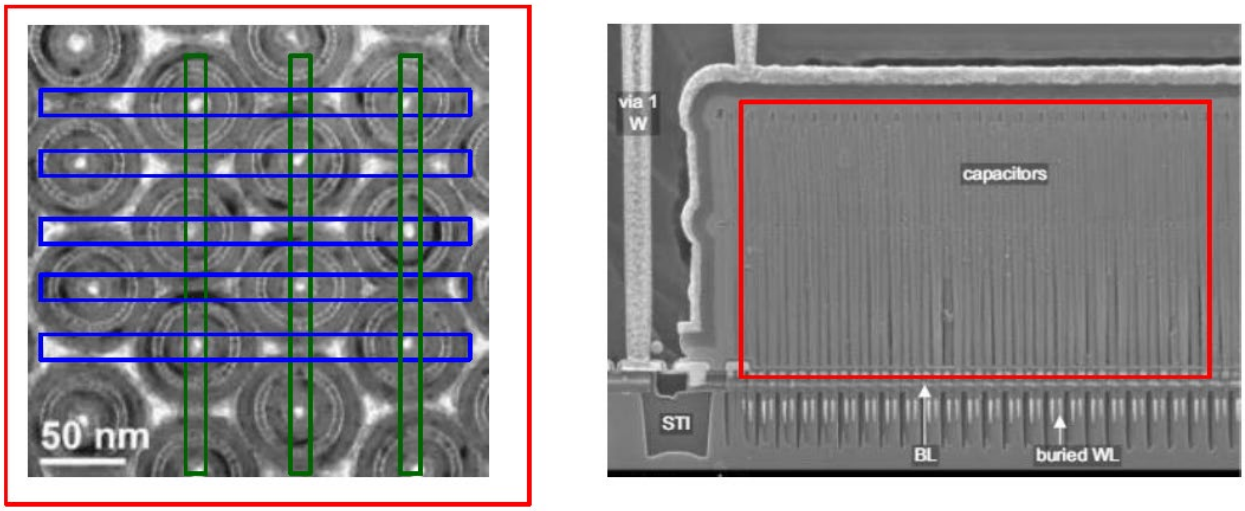
Direct Infringement (35 U.S.C. § 271(a))

63. NTC has directly infringed and continues to directly infringe one or more claims of the '461 Patent in this District and elsewhere in Texas and the United States.

64. NTC has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the '461 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '461 Accused Products. Furthermore, NTC makes and sells the '461 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '461 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '461 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, NTC directly infringes the '461 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including NTC Delaware and NTC U.S.A. Subject to NTC's direction and control, such subsidiaries conduct activities that constitute direct infringement of the '461 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '461 Accused Products. NTC receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including NTC Delaware and NTC U.S.A.

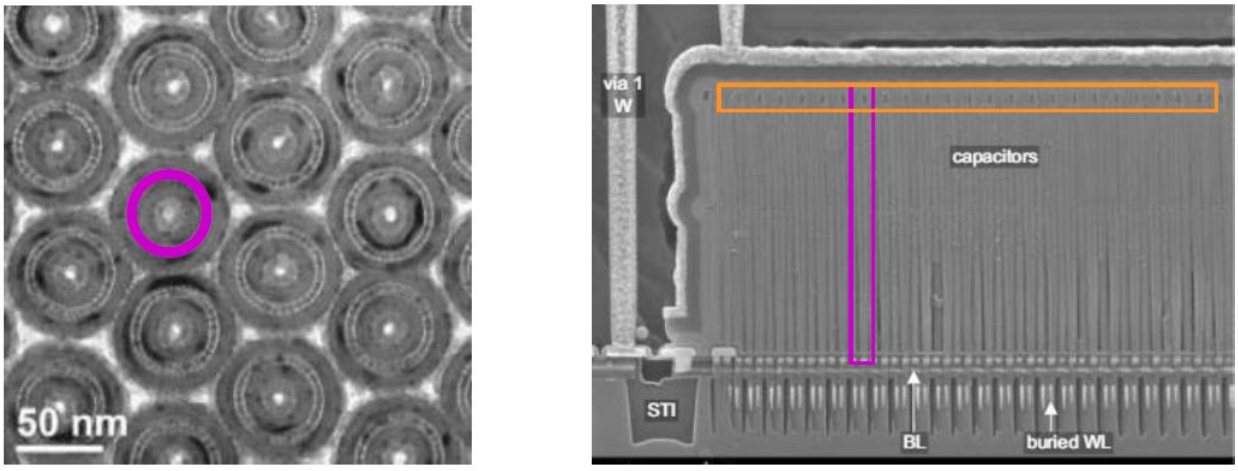
65. By way of illustration only, the '461 Accused Products include each and every element of claim 1 of the '461 Patent. The '461 Accused Products include "[a]n array of stacked capacitors" that comprise the limitations of claim 1. For example, the '461 Accused Products comprise "a multiplicity of stacked capacitors (red box) aligned in at least two rows (blue boxes) extending in one of two first specific but different directions such that the stack capacitors of adjacent rows are aligned in at least two columns (green boxes) extending in another one of said

two first specific directions, said rows and said columns extending in said two first specific directions," as shown below:



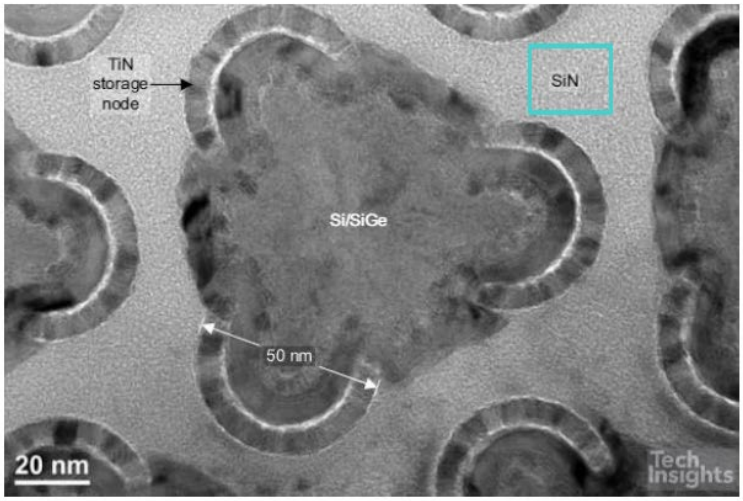
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 18, 16

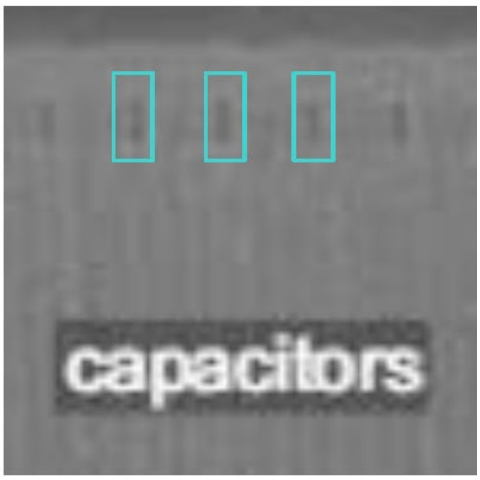
66. The '461 Accused Products comprise "each of said capacitors of said multiplicity having an electrode layer extending away from a surface of a substrate to an upper region and said electrode layer further defining a top portion at said upper region." For example, in the '461 Accused Products each of said capacitors of said multiplicity has an electrode layer extending away from a surface of a substrate to an upper region (purple box) and said electrode layer further defining a top portion (orange box) at said upper region, as shown below:



Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 18, 16

67. The '461 Accused Products comprise "an insulator in said upper region and between at least one of said rows and said columns to provide spacing and to prevent the electrode layer of each of said stacked capacitors in said adjacent rows and columns from touching and such that there is no electrical contact." For example, the '461 Accused Products comprise an insulator in said upper region (aqua boxes) and between at least one of said rows and said columns to provide spacing and to prevent the electrode layer of each of said stacked capacitors in said adjacent rows and columns from touching and such that there is no electrical contact, as shown below:





Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 18, 16

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

68. In addition and/or in the alternative to its direct infringements, NTC has indirectly infringed and continues to indirectly infringe one or more claims of the ’461 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’461Accused Products.

69. At a minimum, NTC has knowledge of the ’461 Patent since being served with this Complaint. NTC also had knowledge of the ’461 Patent since receiving a letter from Polaris providing details of its exemplary infringements prior to the filing of this Complaint. NTC also had knowledge of the ’461 Patent since receiving detailed correspondence from Polaris dated November 1, 2021, alerting NTC to its infringements. Since receiving notice of its infringements, NTC has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’461 Patent. Indeed, NTC has

intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '461 Accused Products;[8] creating and/or maintaining established distribution channels for the '461Accused Products into and within the United States; manufacturing the '461 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '461 Accused Products that promote their features, specifications, and applications;[9] promoting the incorporation of the '461 Accused Products into end-user products,[10] and by providing technical support and/or related services for these products to purchasers in the United States.

Damages

70. On information and belief, despite having knowledge of the '461 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '461 Patent, NTC has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. NTC's infringing activities relative to the '461 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

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[8] *See, e.g.*, https://www.nanya.com/en/Product/List/450/2264 (last visited November 29, 2022).
[9] *See, e.g.*, https://www.nanya.com/en/Product/4467/NT5AD2048M4C3-JR (last visited November 29, 2022).
[10] *See* https://www.nanya.com/en/Application/8/Home%20%20Entertainment (last visited November 29, 2022).

71. Polaris has been damaged as a result of NTC's infringing conduct described in this Count. NTC is, thus, liable to Polaris in an amount that adequately compensates Polaris for NTC's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT IV

(INFRINGEMENT OF U.S. PATENT NO. of USP 7,471,547)

72. Plaintiff incorporates the preceding paragraphs herein by reference.

73. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

74. Polaris is the owner of all substantial rights, title, and interest in and to the '547 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

75. The '547 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on December 30, 2008, after full and fair examination.

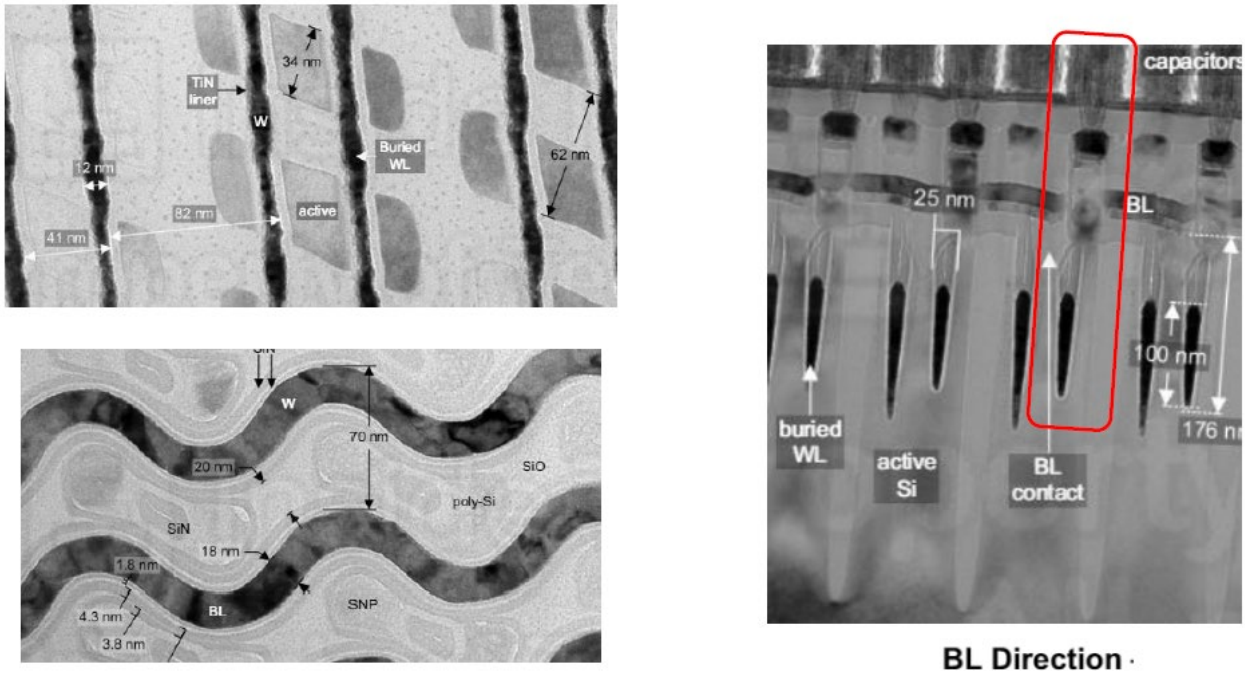
76. NTC has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '547 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, NTC products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '547 Patent, including, but not limited to, its DDR4 SDRAM (collectively, the "'547 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

77. NTC has directly infringed and continues to directly infringe one or more claims of the '547 Patent in this District and elsewhere in Texas and the United States.

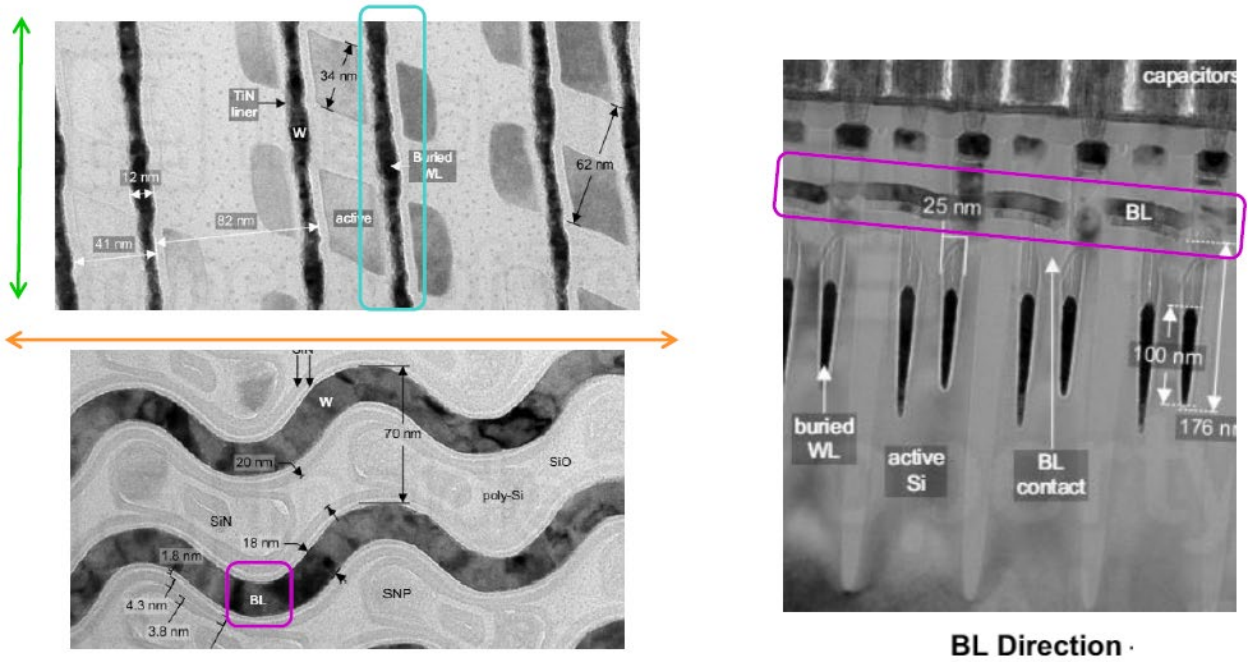
78. NTC has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 10 of the '547 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '547 Accused Products. Furthermore, NTC makes and sells the '547 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '547 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '547 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, NTC directly infringes the '547 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including NTC Delaware and NTC U.S.A. Subject to NTC's direction and control, such subsidiaries conduct activities that constitute direct infringement of the '547 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '547 Accused Products. NTC receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including NTC Delaware and NTC U.S.A.

79. By way of illustration only, the '547 Accused Products include each and every element of claim 15 of the '547 Patent. The '547 Accused Products are "[a]n integrated circuit including a memory cell array" that comprise the limitations of claim 10. For example, the '547 Accused Products comprise "memory cells, each of the memory cells comprising a storage element and an access transistor," as shown in the red box below:



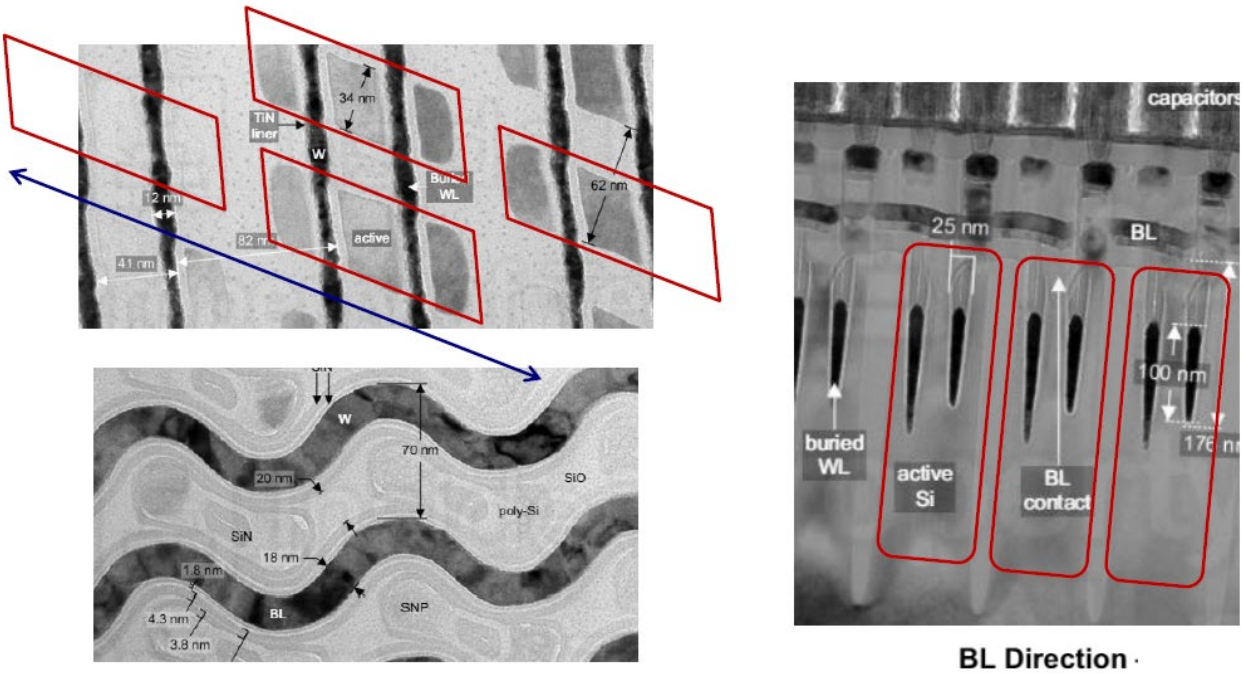
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 26, 28

80. The '547 Accused Products comprise "bit lines running along a first direction; word lines running along a second direction that is transverse the first direction." For example, the '547 Accused Products comprise bit lines (purple box) running along a first direction (orange line); word lines (aqua box) running along a second direction that is transverse the first direction (green line), as shown below:



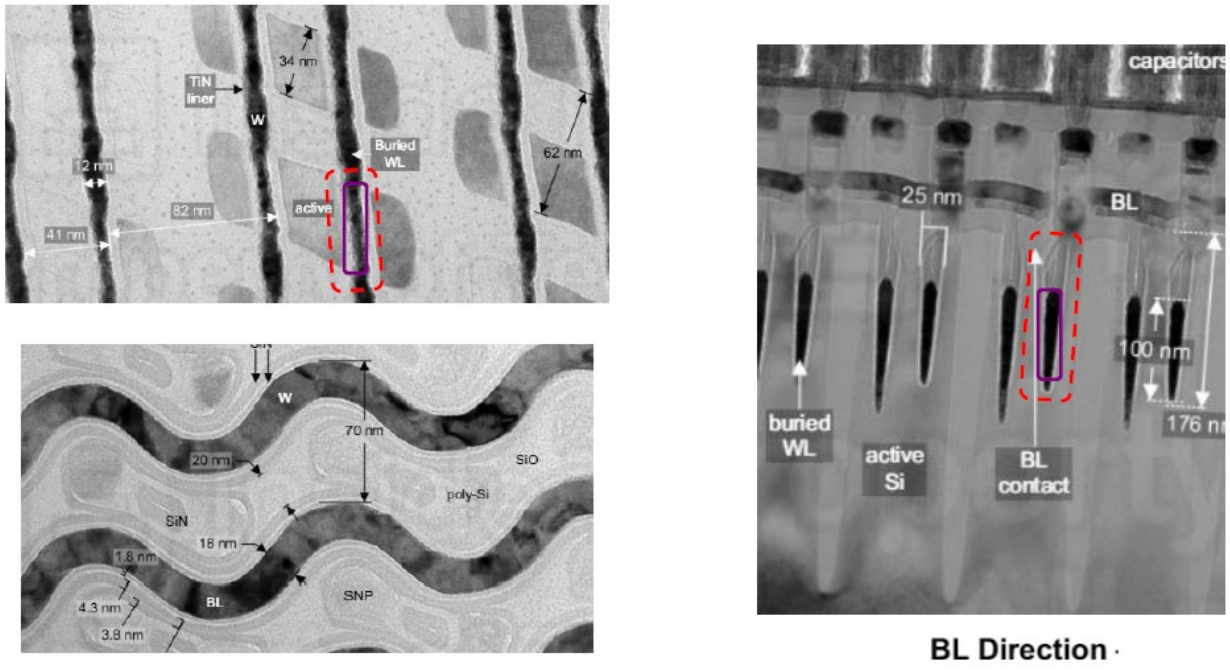
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

81. The '547 Accused Products comprise "active areas extending in a direction that is slanted with respect to the first and second directions." For example, the '547 Accused Products comprise active areas (red boxes) extending in a direction that is slanted with respect to the first and second directions (dark blue line), as shown below:



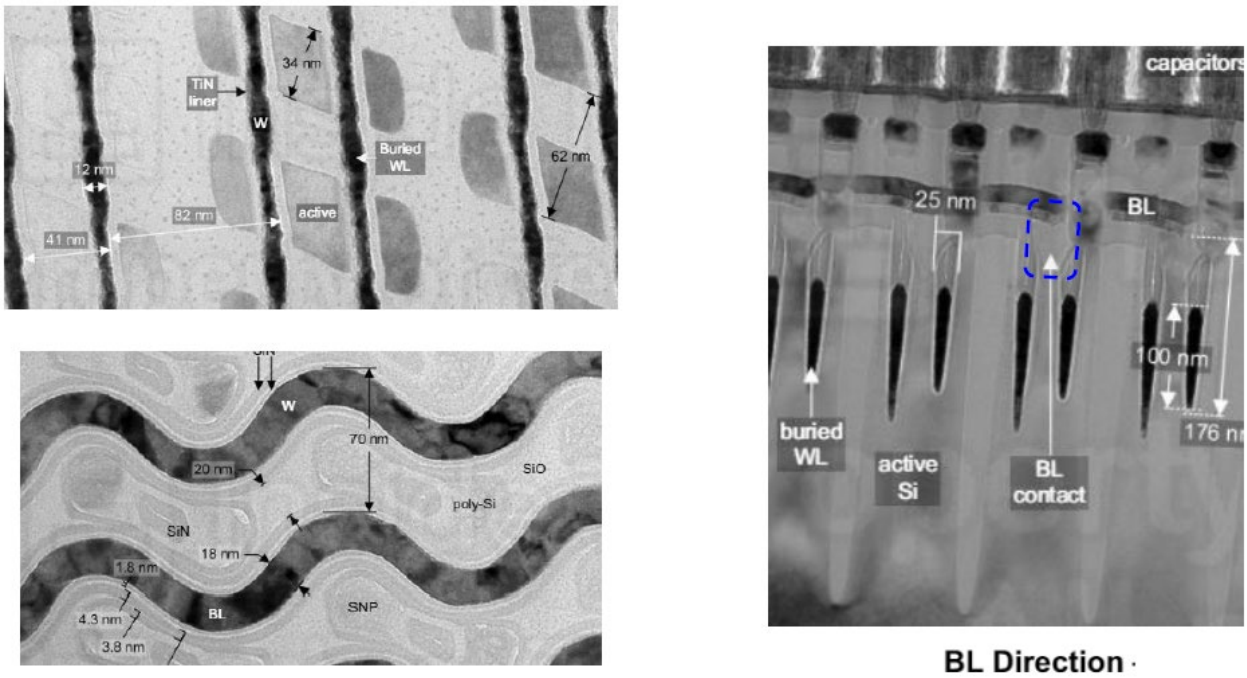
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

82. The '547 Accused Products comprise "gate electrodes of the access transistors being disposed in gate grooves that are formed in the active areas." For example, the '547 Accused Products comprise gate electrodes (purple box) of the access transistors being disposed in gate grooves (dashed red box) that are formed in the active areas, as shown below:



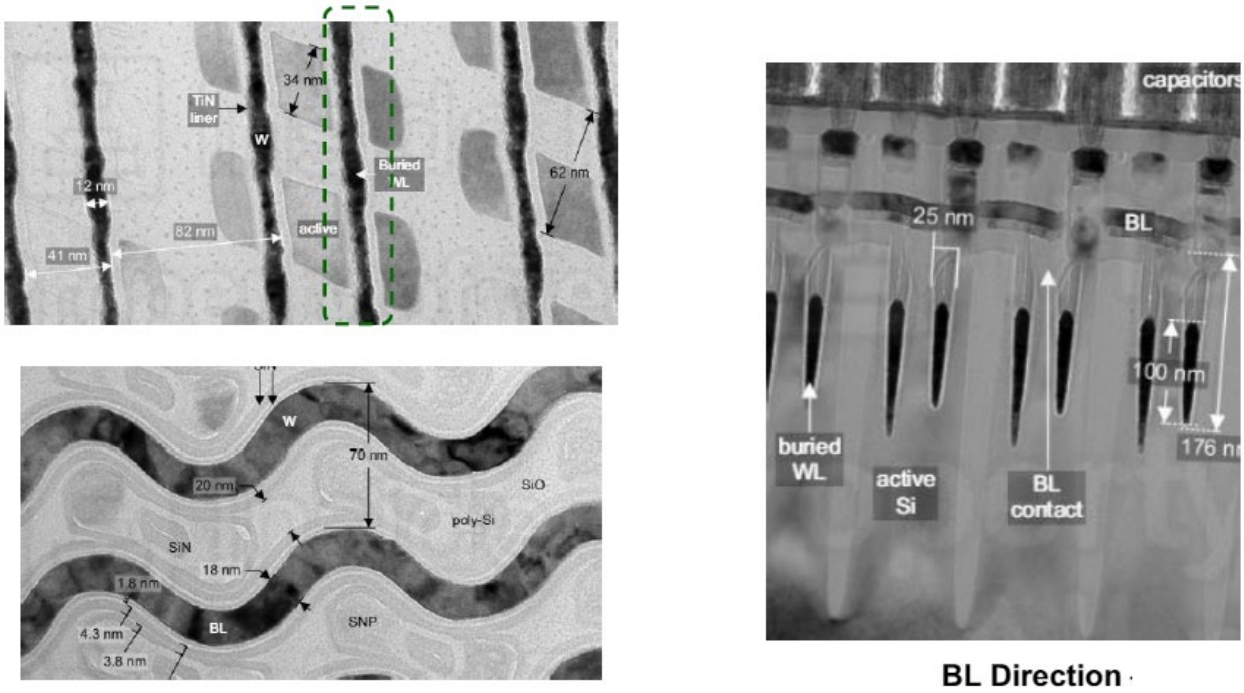
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

83. The '547 Accused Products comprise "the access transistors electrically coupling corresponding storage elements to corresponding bit lines via bit line contacts." For example, the '547 Accused Products comprise the access transistors electrically coupling corresponding storage elements to corresponding bit lines via bit line contacts, as shown in the dashed blue box below:



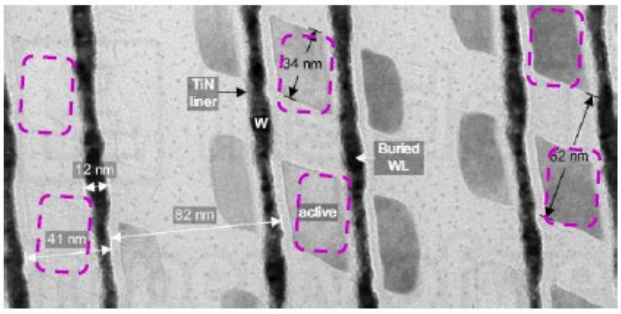
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

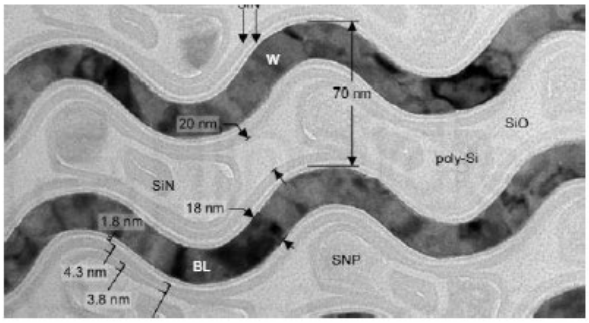
84. The ’547 Accused Products comprise “the transistors being addressed by the word lines.” For example, the ’547 Accused Products comprise the transistors being addressed by the word lines, as shown in the dashed green box below:

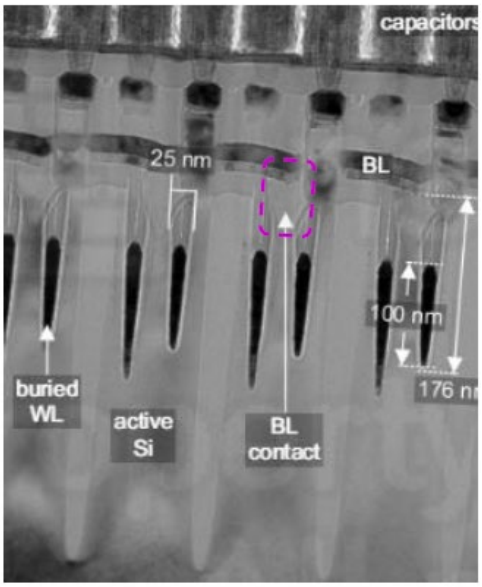


Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

85. In the '547 Accused Products, "the bit line contacts are formed in a region generally defined by an intersection of a bit line and a corresponding active area line." For example, in the '547 Accused Products, the bit line contacts are formed in a region generally defined by an intersection of a bit line and a corresponding active area line, as shown in the purple boxes below:



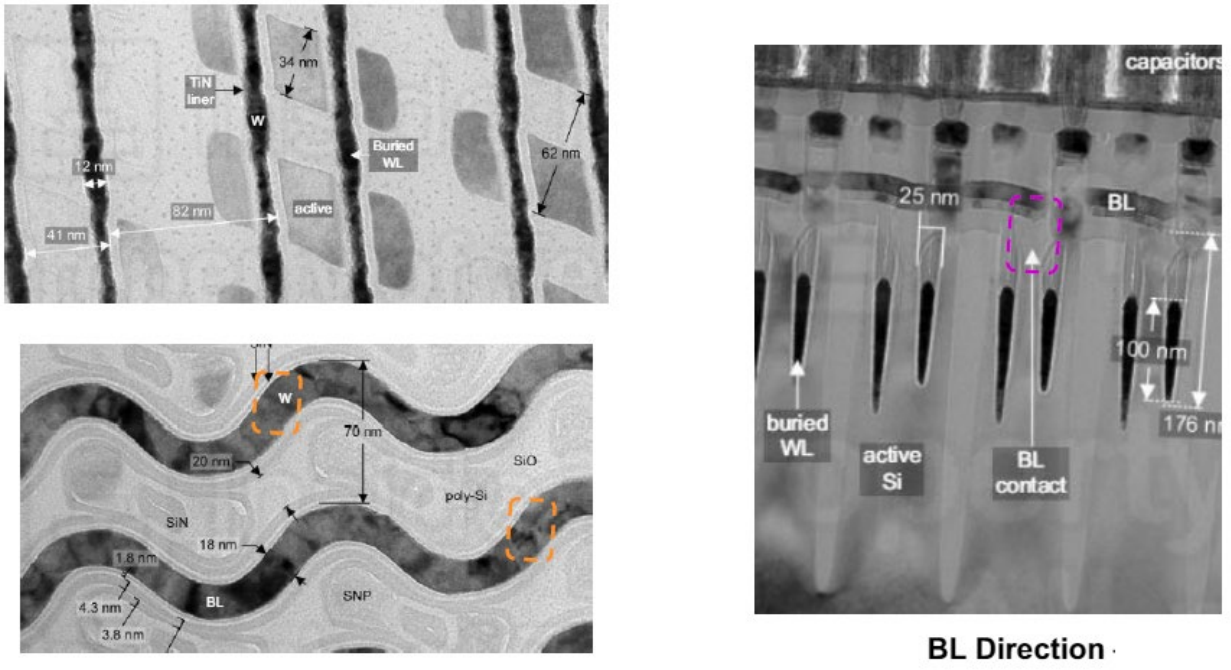




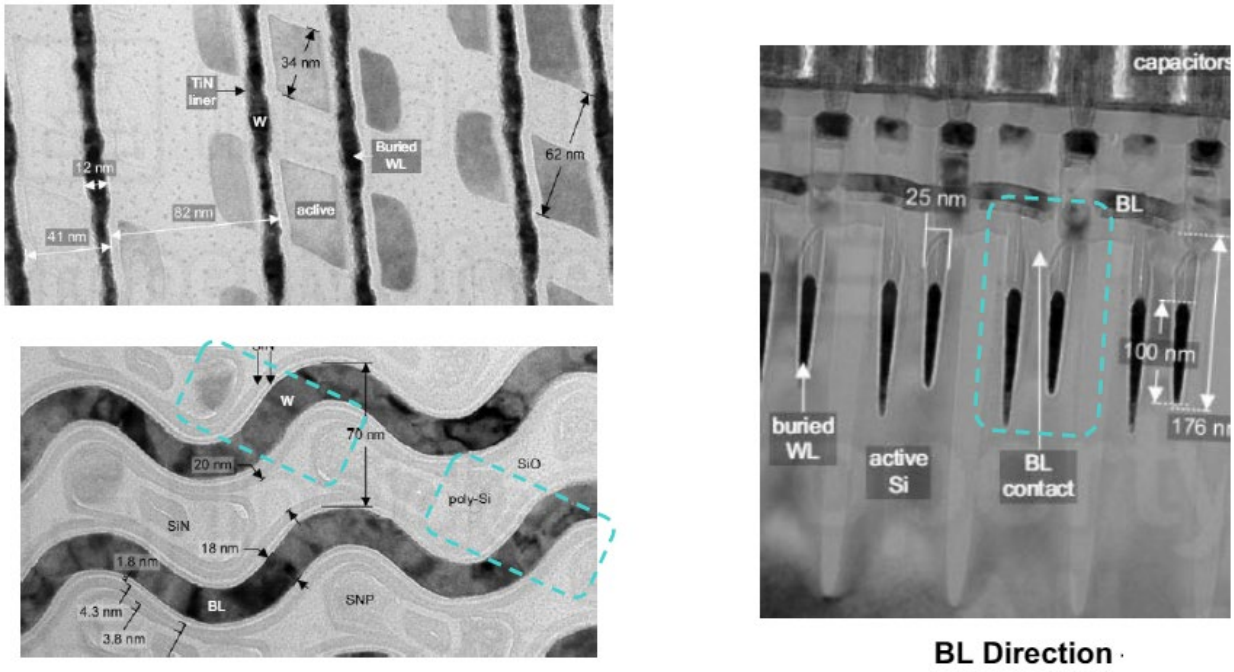
BL Direction

Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

86. In the '547 Accused Products, "neighboring bit line contacts, that are shifted along a direction that is slanted with respect to the first and second directions, are connected with neighboring bit lines and wherein each of the memory cells is coupled to one bit line." For example, in the '547 Accused Products, neighboring bit line contacts, that are shifted along a direction that is slanted with respect to the first and second directions, are connected with neighboring bit lines (orange dashed boxes) and wherein each of the memory cells is coupled to one bit line (aqua dashed box), as shown below:



Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28



Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

87. In addition and/or in the alternative to its direct infringements, NTC has indirectly infringed and continues to indirectly infringe one or more claims of the '547 Patent by knowingly

and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '547 Accused Products.

88. At a minimum, NTC has knowledge of the '547 Patent since being served with this Complaint. NTC also had knowledge of the '547 Patent since receiving a letter from Polaris providing details of its exemplary infringements prior to the filing of this Complaint. Since receiving notice of its infringements, NTC has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '547 Patent. Indeed, NTC has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '547 Accused Products;[11] creating and/or maintaining established distribution channels for the '547 Accused Products into and within the United States; manufacturing the '547 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '547 Accused Products that promote their features, specifications, and applications;[12] promoting the incorporation of the '547 Accused Products into end-user products,[13]

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[11] *See, e.g.*, https://www.nanya.com/en/Product/List/450/2264 (last visited November 29, 2022).
[12] *See, e.g.*, https://www.nanya.com/en/Product/4467/NT5AD2048M4C3-JR (last visited November 29, 2022).
[13] *See* https://www.nanya.com/en/Application/8/Home%20%20Entertainment (last visited November 29, 2022).

and by providing technical support and/or related services for these products to purchasers in the United States.

Damages

89. On information and belief, despite having knowledge of the '547 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '547 Patent, NTC has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. NTC's infringing activities relative to the '547 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

90. Polaris has been damaged as a result of NTC's infringing conduct described in this Count. NTC is, thus, liable to Polaris in an amount that adequately compensates Polaris for NTC's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT V

(INFRINGEMENT OF U.S. PATENT NO. 7,532,523)

91. Plaintiff incorporates the preceding paragraphs herein by reference.

92. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

93. Polaris is the owner of all substantial rights, title, and interest in and to the '523 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

94. The ’523 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on May 12, 2009, after full and fair examination.

95. NTC has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the ’523 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, NTC products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the ’523 Patent, including, but not limited to, DDR3 SDRAM (collectively, the “’523 Accused Products”).

Direct Infringement (35 U.S.C. § 271(a))

96. NTC has directly infringed and continues to directly infringe one or more claims of the ’523 Patent in this District and elsewhere in Texas and the United States.

97. NTC has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the ’523 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing, the ’523 Accused Products. Furthermore, NTC makes and sells the ’523 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the ’523 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’523 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, NTC directly infringes the ’523 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including NTC Delaware and NTC U.S.A. Subject to NTC’s direction and control, such subsidiaries conduct activities that constitute direct infringement of the

'523 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '523 Accused Products. NTC receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including NTC Delaware and NTC U.S.A.

98. By way of illustration only, the '523 Accused Products include each and every element of claim 1 of the '523 Patent. The '523 Accused Products include a "memory chip for variably setting terminations" that comprise the limitations of claim 1. For example, the '523 Accused Products comprise "a terminal," shown below in red.

Ball Descriptions

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (when TDQS is enabled via Mode Register A11=1 in MR1) signal for x8
DQ	Input/output	**Data Inputs/Output:** Bi-directional data bus.

Source: Nanya NT5CB(C)256M8JQ/NT5CB(C)128M16JR DDR3(L) SDRAM Datasheet

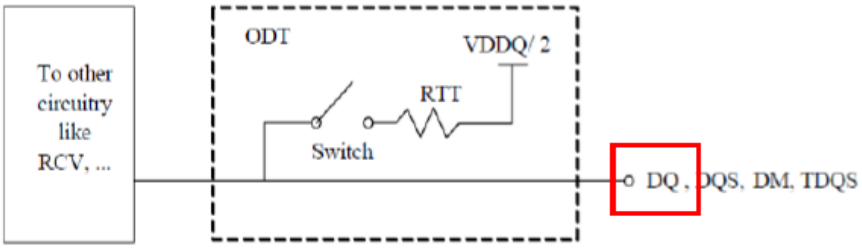
On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3(L) SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{\text{DQS}}$, and DM for x8 configuration (and TDQS, $\overline{\text{TDQS}}$ for x8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. For x16 configuration, ODT is applied to each DQ, DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$, DMU and DMI signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown as below.

Functional Representation of ODT



Source: Nanya NT5CB(C)256M8JQ/NT5CB(C)128M16JR DDR3(L) SDRAM Datasheet

99. The '523 Accused Products comprise "a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value." For example, the termination circuit is coupled to the terminal, shown below in blue.

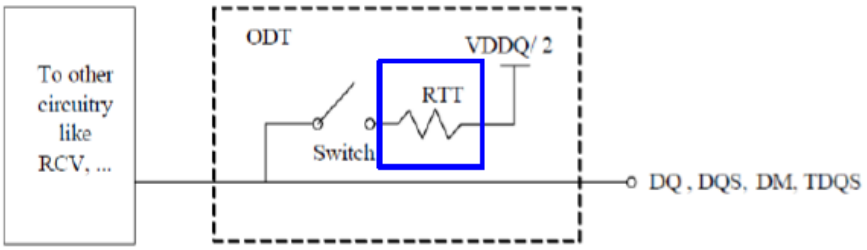
On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3(L) SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{\text{DQS}}$, and DM for x8 configuration (and TDQS, $\overline{\text{TDQS}}$ for x8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. For x16 configuration, ODT is applied to each DQ, DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$, DMU and DMI signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown as below.

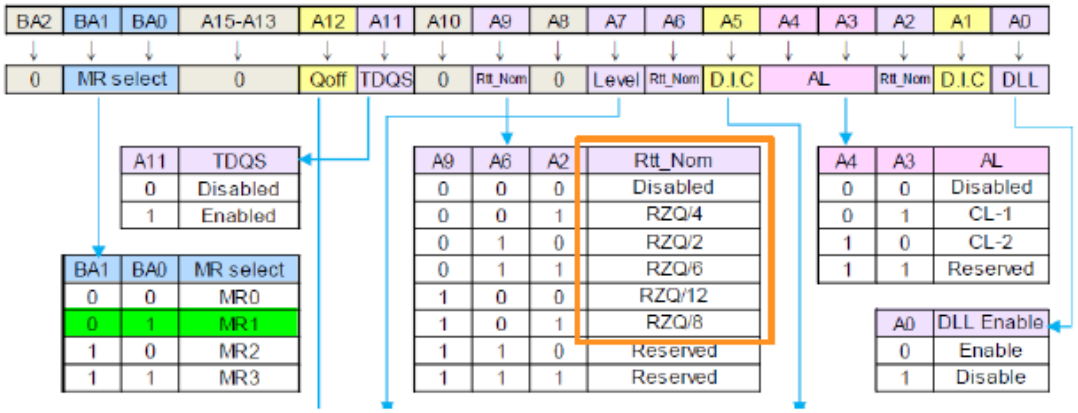
Functional Representation of ODT



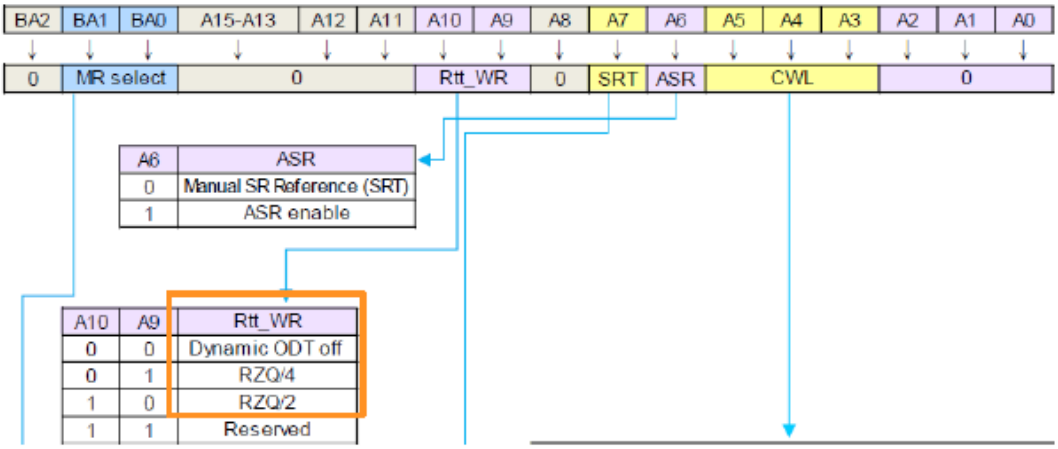
Source: Nanya NT5CB(C)256M8JQ/NT5CB(C)128M16JR DDR3(L) SDRAM Datasheet

Further, the termination circuit is configured to terminate the terminal according to a settable resistance value, shown below in orange.

MR1 Definition



MR2 Definition



Source: Nanya NT5CB(C)256M8JQ/NT5CB(C)128M16JR DDR3(L) SDRAM Datasheet

100. The '523 Accused Products comprise "a control command port for receiving a control command signal for affecting accessibility of the memory chip." For example, the control command port, shown below in purple, is configured to receive a control command signal for affecting accessibility of the memory chip, shown below in green.

Ball Descriptions

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (when TDQS is enabled via Mode Register A11=1 in MR1) signal for x8
DQ	Input/output	**Data Inputs/Output:** Bi-directional data bus.

Source: Nanya NT5CB(C)256M8JQ/NT5CB(C)128M16JR DDR3(L) SDRAM Datasheet

DDR3(L) SDRAM Command Description and Operation

Command Truth Table

Function	Abbr.	CKE		CS	RAS	CAS	WE	BA0-BA2	A13-A14	A12-BC	A10-AP	A0-A9, A11	NOTES
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	

Source: Nanya NT5CB(C)256M8JQ/NT5CB(C)128M16JR DDR3(L) SDRAM Datasheet

101. The '523 Accused Products comprise "a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal," shown below in blue.

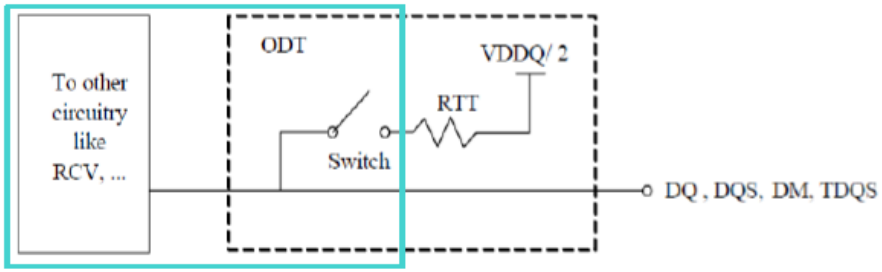
On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3(L) SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{\text{DQS}}$, and DM for x8 configuration (and TDQS, $\overline{\text{TDQS}}$ for x8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. For x16 configuration, ODT is applied to each DQ, DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$, DMU and DMI signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown as below.

Functional Representation of ODT



Source: Nanya NT5CB(C)256M8JQ/NT5CB(C)128M16JR DDR3(L) SDRAM Datasheet

102. The ’523 Accused Products comprise “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal.” For example, the ’523 Accused Products comprise a termination port, shown below in green, configured to receive a termination signal, shown below in red.

Ball Descriptions

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (when TDQS is enabled via Mode Register A11=1 in MR1) signal for x8
DQ	Input/output	**Data Inputs/Output:** Bi-directional data bus.

Source: Nanya NT5CB(C)256M8JQ/NT5CB(C)128M16JR DDR3(L) SDRAM Datasheet

Further, the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal, shown below in blue.

Ball Descriptions

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (when TDQS is enabled via Mode Register A11=1 in MR1) signal for x8
DQ	Input/output	**Data Inputs/Output:** Bi-directional data bus.

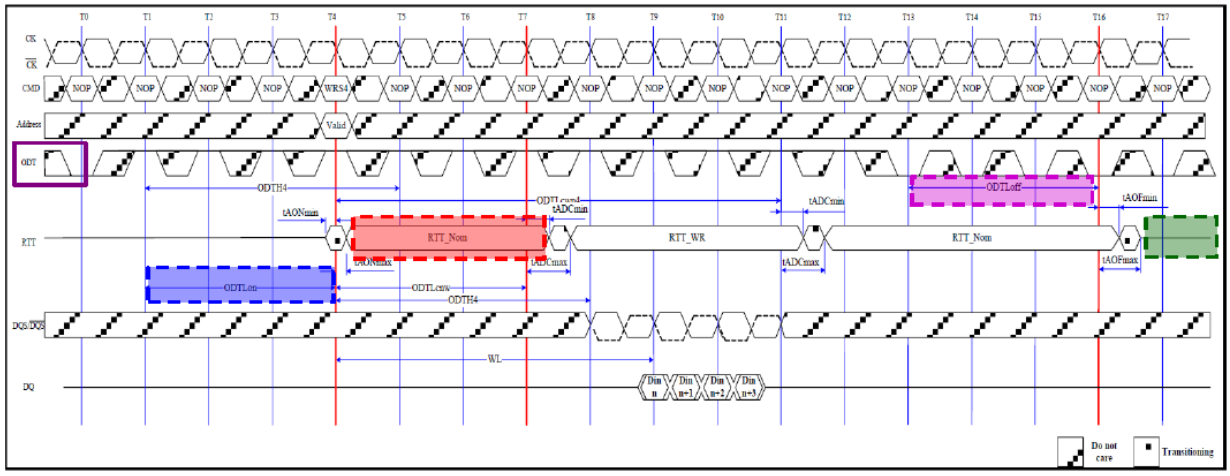
Source: Nanya NT5CB(C)256M8JQ/NT5CB(C)128M16JR DDR3(L) SDRAM Datasheet

103. The '523 Accused Products are configured such that "the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value." For example, as shown below in purple, the control circuit as a function of the termination signal selectively performs one of (i) terminating the terminal with the set resistance value (shown in red) after a first time delay (shown in blue) and (ii) not terminating the terminal (shown in green) in

accordance with a second time delay (shown in pink), the first time delay being sufficiently long to set the resistance value, with the first time delay allowing for the resistance value to be set.

ODT Timing Diagrams

Dynamic ODT: Behavior with ODT being asserted before and after the write



Source: Nanya NT5CB(C)256M8JQ/NT5CB(C)128M16JR DDR3(L) SDRAM Datasheet

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

104. In addition and/or in the alternative to its direct infringements, NTC has indirectly infringed and continues to indirectly infringe one or more claims of the ’523 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’523 Accused Product.

105. At a minimum, NTC has knowledge of the ’523 Patent since being served with this Complaint. NTC also had knowledge of the ’523 Patent since receiving a letter from Polaris providing details of its exemplary infringements prior to the filing of this Complaint. NTC also had knowledge of the ’523 Patent since receiving detailed correspondence from Polaris dated January 20, 2021, alerting NTC to its infringements. Since receiving notice of its infringements, NTC has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C.

§ 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '523 Patent. Indeed, NTC has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '523 Accused Products;[14] creating and/or maintaining established distribution channels for the '523 Accused Products into and within the United States; manufacturing the '523 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '523 Accused Products that promote their features, specifications, and applications;[15] promoting the incorporation of the '523 Accused Products into end-user products,[16] and by providing technical support and/or related services for these products to purchasers in the United States.

Damages

106. On information and belief, despite having knowledge of the '523 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '523 Patent, NTC has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. NTC's infringing activities relative to the '523 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such

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[14] *See, e.g.*, https://www.nanya.com/en/Product/List/450/2249 (last visited November 29, 2022).
[15] *See, e.g.*, https://www.nanya.com/en/Product/4116/NT5CC128M16JR-DIB (last visited November 29, 2022).
[16] *See* https://www.nanya.com/en/Application/8/Home%20%20Entertainment (last visited November 29, 2022).

that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

107. Polaris has been damaged as a result of NTC's infringing conduct described in this Count. NTC is, thus, liable to Polaris in an amount that adequately compensates Polaris for NTC's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT VI

(INFRINGEMENT OF U.S. PATENT NO. of USP 7,772,631)

108. Plaintiff incorporates the preceding paragraphs herein by reference.

109. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

110. Polaris is the owner of all substantial rights, title, and interest in and to the '631 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

111. The '631 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on August 10, 2010, after full and fair examination.

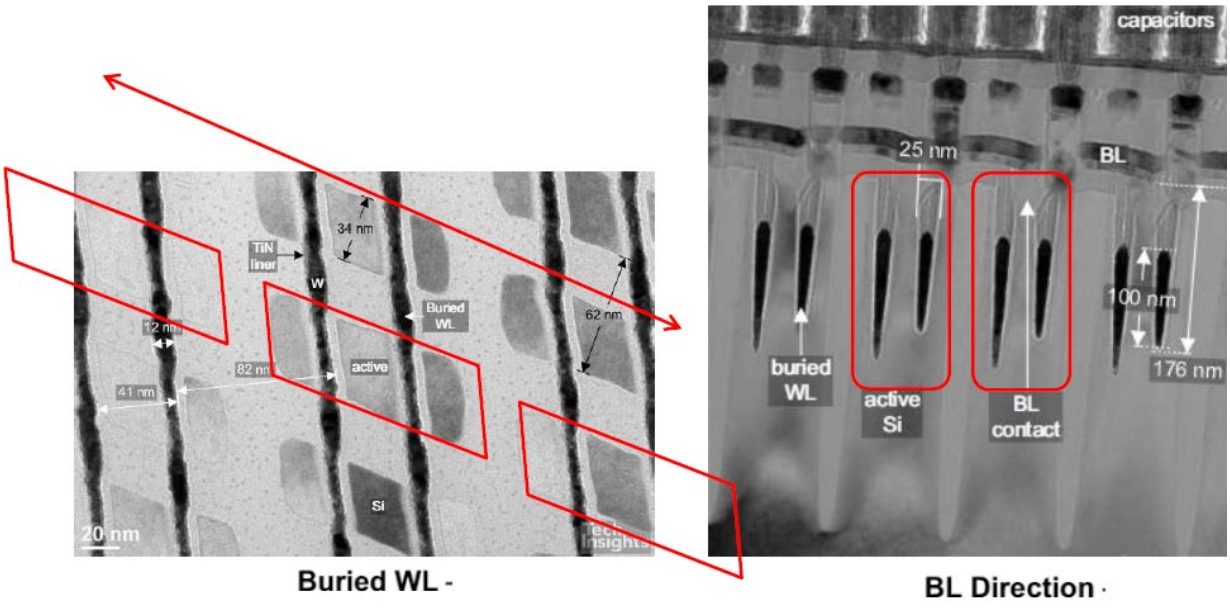
112. NTC has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '631 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, NTC products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '631 Patent, including, but not limited to, its DDR4 SDRAM (collectively, the "'631 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

113. NTC has directly infringed and continues to directly infringe one or more claims of the '631 Patent in this District and elsewhere in Texas and the United States.

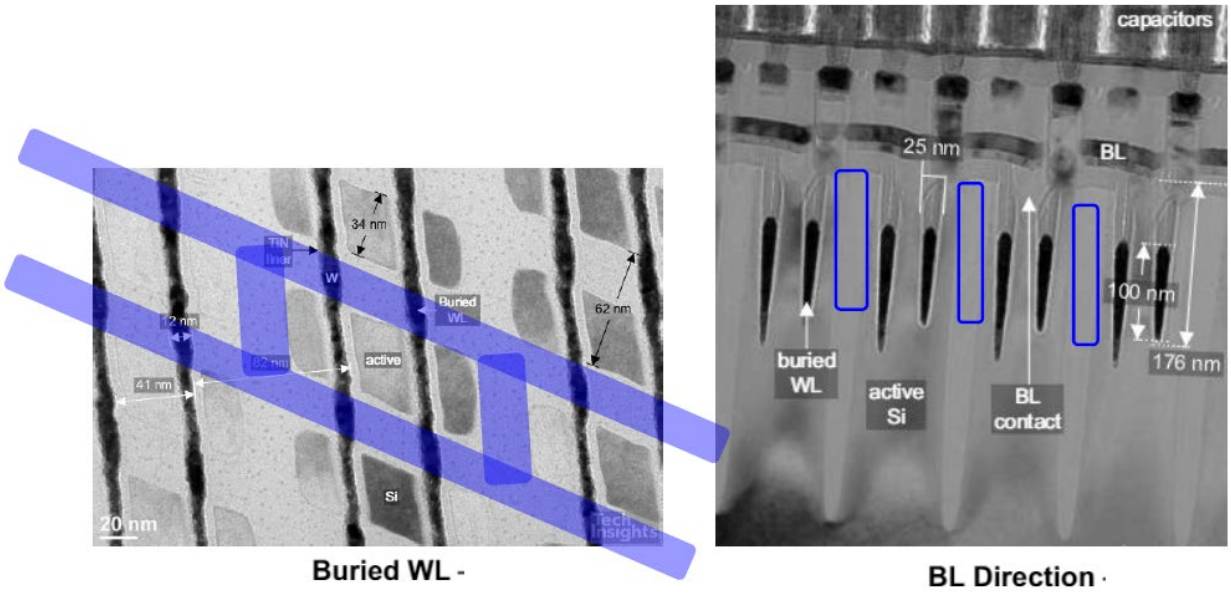
114. NTC has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the '631 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '631 Accused Products. Furthermore, NTC makes and sells the '631 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '631 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '631 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, NTC directly infringes the '631 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including NTC Delaware and NTC U.S.A. Subject to NTC's direction and control, such subsidiaries conduct activities that constitute direct infringement of the '631 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '631 Accused Products. NTC receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including NTC Delaware and NTC U.S.A.

115. By way of illustration only, the '631 Accused Products include each and every element of claim 1 of the '631 Patent. The '631 Accused Products include "[a]n integrated circuit having a memory cell arrangement with a folded bit line arrangement" that comprise the limitations of claim 1. For example, the '631 Accused Products comprise "a plurality of active regions along a first direction in a semiconductor body," as shown with the red boxes and line below:



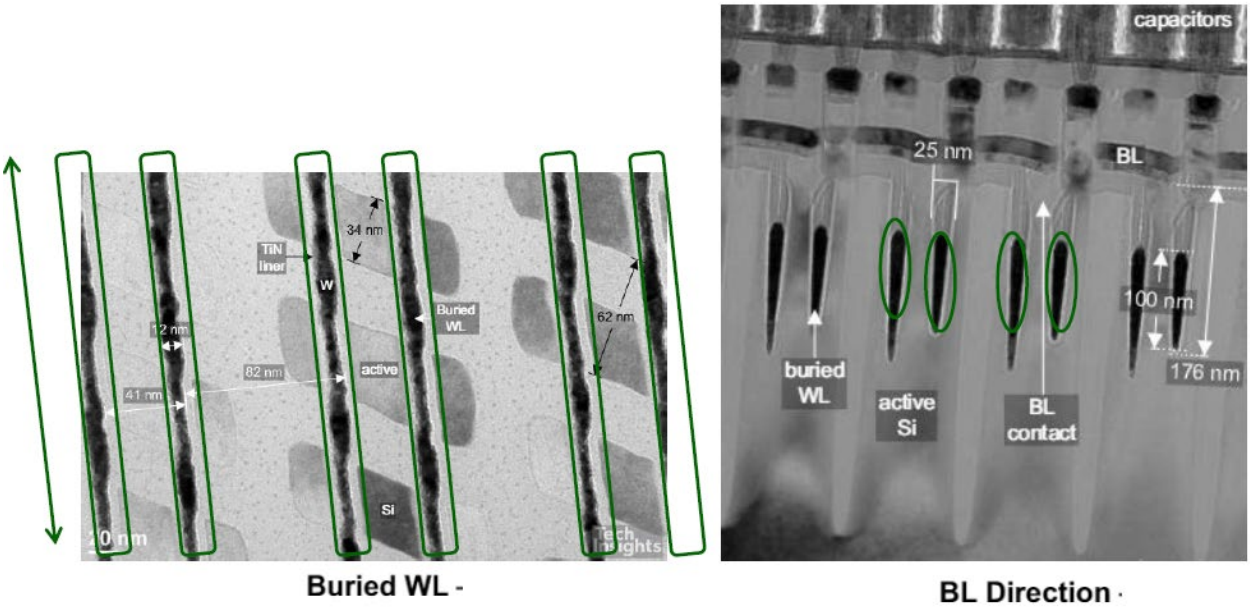
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

116. The '631 Accused Products comprise "the active regions being surrounded by isolation trenches on all sides." For example, in the '631 Accused Products the active regions are surrounded by isolation trenches on all sides, as shown with the blue boxes below:



Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

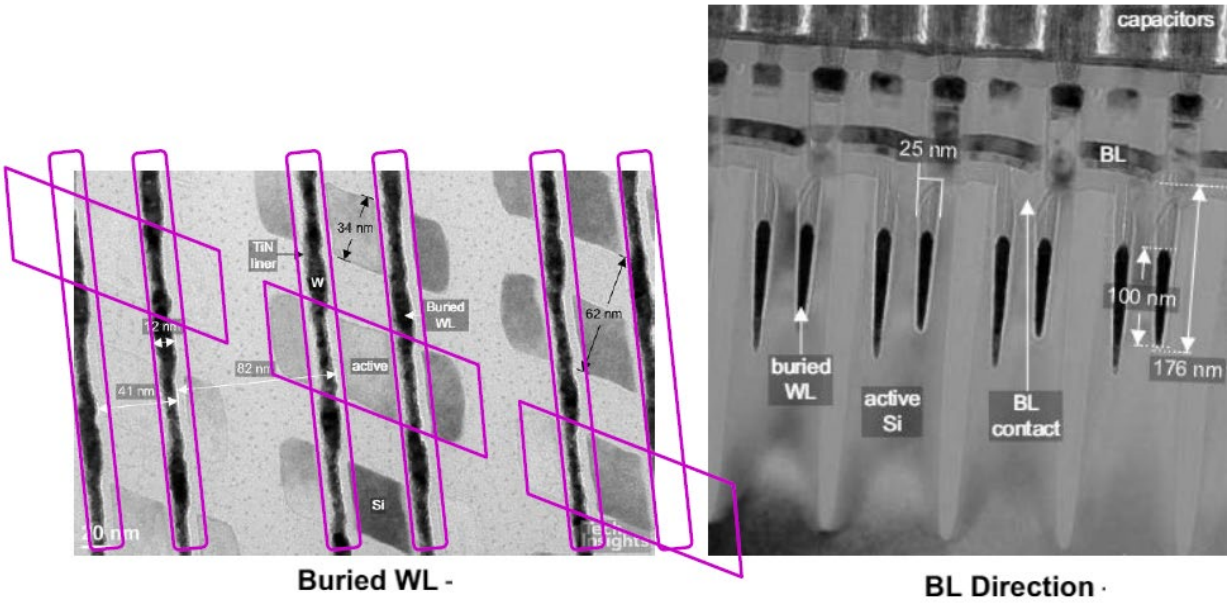
117. The ’631 Accused Products comprise “a plurality of parallel buried word lines along a second direction in the semiconductor body.” For example, the ’631 Accused Products comprise a plurality of parallel buried word lines along a second direction in the semiconductor body, as shown in dark green below:



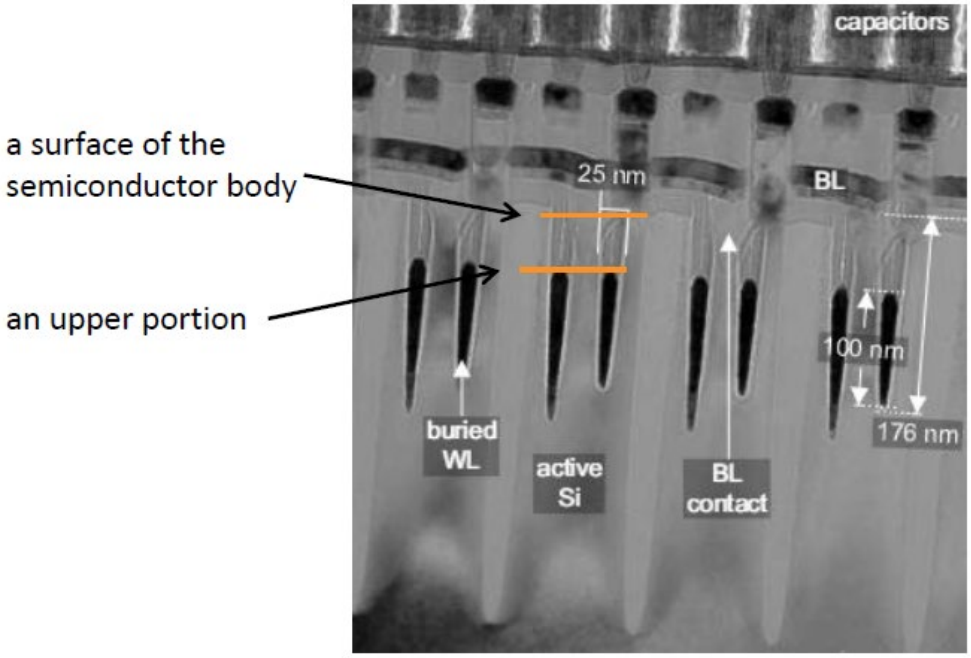
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

118. The ’631 Accused Products comprise “the buried word lines running through the active regions and having an upper portion below a surface of the semiconductor body, where two of the buried word lines are spaced apart from one another and from the isolation trenches running through a respective active region, and the buried word lines being insulated from a channel region in the respective active region by a gate dielectric layer.” For example, the ’631 Accused Products comprise the buried word lines running through the active regions (purple boxes) and having an upper portion below a surface of the semiconductor body (orange lines), where two of the buried word lines are spaced apart from one another (aqua arrows) and from the isolation trenches running through a respective active region (green arrows), and the buried word lines being insulated from

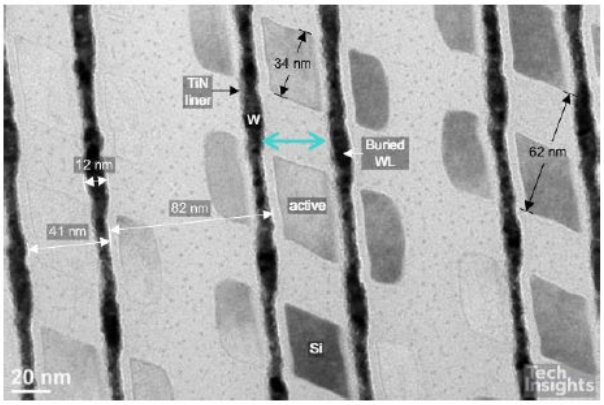
a channel region in the respective active region by a gate dielectric layer (red boxes), as shown below:



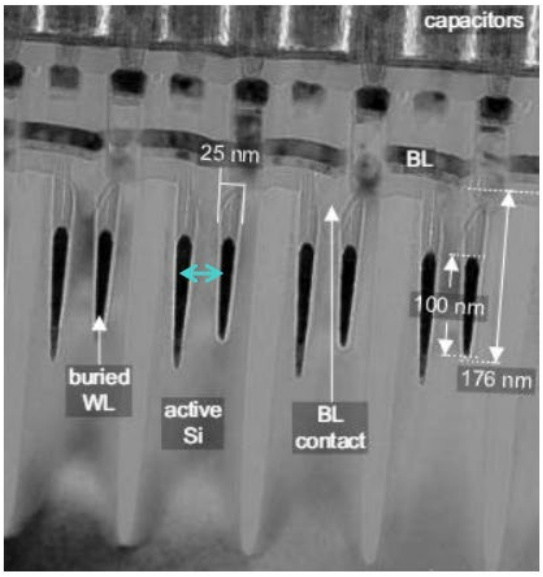
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28



Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 28

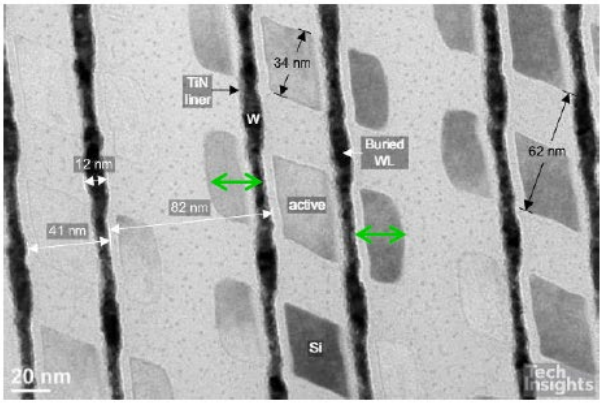


Buried WL -

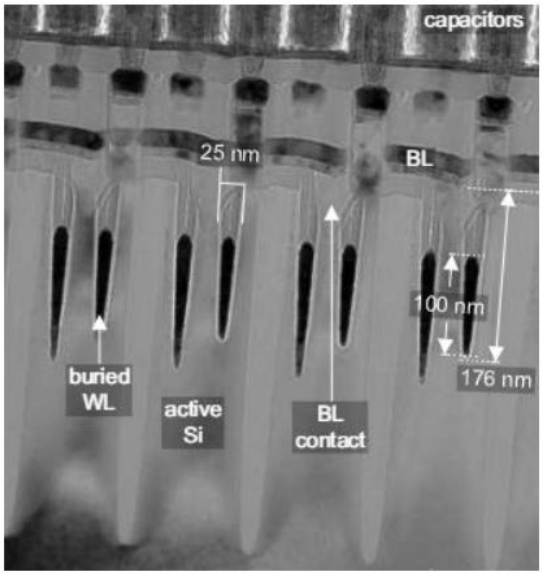


BL Direction ·

Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

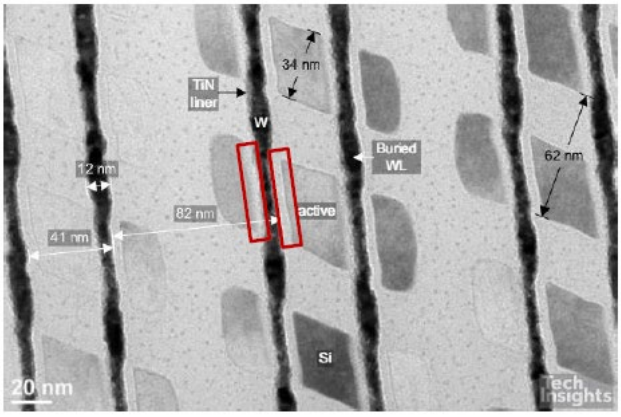


Buried WL -

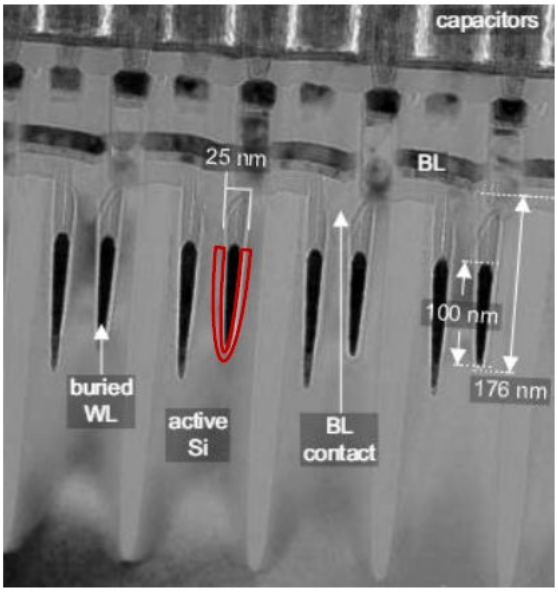


BL Direction ·

Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28



Buried WL -

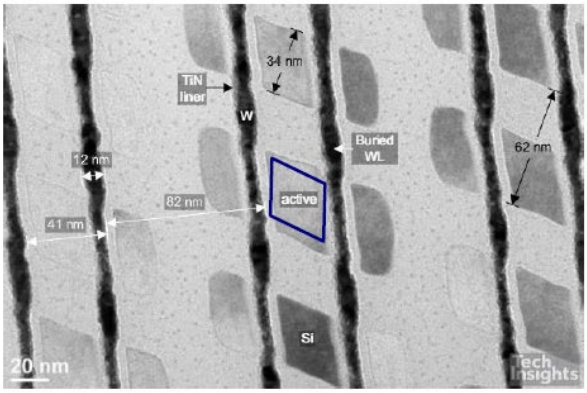


BL Direction

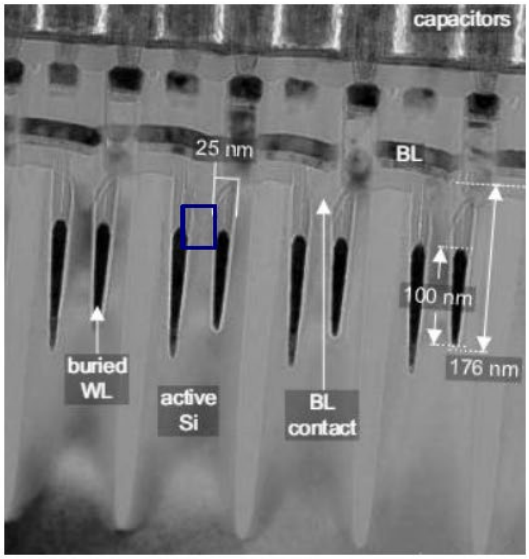
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

119. The '631 Accused Products comprise "a source region between the two buried word lines." For example, the '631 Accused Products comprise a source region between the two buried word lines, as shown in the blue boxes below:

a source region between the two buried word lines;



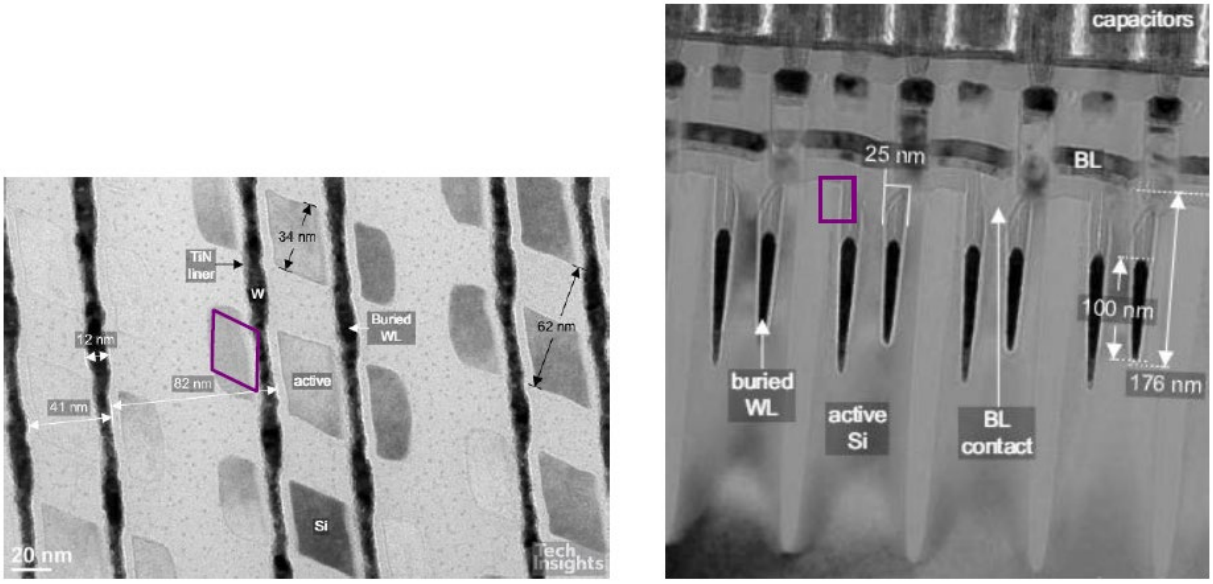
Buried WL -



BL Direction ·

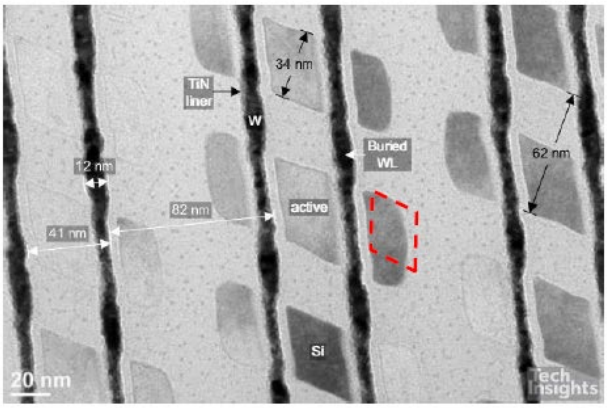
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

120. The '631 Accused Products comprise "a first drain region between one of the two buried word lines and an isolation trench portion." For example, the '631 Accused Products comprise a first drain region between one of the two buried word lines and an isolation trench portion, as shown in the purple boxes below:

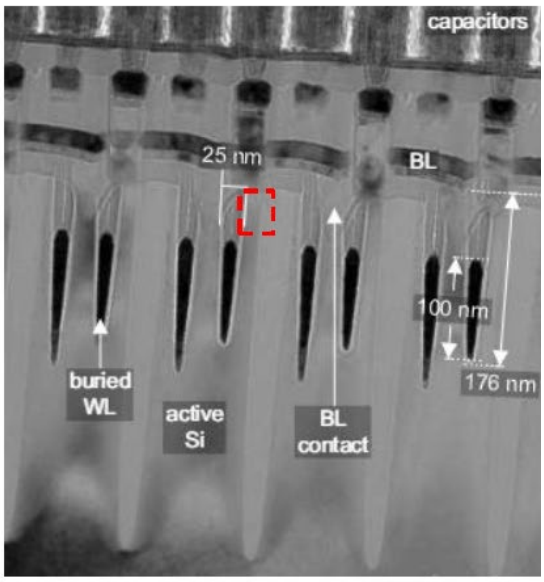


Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

121. The '631 Accused Products comprise "a second drain region between the other of the two buried word lines and another isolation trench portion." For example, the '631 Accused Products comprise a second drain region between the other of the two buried word lines and another isolation trench portion, as shown in the red dashed box below:



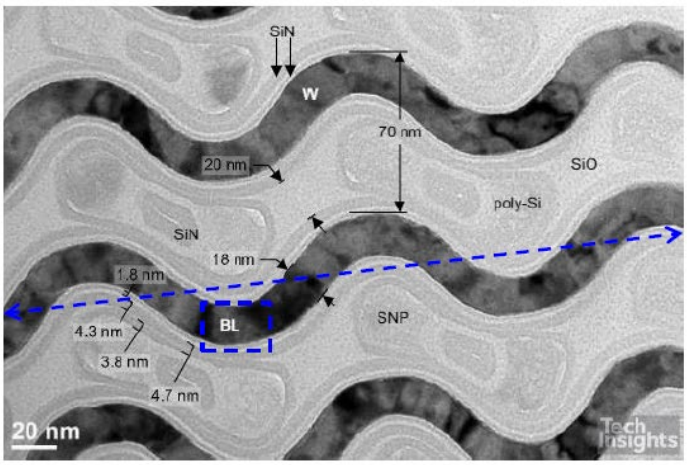
Buried WL -

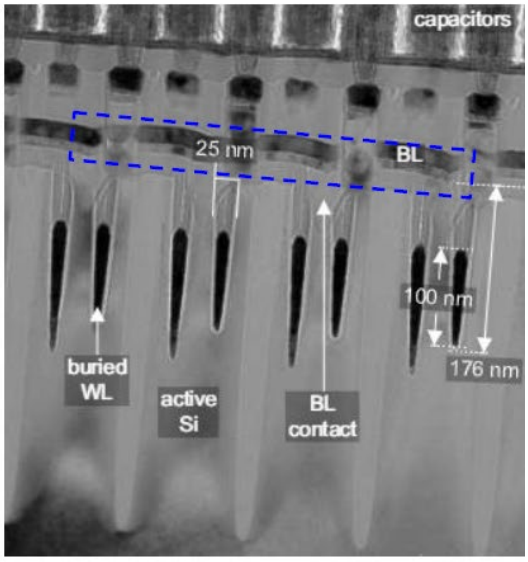


BL Direction ·

Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

122. The '631 Accused Products comprise "a plurality of parallel bit lines along a third direction at the surface of the semiconductor body." For example, the '631 Accused Products comprise a plurality of parallel bit lines along a third direction (blue dashed line and box) at the surface of the semiconductor body, as shown below:

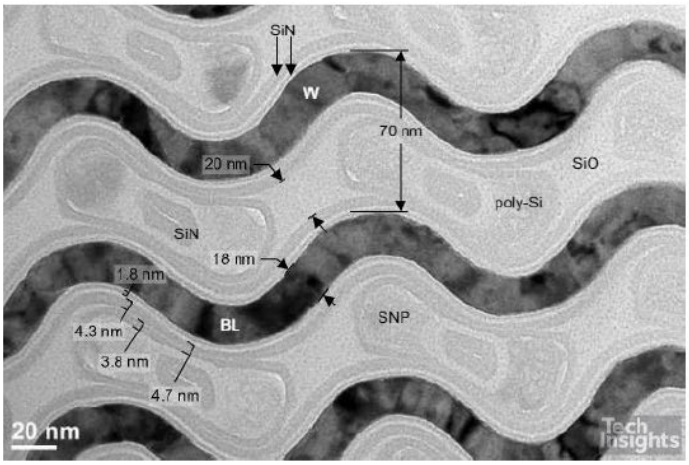


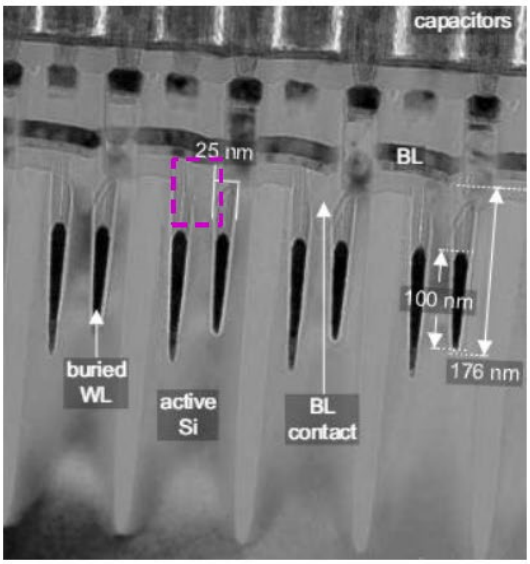


BL Direction ·

Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 26, 28

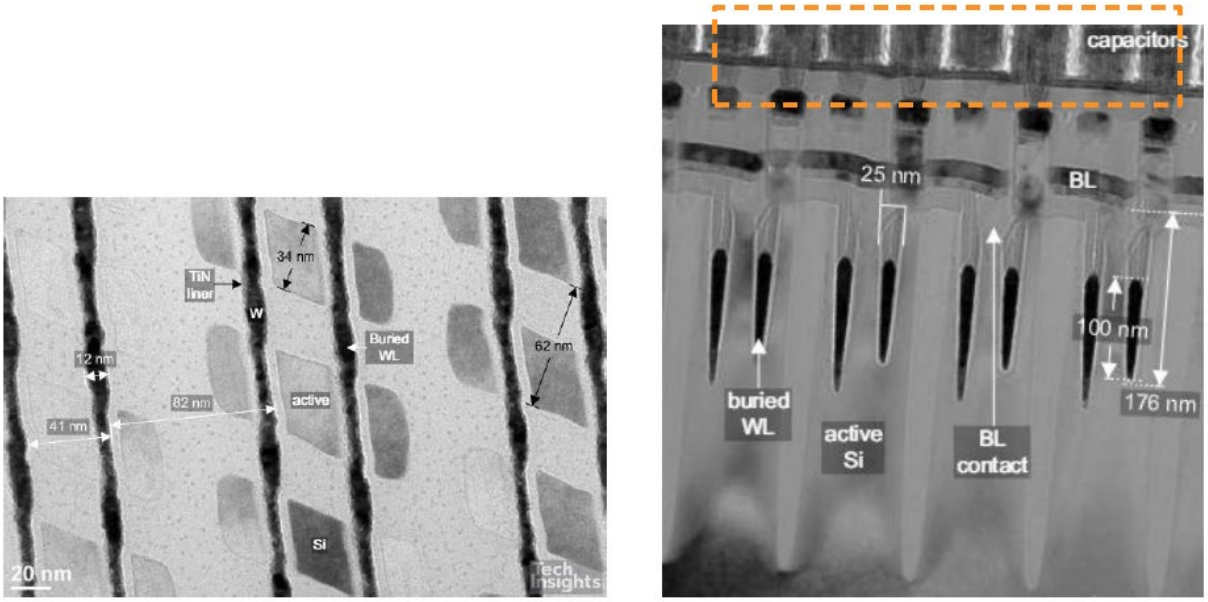
123. In the ’631 Accused Products, “a bit line makes contact with the source region.” For example, in the ’631 Accused Products, a bit line makes contact with the source region, as shown in the purple dashed box below:





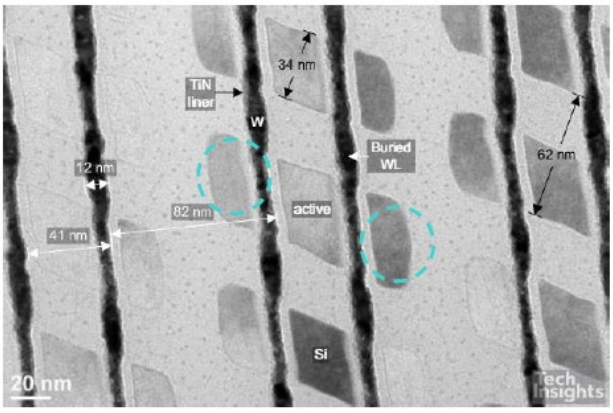
Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 26, 28

124. The ’631 Accused Products comprise “a plurality of storage capacitors.” For example, the ’631 Accused Products comprise a plurality of storage capacitors, as shown in the orange dashed box below:

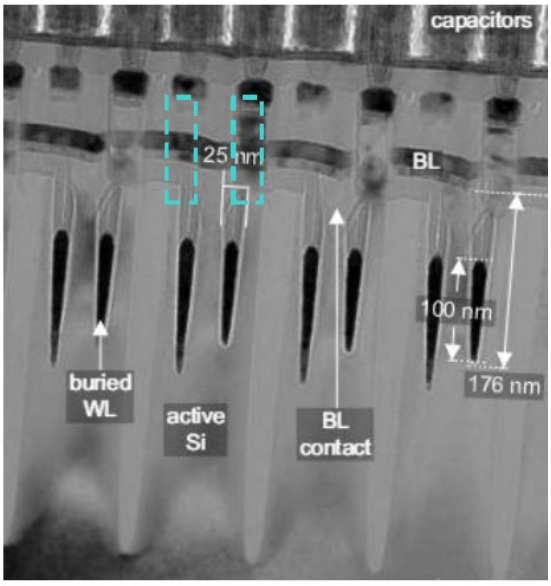


Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

125. The '631 Accused Products comprise "a first and second storage capacitor of the plurality of storage capacitors being connected to the first and second drain regions, respectively." For example, the '631 Accused Products comprise a first and second storage capacitor of the plurality of storage capacitors being connected to the first and second drain regions, respectively, as shown in the aqua dashed boxes and circles below:



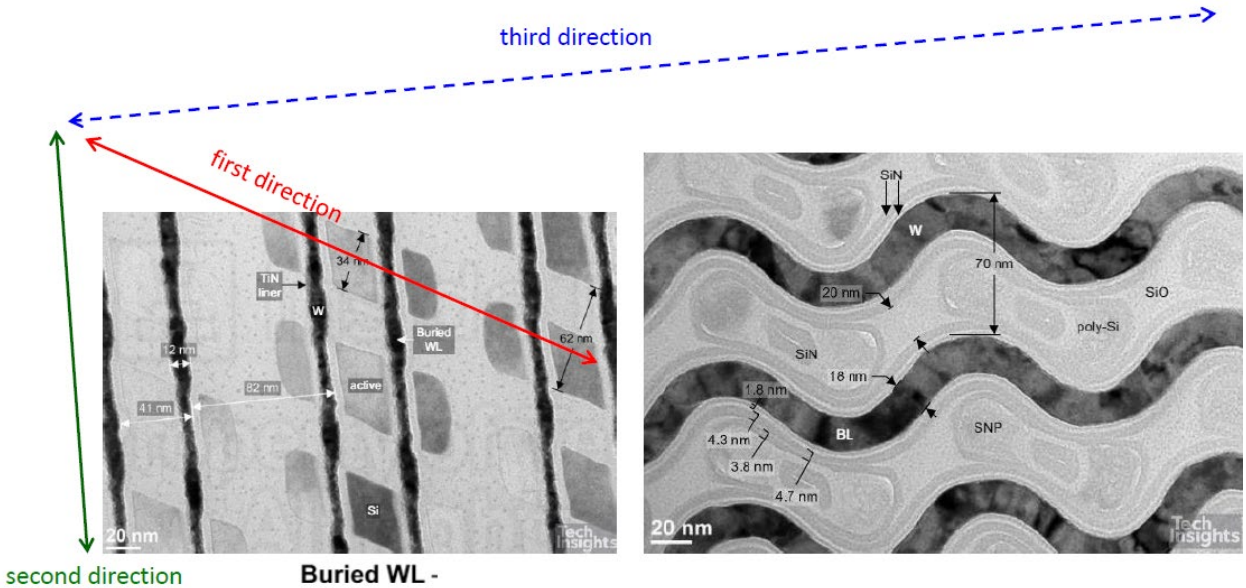
Buried WL -



BL Direction

Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 28

126. In the '631 Accused Products, "the first direction is diagonal to the second and third directions." For example, in the '631 Accused Products, the first direction is diagonal to the second and third directions, as shown below:



Buried WL -

Source: Nanya NT5AD512M16A4-HR 20 nm 8Gb DDR4 SDRAM Advanced Memory Essentials, TechInsights, Page 30, 26

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

127. In addition and/or in the alternative to its direct infringements, NTC has indirectly infringed and continues to indirectly infringe one or more claims of the '631 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '631 Accused Products.

128. At a minimum, NTC has knowledge of the '631 Patent since being served with this Complaint. NTC also had knowledge of the '631 Patent since receiving a letter from Polaris providing details of its exemplary infringements prior to the filing of this Complaint. NTC also had knowledge of the '631 Patent since receiving detailed correspondence from Polaris dated November 1, 2021, alerting NTC to its infringements. Since receiving notice of its infringements, NTC has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '631 Patent. Indeed, NTC has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '631 Accused Products;[17] creating and/or maintaining established distribution channels for the '631 Accused Products into and within the United States; manufacturing the '631 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '631 Accused

[17] *See, e.g.*, https://www.nanya.com/en/Product/List/450/2264 (last visited November 29, 2022).

Products that promote their features, specifications, and applications;[18] promoting the incorporation of the '631 Accused Products into end-user products,[19] and by providing technical support and/or related services for these products to purchasers in the United States.

Damages

129. On information and belief, despite having knowledge of the '631 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '631 Patent, NTC has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. NTC's infringing activities relative to the '631 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

130. Polaris has been damaged as a result of NTC's infringing conduct described in this Count. NTC is, thus, liable to Polaris in an amount that adequately compensates Polaris for NTC's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

CONCLUSION

131. Polaris is entitled to recover from NTC the damages sustained by Polaris as a result of NTC's wrongful acts, and willful infringements, in an amount subject to proof at trial, which,

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[18] *See, e.g.*, https://www.nanya.com/en/Product/4467/NT5AD2048M4C3-JR (last visited November 29, 2022).

[19] *See* https://www.nanya.com/en/Application/8/Home%20%20Entertainment (last visited November 29, 2022).

by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

132. Polaris has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute may give rise to an exceptional case within the meaning of 35 U.S.C. § 285, and Polaris is entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

JURY DEMAND

133. Polaris hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

PRAYER FOR RELIEF

134. Polaris respectfully requests that the Court find in its favor and against NTC, and that the Court grant Polaris the following relief:

(i) A judgment that one or more claims of the Asserted Patents have been infringed, either literally and/or under the doctrine of equivalents, by Defendant

(ii) A judgment that one or more claims of the Asserted Patents have been willfully infringed, either literally and/or under the doctrine of equivalents, by Defendant;

(iii) A judgment that Defendant account for and pay to Plaintiff all damages and costs incurred by Plaintiff because of Defendant's infringing activities and other conduct complained of herein, including an accounting for any sales or damages not presented at trial;

(iv) A judgment that Defendant account for and pay to Plaintiff a reasonable, ongoing, post judgment royalty because of Defendant's infringing activities, including continuing infringing activities, and other conduct complained of herein;

(v) A judgment that Plaintiff be granted pre-judgment and post judgment interest on the damages caused by Defendant's infringing activities and other conduct complained of herein;

(vi) A judgment that this case is exceptional under the provisions of 35 U.S.C. § 285 and award enhanced damages; and

(vii) Such other and further relief as the Court deems just and equitable.

Dated: February 6, 2023

Respectfully submitted,

/s/ Edward R. Nelson III

Edward R. Nelson III
Lead Attorney
State Bar No. 00797142 Nelson Bumgardner Conroy PC 3131 West 7th Street, Suite 300 Fort Worth, Texas 76107
Tel: (817) 377-9111
ed@nelbum.com
Ryan P. Griffin
State Bar No. 24053687
Jonathan H. Rastegar
State Bar No. 24064043 David T. DeZern
State Bar No. 24059677 Nelson Bumgardner Conroy PC 2727 N. Harwood St., Suite 250
Dallas, TX 75201
Tel: (214) 446-4950
ryan@nelbum.com
jon@nelbum.com
david@nelbum.com

Attorneys for Plaintiff Polaris Innovations Limited