IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SYNOPSYS, INC. and CADENCE DESIGN SYSTEMS, INC.,	)	
Plaintiffs,	)	
v.	)	C.A. No. _____
BELL SEMICONDUCTOR, LLC,	)	DEMAND FOR JURY TRIAL
Defendant.	)	

COMPLAINT FOR DECLARATORY JUDGMENT

Plaintiffs Synopsys, Inc. ("Synopsys") and Cadence Design Systems, Inc. ("Cadence") (collectively, "Plaintiffs") bring this Complaint against Defendant Bell Semiconductor, LLC ("BSLLC" or "Defendant"). In support of this Complaint for Declaratory Judgment, Plaintiffs allege as follows:

NATURE OF THE ACTION

1. This is an action for declaratory judgment of non-infringement and invalidity of U.S. Patent Nos. 7,007,259 ("the '259 patent"), 6,436,807 ("the '807 patent"), 7,396,760 ("the '760 patent"), 7,260,803 ("the '803 patent"), 7,231,626 ("the '626 patent"), and 7,149,989 ("the '989 patent") (collectively, "Asserted Patents") under the Federal Declaratory Judgment Act, 28 U.S.C. §§ 2201 and 2202, and the patent laws of the United States, 35 U.S.C. § 1 et seq., and for other relief the Court deems just and proper. This lawsuit follows a sprawling litigation campaign BSLLC has initiated against Plaintiffs' customers in which BSLLC alleges that the customers' use of certain of Plaintiffs' software products infringes six BSLLC patents, *i.e.*, the Asserted Patents.

2. Plaintiffs Synopsys and Cadence are the two largest suppliers of Electronic Design Automation ("EDA") software tools in the world. Engineers use Plaintiffs' EDA design tools to design, develop and test semiconductor chips. Since the 1980s, engineers around the world have used Plaintiffs' EDA design tools to design billions of semiconductor chips used in electronic devices that enable communications, computing, healthcare, military systems, transportation, clean energy, and countless other applications. BSLLC alleges that certain tasks performed by place-and-route and physical verification EDA design tools infringe the Asserted Patents.

3. Synopsys' IC Compiler and IC Compiler II products (collectively, "IC Compiler") and Cadence's Innovus and Virtuoso products provide customers with a comprehensive place-and-route system that, among other things, determines where each gate should be located on the physical chip (the placement portion of place-and-route), and routes wires between different elements on the chip while minimizing wire delay (the route portion of place-and-route). Synopsys' predecessor product to IC Compiler, Astro, also provided customers with a comprehensive place-and-route system.

4. Synopsys' IC Validator physical verification product, and Cadence's Pegasus and PVS physical verification products, provide semiconductor designers with metal fill, Design Rule Checking ("DRC"), Layout Vs. Schematic ("LVS") features, pattern matching, and Electrical Rule Checking ("ERC") features. Synopsys' predecessor product to IC Validator, Hercules, also provided DRC, LVS, electrical rule checking and metal fill generation features.

5. Synopsys' IC Validator product can also be used in conjunction with IC Compiler, allowing signoff quality checking to occur during the implementation phase of

semiconductor design, as well as user friendly DRC, and signoff metal fill generation in an interface familiar to the place-and-route engineer.

6. Cadence's Pegasus and PVS products can be used in conjunction with Cadence's Innovus and Virtuoso products, allowing signoff quality checking to occur during the implementation phase of semiconductor design, as well as user friendly DRC, and signoff metal fill generation in an interface familiar to the place-and-route engineer.

7. Plaintiffs' customers are among the world's most innovative companies, who create the semiconductor chips that power cellular communications, computers, computer networks, medical devices, automobiles, aerospace and military equipment, satellites, industrial and manufacturing equipment, consumer electronics, household appliances, healthcare systems, and much more. All of the companies BSLLC has sued for infringement of the Asserted Patents are customers of one or both of the Plaintiffs: Ambarella, Advanced Micro Devices ("AMD"), Ampere Computing, Analog Devices ("ADI"), ASMedia Technology, Infineon, Kioxia, Lattice Semiconductor, MACOM, Marvell, Maxlinear, Micron, NVIDIA, NXP, Omnivision, ams-OSRAM, Phison Electronics, Qualcomm, Rockchip Electronics, Sequans Communications, Silicon Laboratories, Skyworks Solutions, Socionext, and Western Digital (collectively, "Customers").

8. BSLLC is a patent monetization entity and wholly owned subsidiary of Hilco IP Merchant Capital, LLC, the "IP Monetization" arm of Hilco Global, an international financial services company. On information and belief, BSLLC neither makes products nor invests in research & development. BSLLC's business is litigation. On information and belief, BSLLC is the owner by assignment of the Asserted Patents.

9. As part of its litigation campaign against the semiconductor industry, BSLLC has sued twenty-five of Plaintiffs' Customers in eighty-seven cases pending in over a dozen different federal jurisdictions. BSLLC has continually filed new federal lawsuits in a piecemeal fashion, bringing new allegations of infringement of one or more of the Asserted Patents against Plaintiffs' customers over the past six months.

10. A list of the current district court cases brought by BSLLC involving the Asserted Patents, identified by case name, date filed, the specific Asserted Patents BSLLC asserts in each case, and the presiding judge is as follows (collectively, "District Court Customer Suits"):

	Case (Including party, case number and jurisdiction)	Filing Date	Patents-In-Suit	Judge
1	Bell Semiconductor, LLC v. Advanced Micro Devices, Inc. 1-22-cv-10632 (DMA)	4/27/2022	6436807 7007259	Hon. Angel Kelley
2	Bell Semiconductor, LLC v. Advanced Micro Devices, Inc. 1-22-cv-11383 (DMA)	8/26/2022	7149989 7260803	Hon. Angel Kelley
3	Bell Semiconductor, LLC v. Advanced Micro Devices, Inc. 1-22-cv-11696 (DMA)	10/5/2022	7231626	Hon. Angel Kelley
4	Bell Semiconductor, LLC v. Advanced Micro Devices, Inc. 1-22-cv-11783 (DMA)	10/18/2022	7396760	Hon. Leo T. Sorokin
5	Bell Semiconductor, LLC v. Ambarella, Inc. 3-22-cv-00245 (SDOH)	8/26/2022	7149989 7260803	Hon. Walter H. Rice
6	Bell Semiconductor, LLC v. Ambarella, Inc. 3-22-cv-00273 (SDOH)	9/23/2022	6436807 7007259	Hon. Michael J. Newman
7	Bell Semiconductor, LLC v. Ambarella, Inc. 3-22-cv-00323 (SDOH)	11/11/2022	7231626 7396760	Hon. Thomas M. Rose

	Case (Including party, case number and jurisdiction)	Filing Date	Patents-In-Suit	Judge
8	Bell Semiconductor, LLC v. Ampere Computing, LLC 3-22-cv-01280 (DOR)	8/26/2022	7149989 7260803	Hon. Michael W. Mosman
9	Bell Semiconductor, LLC v. Ampere Computing, LLC 3-22-cv-01435 (DOR)	9/22/2022	6436807 7007259	Hon. Michael W. Mosman
10	Bell Semiconductor, LLC v. ams-OSRAM AG d/b/a ams OSRAM Automotive Lighting Systems USA, Inc. 2-22-cv-12017 (EDMI)	8/26/2022	7149989 7260803	Hon. Gershwin A. Drain
11	Bell Semiconductor, LLC v. ams-OSRAM AG 2-22-cv-11857 (EDMI)	8/11/2022	6436807 7007259	Hon. Gershwin A. Drain
12	Bell Semiconductor, LLC v. ams-OSRAM AG 2-22-cv-12518 (EDMI)	10/20/2022	7231626 7396760	Hon. Linda V. Parker
13	Bell Semiconductor, LLC v. Analog Devices, Inc 1-22-cv-11384 (DMA)	8/26/2022	7149989 7260803	Hon. Nathaniel M. Gorton
14	Bell Semiconductor, LLC v. Analog Devices, Inc. 1-22-cv-10633 (DMA)	4/27/2022	6436807 7007259	Hon. F. Dennis Saylor, IV
15	Bell Semiconductor, LLC v. Analog Devices, Inc. 1-22-cv-11718 (DMA)	10/11/2022	7396760	Hon. F. Dennis Saylor, IV
16	Bell Semiconductor, LLC v. Analog Devices, Inc. 1-22-cv-11901 (DMA)	11/10/2022	7231626	Hon. Judith G. Dein
17	Bell Semiconductor, LLC v. ASMedia Technology, Inc. 1-22-cv-07307 (SDNY)	8/26/2022	7149989 7260803	Hon. Lorna G. Schofield
18	Bell Semiconductor, LLC v. ASMedia Technology, Inc. 1-22-cv-08166 (SDNY)	9/23/2022	6436807 7007259	Hon. Lewis J. Liman

	Case (Including party, case number and jurisdiction)	Filing Date	Patents-In-Suit	Judge
19	Bell Semiconductor, LLC v. ASMedia Technology, Inc. 1-22-cv-09260 (SDNY)	10/28/2022	7231626 7396760	Hon. Valerie E. Caproni
20	Bell Semiconductor, LLC v. Infineon Technologies America Corp. 1-22-cv-11698 (DMA)	10/5/2022	7231626	Hon. M. Page Kelley
21	Bell Semiconductor, LLC v. Infineon Technologies America Corporation 1-22-cv-10634 (DMA)	4/27/2022	6436807 7007259	Hon. Allison D. Burroughs
22	Bell Semiconductor, LLC v. Infineon Technologies America Corporation 1-22-cv-11385 (DMA)	8/26/2022	7149989 7260803	Hon. F. Dennis Saylor, IV
23	Bell Semiconductor, LLC v. Infineon Technologies America Corporation 1-22-cv-11926 (DMA)	11/13/2022	7396760	Hon. Leo T. Sorokin
24	Bell Semiconductor, LLC v. Kioxia America, Inc. 2-22-cv-00726 (EDCA)	4/27/2022	7007259	Hon. Kimberly J. Mueller
25	Bell Semiconductor, LLC v. Kioxia America, Inc. 2-22-cv-01510 (EDCA)	8/26/2022	7149989 7260803	Hon. William B. Shubb
26	Bell Semiconductor, LLC v. Kioxia Corporation et al 2-22-cv-01797 (EDCA)	10/7/2022	7396760	Hon. William B. Shubb
27	Bell Semiconductor, LLC v. Kioxia Corporation et al 2-22-cv-01880 (EDCA)	10/20/2022	7231626 6436807	Hon. Kimberly J. Mueller
28	Bell Semiconductor, LLC v. Lattice Semiconductor Corporation 3-22-cv-01437 (DOR)	9/22/2022	6436807 7007259	Hon. Karin J. Immergut

	Case (Including party, case number and jurisdiction)	Filing Date	Patents-In-Suit	Judge
29	Bell Semiconductor, LLC v. Lattice Semiconductor Corporation 3-22-cv-01542 (DOR)	10/13/2022	7231626	Hon. Stacie F. Beckerman
30	Bell Semiconductor, LLC v. Lattice Semiconductor Corporation 3-22-cv-01543 (DOR)	10/13/2022	7396760	Hon. Marco A. Hernandez
31	Bell Semiconductor, LLC v. Lattice Semiconductor, Inc. 3-22-cv-01282 (DOR)	8/26/2022	7149989 7260803	Hon. Michael W. Mosman
32	Bell Semiconductor, LLC v. MACOM Technology Solutions Inc. 1-22-cv-11290 (DMA)	8/11/2022	7007259	Hon. Denise J. Casper
33	Bell Semiconductor, LLC v. MACOM Technology Solutions Inc. 1-22-cv-11386 (DMA)	8/26/2022	7149989 7260803	Hon. Patti B. Saris
34	Bell Semiconductor, LLC v. MACOM Technology Solutions Inc. 1-22-cv-11719 (DMA)	10/11/2022	7396760	Hon. Nathaniel M. Gorton
35	Bell Semiconductor, LLC v. MACOM Technology Solutions Inc. 1-22-cv-11788 (DMA)	10/19/2022	7231626 6436807	Hon. Leo T. Sorokin
36	Bell Semiconductor, LLC v. Marvell Semiconductor, Inc. 4-22-cv-11721 (DMA)	10/11/2022	7396760	Hon. Denise J. Casper
37	Bell Semiconductor, LLC v. Marvell Technology Group, Ltd. et al. 4-22-cv-10635 (DMA)	4/27/2022	6436807 7007259	Hon. Denise J. Casper
38	Bell Semiconductor, LLC v. Marvell Technology Group, Ltd.	8/26/2022	7149989 7260803	Hon. F. Dennis Saylor, IV

	Case (Including party, case number and jurisdiction)	Filing Date	Patents-In-Suit	Judge
	et al. 4-22-cv-11387 (DMA)			
39	Bell Semiconductor, LLC v. Marvell Technology Group, Ltd. et al. 4-22-cv-11906 (DMA)	11/10/2022	6436807 7231626	**N/A** (11/12)
40	Bell Semiconductor, LLC v. Maxlinear, Inc. 3-22-cv-01178 (SDCA)	8/11/2022	7007259 6436807	Hon. Cynthia Bashant
41	Bell Semiconductor, LLC v. Maxlinear, Inc. 3-22-cv-01268 (SDCA)	8/26/2022	7149989 7260803	Hon. Linda Lopez
42	Bell Semiconductor, LLC v. Maxlinear, Inc. 3-22-cv-01537 (SDCA)	10/7/2022	7396760	Hon. Ruth Bermudez Montenegro
43	Bell Semiconductor, LLC v. Micron Technology, Inc. 1-22-cv-00192 (DID)	4/27/2022	6436807 7007259	Hon. David C. Nye
44	Bell Semiconductor, LLC v. Micron Technology, Inc. 1-22-cv-00375 (DID)	8/26/2022	7149989 7260803	Hon. David C. Nye
45	Bell Semiconductor, LLC v. Micron Technology, Inc. 1-22-cv-00417 (DID)	10/5/2022	7231626	Hon. David C. Nye
46	Bell Semiconductor, LLC v. Micron Technology, Inc. 1-22-cv-00438 (DID)	10/18/2022	7396760	Hon. David C. Nye
47	Bell Semiconductor, LLC v. NVIDIA Corporation 4-22-cv-10636 (DMA)	4/27/2022	7007259	Hon. Allison D. Burroughs
48	Bell Semiconductor, LLC v. Nvidia Corporation 4-22-cv-11388 (DMA)	8/26/2022	7149989 7260803	Hon. Denise J. Casper
49	Bell Semiconductor, LLC v. NVIDIA Corporation 4-22-cv-11700 (DMA)	10/5/2022	7231626	Hon. Angel Kelley

	Case (Including party, case number and jurisdiction)	Filing Date	Patents-In-Suit	Judge
50	Bell Semiconductor, LLC v. NVIDIA Corporation 1-22-cv-11933 (DMA)	11/14/2022	6436807 7396760	Hon. William G. Young
51	Bell Semiconductor, LLC v. NXP USA, Inc. 3-22-cv-00594 (SDCA)	4/27/2022	7007259	Hon. Cynthia Bashant
52	Bell Semiconductor, LLC v. NXP USA, Inc. 3-22-cv-01267 (SDCA)	8/26/2022	7149989 7260803	Hon. Linda Lopez
53	Bell Semiconductor, LLC v. NXP USA, Inc. 3-22-cv-01527 (SDCA)	10/6/2022	7231626	Hon. Todd W. Robinson
54	Bell Semiconductor, LLC v. NXP USA, Inc. 3-22-cv-01794 (SDCA)	11/15/2022	7396760	Hon. Jinsook Ohta
55	Bell Semiconductor, LLC v. Omnivision Technologies, Inc. 8-22-cv-01512 (CDCA)	8/11/2022	7007259	Hon. John A. Kronstadt
56	Bell Semiconductor, LLC v. Omnivision Technologies, Inc. 8-22-cv-01591 (CDCA)	8/26/2022	7149989 7260803	Hon. John A. Kronstadt
57	Bell Semiconductor, LLC v. Omnivision Technologies, Inc. 8-22-cv-01840 (CDCA)	10/7/2022	7396760	Hon. Karen E. Scott
58	Bell Semiconductor, LLC v. Omnivision Technologies, Inc. 8-22-cv-01979 (CDCA)	10/27/2022	6436807 7231626	Hon. John A. Kronstadt
59	Bell Semiconductor, LLC v. Phison Electronics, Inc. 1-22-cv-02197 (DCO)	8/26/2022	7149989 7260803	Hon. Daniel D. Domenico
60	Bell Semiconductor, LLC v. Phison Electronics, Inc. 1-22-cv-02485 (DCO)	9/23/2022	6436807 7007259	Hon. N. Reid Neureiter

	Case (Including party, case number and jurisdiction)	Filing Date	Patents-In-Suit	Judge
61	Bell Semiconductor, LLC v. Phison Electronics, Inc. 1-22-cv-02696 (DCO)	10/13/2022	7231626	Hon. Kristen L. Mix
62	Bell Semiconductor, LLC v. Phison Electronics, Inc. 1-22-cv-02698 (DCO)	10/13/2022	7396760	Hon. S. Kato Crews
63	Bell Semiconductor, LLC v. Qualcomm Inc. et al 3-22-cv-00595 (SDCA)	4/27/2022	6436807 7007259	Hon. Cynthia Bashant
64	Bell Semiconductor, LLC v. Qualcomm Incorporated et al. 3-22-cv-01266 (SDCA)	8/26/2022	7149989 7260803	Hon. Linda Lopez
65	Bell Semiconductor, LLC v. Qualcomm Technologies, Inc. 3-22-cv-01526 (SDCA)	10/6/2022	7231626	Hon. Todd W. Robinson
66	Bell Semiconductor, LLC v. Qualcomm Technologies, Inc. 3-22-cv-01796 (SDCA)	11/16/2022	7396760	Hon. Cathy Ann Bencivengo
67	Bell Semiconductor, LLC v. Rockchip Electronics Co. Ltd. 4-22-cv-00819 (EDTX)	9/23/2022	6436807 7007259	Hon. Sean D. Jordan
68	Bell Semiconductor, LLC v. Rockchip Electronics Co., Ltd. 4-22-cv-00734 (EDTX)	8/26/2022	7149989 7260803	Hon. Amos L. Mazzant, III
69	Bell Semiconductor, LLC v. Rockchip Electronics Co., Ltd. 4-22-cv-00962 (EDTX)	11/14/2022	7231626 7396760	Hon. Amos L. Mazzant, III
70	Bell Semiconductor, LLC v. Sequans Communications, SA et al. 0-22-cv-02106 (DMN)	8/26/2022	7149989 7260803	Hon. Wilhelmina M. Wright
71	Bell Semiconductor, LLC v. Sequans Communications, SA et al. 0-22-cv-02344 (DMN)	9/23/2022	6436807 7007259	Hon. Wilhelmina M. Wright

	Case (Including party, case number and jurisdiction)	Filing Date	Patents-In-Suit	Judge
72	Bell Semiconductor, LLC v. Sequans Communications, SA et al. 0-22-cv-02660 (DMN)	10/21/2022	7231626 7396760	Hon. Wilhelmina M. Wright
73	Bell Semiconductor, LLC v. Silicon Laboratories, Inc. 1-22-cv-01096 (WDTX) *[1-22-cv-11292 (DMA)]*	8/11/2022	7007259	Hon. Robert Pitman
74	Bell Semiconductor, LLC v. Silicon Laboratories, Inc. 1-22-cv-01094 (WDTX) *[1-22-cv-11389 (DMA)]*	8/26/2022	7149989 7260803	Hon. Robert Pitman
75	Bell Semiconductor, LLC v. Silicon Laboratories, Inc. 1-22-cv-01086 (WDTX) *[1-22-cv-11722 (DMA)]*	10/11/2022	7396760	Hon. Robert Pitman
76	Bell Semiconductor, LLC v. Silicon Laboratories, Inc. 1-22-cv-01122 (WDTX)	11/1/2022	6436807 7231626	Hon. Lee Yeakel
77	Bell Semiconductor, LLC v. Skyworks Solutions, Inc. 1-22-cv-11291 (DMA)	8/11/2022	6436807 7007259	Hon. William G. Young
78	Bell Semiconductor, LLC v. Skyworks Solutions, Inc. 1-22-cv-11390 (DMA)	8/26/2022	7149989 7260803	Hon. Allison D. Burroughs
79	Bell Semiconductor, LLC v. Skyworks Solutions, Inc. 1-22-cv-11723 (DMA)	10/11/2022	7396760	Hon. Denise J. Casper
80	Bell Semiconductor, LLC v. Skyworks Solutions, Inc. 1-22-cv-11839 (DMA)	10/28/2022	7231626	Hon. Allison D. Burroughs
81	Bell Semiconductor, LLC v. Socionext America Inc. 2-22-cv-10906 (EDMI)	4/27/2022	6436807 7007259	Hon. Gershwin A. Drain

	Case (Including party, case number and jurisdiction)	Filing Date	Patents-In-Suit	Judge
82	Bell Semiconductor, LLC v. Socionext America, Inc. 2-22-cv-12018 (EDMI)	8/26/2022	7149989 7260803	Hon. Gershwin A. Drain
83	Bell Semiconductor, LLC v. Socionext America, Inc. 2-22-cv-12749 (EDMI)	11/14/2022	7231626 7396760	Hon. Terrence G. Berg
84	Bell Semiconductor, LLC v. Western Digital Technologies, Inc. 8-22-cv-01592 (CDCA)	8/26/2022	7149989 7260803	Hon. John A. Kronstadt
85	Bell Semiconductor, LLC v. Western Digital Technologies, Inc. 8-22-cv-01823 (CDCA)	10/5/2022	7231626	Hon. Karen E. Scott
86	Bell Semiconductor, LLC v. Western Digital Technologies, Inc. 8-22-cv-01127 (CDCA)	6/7/2022	6436807 7007259	Hon. John A. Kronstadt
87	Bell Semiconductor, LLC v. Western Digital Technologies, Inc. 8-22-cv-02083 (CDCA)	11/15/2022	7396760	Hon. John W. Holcomb

11. BSLLC also filed three cases requesting that the International Trade Commission ("ITC" or "Commission") investigate various of Plaintiffs' Customers (and certain of their customers) for unfair trade practice due to purported infringement of a subset of the Asserted Patents, with two of those ITC complaints being filed within the past six weeks. A list of the ITC cases brought by BSLLC against Plaintiffs' Customers, identified by case name, date filed, and the specific Asserted Patents BSLLC asserts in each case, is as follows:

Case (Including Case Name, Case Number, And Identification Of Respondents)	Date Case Filed	Patents-In-Suit
Electronic Devices, Semiconductor Devices, and Components Thereof; Inv. No. 337-TA-3640 (Violation) 337-3640 (ITC) Respondents: NXP, SMC, Micron Technology, nVidia, AMD, Acer, Infineon, Motorola, Western Digital	10/6/2022	7,231,626 7,260,803
Semiconductor Devices Having Layered Dummy Fill, Electronic Devices, and Components Thereof; Inv. No. 337-TA-3649 (Violation) 337-3649 (ITC) Respondents: Analog Devices, Bose, Marvell Semiconductor, Robosense, Kioxia, MaxLinear, Linksys, MACOM, Silicon Laboratories, Denso, Skyworks, OmniVision, Arlo Technologies	10/14/2022	7,396,760
Electronic Devices and Semiconductor Devices with Timing-Aware Dummy Fill and Components Thereof; Inv. No. 337-TA-1319 (Violation) 337-TA-1319 (ITC)[1] Respondents: NXP, SMC, Micron Technology, nVidia, Advance Micro Devices, Acer, Analog Devices, Bose, Marvell Semiconductor, Robosense, Kioxia, Socionext, Qualcomm, Lenovo, Motorola Mobility	4/29/2022	7,007,259

12. As the above lists illustrate, BSLLC asserts various different combinations of the Asserted Patents in the different lawsuits against Plaintiffs' Customers, resulting in a complicated and sprawling set of cases against Plaintiffs' Customers. Given the volume of cases

[1] BSLLC requested termination of the 337-TA-1319 investigation after the Commission affirmed the Administrative Law Judge's scheduling order that set the date for completion of the investigation to be after the patent asserted in that investigation expired.

BSLLC has brought, and the number of semiconductor companies accused of infringement, a multitude of law firms and legal counsel are involved in defending Plaintiffs' Customers. On information and belief, BSLLC's litigation tactics are designed to harass Plaintiffs' Customers in an effort to force them to accept BSLLC's exorbitant valuation of the Asserted Patents. BSLLC's abusive litigation campaign is burdening not only Plaintiffs' Customers, but also Plaintiffs as their technology is at the heart of BSLLC's infringement allegations.

13. In its litigation campaign against the semiconductor industry, BSLLC has consistently identified Plaintiffs' EDA design tools, and *only* Plaintiffs' EDA design tools, as the instrumentalities that purportedly practice the claimed methods of the Asserted Patents, alleging that Plaintiffs' Customers' use of these tools to design their semiconductor chip products results in infringement of the Asserted Patents.

14. The Customers have entered into license agreements with Plaintiffs, giving the Customers access to and ability to use Plaintiffs' EDA design tools ("License Agreements"). These License Agreements contain defense and/or indemnity provisions relating to allegations of infringement of third-party intellectual property, including patents. As a result of BSLLC's litigation campaign against Plaintiffs' Customers, a multitude of customers have requested indemnity from Plaintiffs. Plaintiffs' Customers are seeking defense and/or indemnity from Plaintiffs in connection with BSLLC's allegations of infringement as to all of the Asserted Patents.

15. By bringing dozens of simultaneous lawsuits and ITC investigations involving the same issues of validity and infringement, BSLLC's litigation campaign ensures spiraling litigation costs, untold instances of duplicative depositions, and inconsistent findings. The suits

are a strain on judicial resources and early, decisive action from the Court would save this Court—and others—from wasted, duplicative efforts. Because BSLLC's infringement allegations against Plaintiffs' Customers are predicated on the customers' use of Plaintiffs' EDA design tools, an actual and substantial controversy, ripe for adjudication, exists as to the validity and infringement of the Asserted Patents.

16. Plaintiffs seek declaratory judgment that BSLLCS's Asserted Patents are invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.

17. Plaintiffs also seek declaratory judgment that the methods embodied in their EDA design tools do not infringe BSLLC's patents, and as a result, use of those EDA design tools by the Customers does not infringe any of the Asserted Patents.

18. Plaintiffs seek declaratory judgment in this action so that the invalidity of BSLLC's Asserted Patents and the non-infringement of the Asserted Patents by use of Plaintiffs' EDA design tools can be adjudicated in a single forum, as between BSLLC, the alleged assignee of the Asserted Patents, and Plaintiffs, the suppliers of the EDA design tools identified as the accused instrumentalities. In so doing, Plaintiffs seek to enable the customer-suit-exception to pause all active litigation by BSLLC against Plaintiffs' Customers for alleged infringement of the Asserted Patents.

19. Plaintiffs also seek temporary and preliminary injunctive relief to preserve the status quo by preventing BSLLC from continuing its costly and disruptive campaign against Plaintiffs' Customers while this action proceeds.

THE PARTIES

20. Plaintiff Synopsys is a Delaware corporation with its principal place of business at 690 East Middlefield Road, Mountain View, California 94043.

21. Plaintiff Cadence is a Delaware corporation with its principal place of business at 2655 Seely Avenue, San Jose, California 95134.

22. Defendant BSLLC is a Delaware limited liability company with its principal place of business at One West Broad Street, Suite 901, Bethlehem, Pennsylvania 18018.

PATENTS ASSERTED AGAINST PLAINTIFFS' CUSTOMERS

23. The Asserted Patents relate to certain methods and steps for use in the design and verification of semiconductor chips that may be performed with the assistance of a computer. The patents generally fall into three groupings: those relating to "dummy metal fill," those relating to engineering change orders ("ECOs"), and those relating to design validation. As described herein, the BSLLC allegations of infringement regarding the Asserted Patents are directed towards the methods performed by Plaintiffs' EDA design tools.

24. All the methods described in the Asserted Patents, regardless of group, are related to a subset of steps allegedly performed during the design of integrated circuits. These methods, however, are directed to only a small part of the integrated circuit design process.

25. Moreover, none of the claims of the Asserted Patents that BSLLC asserted or charted in its complaints, regardless of category, are directed to any manufacturing processes. In fact, the manufacture of any integrated circuits designed using Plaintiffs' EDA tools identified in each of BSLLC's lawsuits takes place after (and in many cases, years after) such integrated circuits were designed using those tools.

A. The Dummy Metal Fill Patents

26. "Dummy metal fill" refers to non-functional metal shapes that are inserted into open areas of the metal layers of a semiconductor design. Dummy metal fill adds no functionality to a manufactured semiconductor device, but is added to a design for the purpose of ensuring that one step in the future chip fabrication process, referred to as Chemical Mechanical Polishing or CMP, does not damage the devices during manufacture. The CMP process uses an abrasive chemical slurry to polish a silicon wafer, removing excess material and evening out any irregular portions, thereby making the silicon wafer flat or planar. One issue that can arise in the CMP process is that different areas on a wafer can have more material removed by the CMP process than other areas, depending on the density of metal in each of the different areas, among other factors. This phenomenon is illustrated below, showing the post-CMP topography variation that results from the difference in interconnection density (*i.e.*, the wafer has dishing in sparse areas in the design).

1. U.S. Patent No. 7,007,259

27. The '259 patent, titled "Method for Providing Clock-Net Aware Dummy Metal Using Dummy Regions," is attached hereto as Exhibit A. United States Patent and Trademark Office ("USPTO") assignment records indicate the '259 patent was originally assigned to LSI Logic Corporation when it issued on February 28, 2006, and was later assigned to a series of

companies before being finally assigned to BSLLC. On its face, the '259 patent claims priority to July 31, 2003.

28. The '259 patent relates to an algorithm for deciding where to put dummy fill objects in a design that has other objects, prioritizing certain open spaces to be filled later than others based on the characteristics of the nearby objects in the design. The '259 patent alleges that prior dummy fill algorithms were purportedly disadvantageous because they required multiple runs of the dummy metal-fill tool.

2. U.S. Patent No. 7,260,803

29. The '803 patent, titled "Incremental Dummy Metal Insertions," is attached hereto as Exhibit B. USPTO assignment records indicate the '803 patent was originally assigned to LSI Corporation when it issued on August 21, 2007, and was later assigned to a series of companies before being finally assigned to BSLLC. On its face, the '803 patent claims priority to October 10, 2004.

30. The '803 patent relates to a method for removing previously inserted dummy metal fill from a design after an incremental change is made to the design by checking "whether any dummy metal objects intersect with any other objects in the design data" and deleting any intersecting dummy metal objects from the design data. The '803 patent alleges this process of checking for and deleting overlapping objects from a design avoids having to rerun the dummy fill tool.

3. U.S. Patent No. 6,436,807

31. The '807 patent, titled "Method for Making an Interconnect Layer and a Semiconductor Device Including the Same," is attached hereto as Exhibit C. USPTO assignment

records indicate the '807 patent was originally assigned to Agere Systems Guardian Corp. when it issued on August 20, 2002, and was later assigned to a series of companies before being finally assigned to BSLLC. On its face, the '807 patent claims priority to January 18, 2000.

32. The '807 patent relates to methods for adding dummy metal fill objects to a design where the width of the dummy metal fill objects is "based upon a dielectric layer deposition bias."

4. U.S. Patent No. 7,396,760

33. The '760 patent, titled "Method and System for Reducing Inter-Layer Capacitance in Integrated Circuits," is attached hereto as Exhibit D. USPTO assignment records indicate the '760 patent was originally assigned to LSI Corporation when it issued on July 8, 2008, and was later assigned to a series of companies before being finally assigned to BSLLC. On its face, the '760 patent claims priority to November 17, 2004.

34. The '760 patent relates to methods for inserting dummy metal fill objects in a design in a manner that allegedly minimizes overlap of dummy fill objects on different layers by rearranging the dummy metal fill objects on adjacent layers in the design.

B. The ECO Patent: U.S. Patent No. 7,231,626

35. The '626 patent, titled "Method of Implementing an Engineering Change Order in an Integrated Circuit Design by Windows," is attached hereto as Exhibit E. USPTO assignment records indicate the '626 patent was originally assigned to LSI Corporation when it issued on June 12, 2007, and was later assigned to a series of companies before being finally assigned to BSLLC. On its face, the '626 patent claims priority to December 17, 2004.

36. The '626 patent relates to methods for implementing an ECO in a semiconductor chip design through selective editing of the design. The '626 patent describes creating a "window" around the design changes introduced by the ECO and routing only the parts of the design within that window.

C. The Design Validation Patent: U.S. Patent No. 7,149,989

37. The '989 patent, titled "Method of Early Physical Design Validation and Identification of Texted Metal Short Circuits in an Integrated Circuit Design," is attached hereto as Exhibit F. USPTO assignment records indicate the '989 patent was originally assigned to LSI Logic Corporation when it issued on December 12, 2006, and was later assigned to a series of companies before being finally assigned to BSLLC. On its face, the '989 patent claims priority to September 22, 2004.

38. The '989 patent relates to methods for identifying "texted metal short circuits in an integrated circuit design" using a "specific rule deck" that contains a subset of the larger design rule deck, where the design rule deck specifies checks to be performed on a chip design.

JURISDICTION AND VENUE

39. The foregoing paragraphs 1-38 are incorporated as if set forth herein in their entirety.

40. This Court has jurisdiction over the subject matter of these claims under the patent laws of the United States pursuant to 28 U.S.C. §§ 1331 and 1338(a). Additionally, this Court has subject-matter jurisdiction over Plaintiffs' request for declaratory relief under 28 U.S.C. §§ 2201 and 2202.

41. An actual controversy exists between Plaintiffs, on the one hand, and BSLLC, on the other, as to (1) whether BSLLC's Asserted Patents are valid and enforceable; (2) whether Plaintiffs' EDA design tools used by the Customers BSLLC has sued infringe the Asserted Patents; and (3) whether Plaintiffs' Customers infringe the Asserted Patents by simply using Plaintiffs' EDA design tools or by making, using, offering for sale, selling and/or importing semiconductor devices designed using Plaintiffs' EDA design tools.

42. This Court has personal jurisdiction over BSLLC because it is incorporated in this District as a Delaware limited liability company. This Court also has personal jurisdiction over BSLLC because of its recent filing of patent lawsuits in this District, including: *Bell Semiconductor, LLC v. Integrated Device Technology, Inc*., C.A. No. 19-2155-LPS (D. Del., filed Nov. 18, 2019); *Bell Semiconductor, LLC v. Micron Technology Inc. et al.*, C.A. No. 22-1292-CFC (D. Del., filed Sept. 30, 2022); and *Bell Semiconductor, LLC v. Advanced Micro Devices, Inc. et al.*, C.A. No. 22-1293-CFC (D. Del., filed Sept. 30, 2022). By bringing lawsuits in this District, Defendant has purposefully availed itself of the benefits and protections of the laws of this state and consented to personal jurisdiction in Delaware.

43. Venue is proper in this District pursuant to 28 U.S.C. § 1391 because of Defendant's intentional contact with Delaware. BSLLC is in the business of patent enforcement and its incorporation in Delaware and assertion of patents in Delaware makes venue proper in this District.

44. Venue is also convenient in this District, as evidenced by the fact that BSLLC has purposely availed itself of the court system in Delaware for the purpose of asserting patents. The alleged infringement and validity of BSLLC's Asserted Patents is best resolved in one district

court action, rather than in the over 85 separate lawsuits and 2 ITC actions BSLLC has filed to date involving the Asserted Patents. Plaintiffs' products are at the core of BSLLC's infringement allegations in each of the cases filed against Plaintiffs' Customers and is conveniently resolved in Delaware, where Plaintiffs and BSLLC are all incorporated, as are many of Plaintiffs' Customers who BSLLC accuses of infringement.

FACTUAL BACKGROUND

1. BSLLC's '259 District Court and ITC Patent Assertions

45. BSLLC began its litigation campaign against Plaintiffs' Customers on April 27, 2022. On that date, BSLLC filed 10 lawsuits against Plaintiffs' Customers for their alleged infringements of the '259 Patent: *Bell Semiconductor, LLC v. Advanced Micro Devices, Inc.*, 1:22-cv-10632 (D. Mass.); *Bell Semiconductor, LLC v. Kioxia America, Inc.*, 2:22-cv-726 (E.D. Cal.); *Bell Semiconductor, LLC v. Socionext America Inc.*, 2:22-cv-10906 (E.D. Mich.); *Bell Semiconductor v. NVIDIA Corp., Inc.*, 4:22-cv-10636 (D. Mass.); *Bell Semiconductor, LLC v. Analog Devices, Inc.*, 1:22-cv-10633 (D. Mass.); *Bell Semiconductor, LLC v. Marvell Technology Group, Ltd. et al.*, 4:22-cv-10635 (D. Mass.); *Bell Semiconductor, LLC v. Infineon Techs. America Corp.* 1:22-cv-10634 (D. Mass.); *Bell Semiconductor, LLC v. Micron Tech., Inc.*, No. 1:22-cv-192 (D. Idaho); *Bell Semiconductor, LLC v. Qualcomm Inc. et al.*, 3:22-cv-595 (S.D. Cal.); and *Bell Semiconductor, LLC v. NXP USA, Inc.*, 3:22-cv-594 (S.D. Cal.).

46. BSLLC's allegations of infringement of the '259 patent are premised on Customers' use of Plaintiffs' EDA "design tools to insert dummy metal into a circuit design (the 'Accused Processes') as recited in the '259 patent claims." In particular, BSLLC alleges that the "Accused Processes" performed by Plaintiffs' EDA design tools satisfy every step of claimed

methods in the '259 patent. As an example of the alleged infringement, BSLLC included a claim chart picking and choosing various features from Cadence's Innovus and Pegasus EDA design tools as exemplary of the infringement alleged with respect to Plaintiffs' EDA design tools.

47. BSLLC further alleges the "Accused Processes" performed by Plaintiffs' EDA design tools "infringe and continue to infringe one or more claims of the '259 patent during the pendency of the '259 patent" and Plaintiffs' Customers therefore infringe "directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the '259 patent." BSLLC's allegations of infringement are solely based on the Customers' use of Plaintiffs' EDA tools and do not specify that any further steps are necessary to effectuate the alleged infringement.

48. BSLLC seeks, as relief in each of the Customer lawsuits involving the '259 patent, (1) an award of damages from Customers; (2) an accounting of damages for alleged infringement; (3) enhanced damages; (4) pre- and post- judgment interest; (5) attorneys' fees and costs; and (6) a permanent injunction pursuant to 35 U.S.C. § 283, prohibiting Customers from continuing to engage in the "Accused Processes" (*i.e.*, use of Plaintiffs' EDA design tools).

49. On April 28, 2022, the day after filing its first wave of lawsuits, BSLLC filed a parallel complaint with the ITC, accusing Plaintiffs' Customers of infringing the '259 patent. A copy of the ITC complaint for that action, *In the Matter of Certain Electronic Devices and Semiconductor Devices with Timing-Aware Dummy Fill and Components Thereof*, Inv. No. 337-TA-1319 ("1319-Action"), is attached as Exhibit G1. The complaint in the 1319-Action named several of Plaintiffs' customers as respondents, including: NXP Semiconductors, N.V., NXP

B.V., NXP USA, Inc., Micron Technology, Inc., NVIDIA Corporation, Advanced Micro Devices, Inc., Infineon Technologies America Corp, Analog Devices, Inc., Marvell Technologies America Corp., Marvell Semiconductor, Inc., Kioxia Corporation, Kioxia America, Inc., Socionext Inc., Socionext America, Inc., and Qualcomm Technologies, Inc. (collectively, "1319-Action Customer Respondents"). The complaint sought an exclusion order preventing the 1319-Action Customer Respondents from importing into the United States semiconductor devices designed using Plaintiffs' EDA design tools.

50. BSLLC alleged that the 1319-Action Customer Respondents infringed the '259 patent because the 1319-Action Customer Respondents' "circuit designs and/or semiconductor products" "are made, produced, and/or processed by a ***design tool***, such as a Cadence" and/or "Synopsys" EDA design tool. Exhibit G2, complaint Ex. 60 at 1(emphasis added). BSLLC further alleged that the processes performed by Plaintiffs' EDA design tools infringe by "inserting dummy metal into a circuit design where dummy regions are prioritized such that the dummy regions located adjacent to clock nets are filled with dummy metal last." *Id*. BSLLC also alleged that Plaintiffs' EDA "design tools all function similarly with respect to the functionality" identified as infringing. As an example of alleged infringement, BSLLC included a claim chart picking and choosing various features from Cadence's Innovus and Pegasus design tools as exemplary of the infringement alleged with respect to Plaintiffs' EDA design tools." *Id*.

51. Based on the 1319-Action Customer Respondents' purported infringing use of Plaintiffs' EDA design tools, BSLLC alleged the 1319-Action Customer Respondents directly infringed claims 1–17 and 35–37 of the '259 Patent. Exhibit G1 at ¶ 3.

52. BSLLC sought as relief in the 1319-Action limited exclusion orders against the individual Respondents, excluding from entry into the United States the products accused of infringing the '259 Patent. Exhibit G1 at ¶ 8. BSLLC further sought cease-and-desist orders, pursuant to 19 U.S.C. § 1337(d), prohibiting each customer respondent from, importing, selling, offering for sale (including via the internet or electronic mail), advertising (including via the internet or electronic mail), or transferring products made using Plaintiffs' EDA design tools. Exhibit G1 at ¶ 9.

53. The Commission instituted the ITC investigation on June 7, 2022. Certain of the 1319-Action Customer Respondents requested entry into the Commission's Early Disposition Program, but the Commission denied early disposition.

54. Because its products were specifically identified and charted in the 1319-Action complaint, and because multiple Customers requested indemnity in view of the allegations in the 1319-Action complaint, Plaintiff Cadence made the difficult decision to intervene in the 1319-Action and moved accordingly on June 14, 2022. The ITC granted Cadence's motion on June 23, 2022, finding "(1) the motion is timely; (2) the movant has an interest relating to the property or transaction that is the subject of the action; (3) the movant is so situated that the disposition of the action may as a practical matter impair or impede the movant's ability to protect that interest; (4) the movant is not adequately represented by existing parties; and (5) the intervention will not unduly delay or prejudice the adjudication of the original parties' rights." ITC Investigation No. 337-TA-1319, Order No. 5 (June 23, 2022), at 2.

55. Shortly thereafter, on July 7, 2022, the ITC Commission adopted a procedural schedule that would have resulted in the completion of the ITC investigation and the Presidential

review period after the expiration of the '259 patent. On information and belief, BSLLC delayed in asserting the '259 patent and misjudged the length of the schedule the ITC was likely to adopt. Consequently, BSLLC requested to withdraw its ITC complaint and terminate the 1319-Action after it lost its challenge to the procedural schedule. BSLLC would instead continue to pursue its infringement allegations in the district courts. The Commission granted BSLLC's request and the 1319-Action was terminated on August 29, 2022.

56. Before the Commission had even officially terminated the 1319-Action, however, BSLLC resumed filing lawsuits against more of Plaintiffs' Customers. BSLLC further asserted the '259 patent in another district court case on June 7, 2022; in six more district court cases on August 11, 2022; and in another eight district court cases on September 22 and 23, 2022: *Bell Semiconductor, LLC v. Western Digital Tech., Inc.*, 8:22-cv-1127 (C.D. Cal.); *Bell Semiconductor, LLC v. Silicon Laboratories, Inc.*, 1:22-cv-1096 (W.D. Tex.); *Bell Semiconductor, LLC v. Maxlinear, Inc*., 3:22-cv-1178 (S.D. Cal.); *Bell Semiconductor, LLC v. Skyworks Solutions, Inc*., 1:22-cv-11291 (D. Mass.); *Bell Semiconductor, LLC v. MACOM Tech. Solutions Inc*., 1:22-cv-11290 (D. Mass.); *Bell Semiconductor, LLC v. Omnivision Techs., Inc*., 8:22-cv-1512 (C.D. Cal.); *Bell Semiconductor, LLC v. Analog Devices, Inc.*, 1:22-cv-10633 (D. Mass.); *Bell Semiconductor, LLC v. Western Digital Techs., Inc.*, 8:22-cv-1127 (C.D. Cal.); *Bell Semiconductor, LLC v. Ampere Computing, LLC*, 3:22-cv-1435 (D. Or.); *Bell Semiconductor, LLC v. Lattice Semiconductor Corp.*, 3:22-cv-1437 (D. Or.); *Bell Semiconductor, LLC v. Phison Elecs., Inc.*, 1:22-cv-2485 (D. Colo.); *Bell Semiconductor, LLC v. Rockchip Elecs. Co. Ltd.*, 4:22-cv-819 (E.D. Tex.); *Bell Semiconductor, LLC v. Ambarella, Inc.*, 3:22-cv-273 (S.D. Ohio);

Bell Semiconductor, LLC v. ASMedia Tech., Inc., 1:22-cv-8166 (S.D.N.Y.); *Bell Semiconductor, LLC v. Sequans Commc'ns, SA et al*., 0:22-cv-2344 (D. Minn.).

57. All 25 of the district court suits filed between April 27, 2022 to September 23, 2022 asserting the '259 patent against Plaintiffs' Customers remain pending.

2. BSLLC'S '807 Patent Assertions

58. BSLLC asserts infringement of the '807 patent in 17 of the 24 district cases in which BSLLC is asserting infringement of the '259 patent. From August 15, 2022 to November 1, 2022, BSLLC filed amended complaints in 10 of the cases it had filed asserting infringement of the '259 patent to add allegations of infringement of the '807 patent, filed 7 new lawsuits asserting the '807 patent together with the '259 patent against more of Plaintiffs' Customers, and also filed an additional 4 new lawsuits against still more of Plaintiffs' Customers, asserting infringement of the '807 patent together with the '626 patent. In addition, on November 10, 2022, BSLLC filed a new lawsuit accusing Analog Devices, Inc. of infringing the '807 patent. *Bell Semiconductor, LLC v. Analog Devices, Inc*., Case No. 1-22-cv-11901 (DMA).

59. In each of these lawsuits, BSLLC alleges Plaintiffs' Customers "directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the '807 patent by using the patented methodology to design one or more semiconductor devices ... in the United States." BSLLC alleges the Customers used Plaintiffs' EDA "design tools ... to make a layout for an interconnect layer of a semiconductor device (the "Accused Processes") as recited in the '807 patent claims." In particular, BSLLC alleges the "Accused Processes" in Plaintiffs' EDA design tools practice every step of the '807 patent claims.

60. BSLLC further alleges that in using Plaintiffs' EDA design tools, Plaintiffs' Customers "infringe and continue to infringe one or more claims of the '807 patent during the pendency of the '807 patent." BSLLC alleges that Plaintiffs' Customers "directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes [of Plaintiffs' EDA design tools] in violation of one or more claims of the '807 patent." As an example of infringement, BSLLC included a claim chart picking and choosing various features from Cadence's Innovus EDA design tool as exemplary of the infringement alleged with respect to Plaintiffs' EDA design tools.

61. BSLLC seeks, as relief in each of the lawsuits involving the '807 patent, (1) an award of damages from Customers; (2) an accounting of damages for alleged infringement; (3) enhanced damages; (4) pre- and post- judgment interest; (5) attorneys' fees and costs; and (6) a permanent injunction pursuant to 35 U.S.C. § 283, prohibiting Plaintiffs' Customers from continuing to engage in the Accused Processes (i.e., use of Plaintiffs' EDA design tools).

62. All 23 of the district court suits asserting infringement of the '807 patent against Plaintiffs' Customers remain pending.

3. BSLLC'S '989 and '803 Patent District Court Assertions

63. On August 26, 2022, BSLLC commenced another phase of BSLLC's litigation campaign against Plaintiffs' Customers. BSLLC filed 24 lawsuits, across thirteen district courts, asserting infringement of both the '989 patent and the '803 patent: *Bell Semiconductor, LLC v. Silicon Laboratories, Inc*. (1:22-cv-11389) (D. Mass.); *Bell Semiconductor, LLC v. Infineon Technologies America Corporation* (1:22-cv-11385) (D. Mass.); *Bell Semiconductor, LLC v.*

Analog Devices, Inc. (1:22-cv-11384) (D. Mass.); *Bell Semiconductor, LLC v. Advanced Micro Devices, Inc.* (1:22-cv-11383) (D. Mass.); *Bell Semiconductor, LLC v. Skyworks Solutions, Inc*. (1:22-cv-11390) (D. Mass.); *Bell Semiconductor, LLC v. Nvidia Corporation* (4:22-cv-11388) (D. Mass.); *Bell Semiconductor, LLC v. Marvell Technology Group, Ltd. et al* (4:22-cv-11387) (D. Mass.); *Bell Semiconductor, LLC v. ASMedia Technology, Inc.* (1:22-cv-7307) (S.D.N.Y.); *Bell Semiconductor, LLC v. Ambarella, Inc*. (3:22-cv-245) (SDOH); *Bell Semiconductor, LLC v. Sequans Communications, SA et al* (0:22-cv-2106) (D. MINN.); *Bell Semiconductor, LLC v. ams-OSRAM AG d/b/a amsOSRAM Automotive Lighting Systems USA, Inc.* (2:22-cv-12017) (E.D. Mich.); *Bell Semiconductor, LLC v. Phison Electronics, Inc*. (1:22-cv-2197) (D. Colo.); *Bell Semiconductor, LLC v. Kioxia America, Inc*. (2:22-cv-1510) (EDCA); *Bell Semiconductor, LLC v. Socionext America, Inc*. (2:22-cv-12018) (E.D. Mich.); *Bell Semiconductor, LLC v. Lattice Semiconductor, Inc*. (3:22-cv-1282) (DOR); *Bell Semiconductor, LLC v. Ampere Computing,* LLC (3:22-cv-1280) (DOR); *Bell Semiconductor, LLC v. Omnivision Technologies, Inc.* (8:22-cv-1591) (CDCA); *Bell Semiconductor, LLC v. Western Digital Technologies, Inc.* (8:22-cv-1592) (CDCA); *Bell Semiconductor, LLC v. Micron Technology, Inc.* (1:22-cv-375) (DID); *Bell Semiconductor, LLC v. Rockchip Electronics Co., Ltd.* (4:22-cv-734) (EDTX); *Bell Semiconductor, LLC v. NXP USA, Inc.* (3:22-cv-1267) (S.D. Cal.); *Bell Semiconductor, LLC v. Qualcomm Incorporated et al* (3:22-cv-1266) (S.D. Cal.); *Bell Semiconductor, LLC v. Maxlinear, Inc*. (3:22-cv-1268) (S.D. Cal.); *Bell Semiconductor, LLC v. MACOM Technology Solutions Inc.* (1:22-cv-11386) (D. Mass.).

64. Rather than seeking to amend its earlier-filed complaints to add its infringement allegations regarding the ’803 and ’989 patents, BSLLC filed separate, parallel lawsuits,

meaning these Customers are involved in multiple district court cases simultaneously, and most before different judges, as BSLLC made no attempt to inform the district courts that it had previously filed related cases.

65. In each of these lawsuits, BSLLC alleges Plaintiffs' Customers "directly infringe pursuant to 35 U.S.C. § 271(a)" one or more claims of the '989 patent and the '803 patent "by using the patented methodology to design one or more semiconductor devices ... in the United States."

66. As to the '989 patent, BSLLC alleges the Customers used Plaintiffs' EDA "design tools ... to validate its circuit designs (the "Accused Processes") as recited in the '989 patent claims." In particular, BSLLC alleges that when Customers use Plaintiffs' products, Plaintiffs' EDA design tools perform the "Accused Processes" as they perform every step recited in the claims. BSLLC specifically alleges the use of Plaintiffs' EDA design tools "infringe and continue to infringe one or more claims of the '989 patent during the pendency of the '989 patent" and Plaintiffs' Customers "directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes [performed by Plaintiffs' EDA design tools] in violation of one or more claims of the '989 patent." As an example of infringement, BSLLC included a claim chart picking and choosing various features from Synopsys' IC Validator EDA design tool as exemplary of the infringement alleged with respect to Plaintiffs' EDA design tools.

67. As to the '803 patent, BSLLC alleges Customers used the "Accused Processes" in Plaintiffs' EDA design tools to practice every step of the claims in the '803 patent. BSLLC

specifically alleges the "Accused Processes" in Plaintiffs' EDA design tools "infringe and continue to infringe one or more claims of the '803 patent during the pendency of the '803 patent" and that Plaintiffs' Customers "directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes [of Plaintiffs' EDA design tools] in violation of one or more claims of the '803 patent." As an example of infringement, BSLLC included a claim chart picking and choosing various features from Cadence's Innovus EDA design tool as exemplary of the infringement alleged with respect to Plaintiffs' EDA design tools.

68. BSLLC seeks, as relief in each of the lawsuits involving the '989 patent and '803 patent, (1) an award of damages from Customers; (2) an accounting of damages for alleged infringement; (3) enhanced damages; (4) pre- and post- judgment interest; (5) attorneys' fees and costs; and (6) a permanent injunction pursuant to 35 U.S.C. § 283, prohibiting Customers from continuing to engage in the Accused Processes (i.e., use of Plaintiffs' EDA design tools).

69. All 24 of the district court suits asserting infringement of the '989 patent and '803 patent against Plaintiffs' Customers remain pending.

4. BSLLC'S '626 Patent Assertions

70. BSLLC continued to expand its litigation campaign against Plaintiffs' Customers with yet another phase of lawsuits. From October 5, 2022 to November 14, 2022, BSLLC asserted infringement of the '626 patent in 22 district court cases against Plaintiffs' Customers, many of which were already saddled with multiple litigations involving one or more of the '259 patent, the '807 patent, the '989 patent and/or the '803 patent. The district court cases alleging

infringement of the '626 patent by Plaintiffs' Customers include: *Bell Semiconductor LLC v. Advanced Micro Devices, Inc.*, 1:22-cv-11696) (D. Mass.); *Bell Semiconductor LLC v. NVIDIA Corporation*, 4:22-cv-11700 (D. Mass.); *Bell Semiconductor LLC v. Infineon Technologies America Corp*., 1:22-cv-11698 (D. Mass.); *Bell Semiconductor LLC v. Western Digital Technologies, Inc*., 8:22-cv-1823 (C.D. Cal.); *Bell Semiconductor LLC v. Micron Technology, Inc*., 1:22-cv-417 (D. Idaho); *Bell Semiconductor LLC v. Qualcomm Technologies, Inc.*, 3:22-cv-1526 (S.D. Cal.); *Bell Semiconductor LLC v. NXP USA, Inc.*, 3:22-cv-1527 (S.D. Cal.); *Bell Semiconductor LLC v. Lattice Semiconductor Corporation*, 3:22-cv-1542 (D. Or); *Bell Semiconductor LLC v. Phison Electronics, Inc*., 1:22-cv-2696 (D. Colo.); *Bell Semiconductor LLC v. MACOM Technology Solutions Inc*., 1:22-cv-11788 (D. Mass.); *Bell Semiconductor LLC v. ams-ORAM AG d/b/a ams OSRAM Automotive Lighting Systems USA, Inc*., 2:22-cv-12518 (E.D. Mich.); *Bell Semiconductor LLC v. Kioxia America, Inc*., 2:22-cv-1880 (E.D. Cal.); *Bell Semiconductor LLC v. Sequans Communications, SA et al*, 0:22-cv-2660 (D. Minn.); *Bell Semiconductor LLC v. Omnivision Technologies, Inc*., 8:22-cv-1979 (C.D. Cal.); *Bell Semiconductor LLC v. ASMedia Technology, Inc.*, 1:22-cv-9260 (S.D.N.Y.); *Bell Semiconductor LLC v. Skyworks Solutions, Inc*., 1:22-cv-11839 (D. Mass.); *Bell Semiconductor LLC v. Silicon Laboratories, Inc*., 1:22-cv-01122 (W.D. Tex.); *Bell Semiconductor, LLC v. Analog Devices, Inc*. 1-22-cv-11901 (D. Mass); *Bell Semiconductor, LLC v. Marvell Technology Group, Ltd. et al*, 4-22-cv-11906 (D. Mass); *Bell Semiconductor, LLC v. Ambarella, Inc.*, 3:22-cv-0323 (S.D. Ohio); *Bell Semiconductor LLC v. Socionext America, Inc.*, 2:22-cv-12749 (E.D. Mich.); *Bell Semiconductor, LLC v. Rockchip Electronics Co., Ltd.*, 4:22-cv-0962 (E.D. Tex.). Of those 22

lawsuits, 11 involve the '626 patent alone, while 5 others involve both the '626 patent and the '807 patent, and 3 more involve both the '626 patent and the '760 patent.

71. In each of these lawsuits, BSLLC alleges Plaintiffs' Customers "directly infringe pursuant to 35 U.S.C. § 271(a)" one or more claims of the '626 patent "by using the patented methodology to design one or more semiconductor devices ... in the United States." BSLLC alleges Customers used Plaintiffs' EDA "design tools ... to perform incremental routing in implementing an ECO (the "Accused Processes") as recited in the '626 patent claims." In particular, BSLLC alleges the "Accused Processes" in Plaintiffs' EDA design tools practice every step of the '626 patent claims.

72. BSLLC further alleges Customers' use of the "Accused Processes" in Plaintiffs' EDA design tools causes them to "infringe and continue to infringe one or more claims of the '626 patent during the pendency of the '626 patent." BSLLC alleges Plaintiffs' Customers "directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes [of Plaintiffs' EDA design tools] in violation of one or more claims of the '626 patent." As an example of infringement, BSLLC included a claim chart picking and choosing various features from Cadence's Innovus EDA design tool as exemplary of the infringement alleged with respect to Plaintiffs' EDA design tools.

73. BSLLC seeks relief in each of the lawsuits involving the '626 patent including, but not limited to, (1) an award of damages from Customers; (2) and accounting of damages for alleged infringement; (3) enhanced damages; (4) pre- and post- judgment interest; (5) attorneys' fees and costs; and (6) a permanent injunction pursuant to 35 U.S.C. § 283, prohibiting

Customers from continuing to engage in the Accused Processes (i.e., use of Plaintiffs' EDA design tools).

74. All 22 of the district court suits asserting infringement of the '626 patent against Plaintiffs' Customers remain pending.

5. BSLLC '760 Patent District Court Assertions

75. In October 2022, BSLLC launched yet another wave of litigation, this time alleging Plaintiffs' Customers infringe the '760 patent. BSLLC filed 15 district court cases naming Plaintiffs' Customers as defendants on October 7 and 28, 2022, as well as an ITC complaint on October 13, 2022, that named a subset of the 15 district court defendant customers as respondents. As of November 15, 2022, BSLLC filed another 7 district court cases naming Plaintiffs' Customers, for a total 22 district court cases involving the '760 patent. In 15 of the 22 district court cases, BSLLC asserted only the '760 patent. In 6 other suits BSLLC asserted the '760 patent along with the '626 patent, and in one lawsuit BSLLC asserted the '760 patent together with '807 patent. The suits involving the '760 patent include: *Bell Semiconductor LLC v. ASMedia Technology, Inc*., 1:22-cv-9260 (S.D.N.Y.); *Bell Semiconductor LLC v. Sequans Communications, SA et al*, 0:22-cv-2660 (D. Minn.); *Bell Semiconductor LLC v. ams-ORAM AG d/b/a ams OSRAM Automotive Lighting Systems USA, Inc*., 2:22-cv-12518 (E.D. Mich.); *Bell Semiconductor LLC v. Advanced Micro Devices, Inc*., 1:22-cv-11783 (D. Mass.); *Bell Semiconductor LLC v. Micron Technology, Inc*., 1:22-cv-438 (D. Idaho); *Bell Semiconductor LLC v. Lattice Semiconductor Corporation*, 3:22-cv-1543 (D. Or.); *Bell Semiconductor LLC v. Phison Electronics, Inc.*, 1:22-cv-2698 (D. Colo.); *Bell Semiconductor LLC v. Analog Devices, Inc*., 1:22-cv-11718 (D. Mass.); *Bell Semiconductor LLC v. Skyworks Solutions, Inc*., 1:22-cv-

11723 (D. Mass.); *Bell Semiconductor LLC v. Silicon Laboratories, Inc*., 1:22-cv-11722 (D. Mass.); *Bell Semiconductor LLC v. Marvell Semiconductor, Inc.*, 4:22-cv-11721 (D. Mass.); *Bell Semiconductor LLC v. MACOM Technology Solutions Inc*., 1:22-cv-11719 (D. Mass.); *Bell Semiconductor LLC v. Maxlinear, Inc*., 3:22-cv-1537 (S.D. Cal.); *Bell Semiconductor LLC v. Omnivision Technologies, Inc.* (8:22-cv-1840) (C.D. Cal.); *Bell Semiconductor LLC v. Kioxia Corporation et al*, 2:22-cv-1797 (E.D. Cal.); *Bell Semiconductor, LLC v. Ambarella, Inc.*, 3:22-cv-00323 (S.D. Ohio); *Bell Semiconductor, LLC v. Infineon Technologies America Corporation*, 1:22-cv-11926 (D. Mass.); *Bell Semiconductor, LLC v. NVIDIA Corporation*, 1:22-cv-11933 (D. Mass.); *Bell Semiconductor LLC v. Socionext America, Inc.*, 2:22-cv-12749 (E.D. Mich.); *Bell Semiconductor, LLC v. Rockchip Electronics Co., Ltd.*, 4:22-cv-00962 (E.D. Tex.); *Bell Semiconductor, LLC v. NXP USA, Inc.*, 3:22-cv-01794 (S.D. Cal.); *Bell Semiconductor LLC v. Western Digital Technologies, Inc.*, 8:22-cv-02083 (C.D. Cal.); and *Bell Semiconductor, LLC v. Qualcomm Technologies, Inc.*, 3:22-cv-01796 (S.D. Cal.).

76. .

77. In each of the 15 district court cases, BSLLC alleges Plaintiffs' Customers "directly infringe pursuant to 35 U.S.C. § 271(a)" one or more claims of the '760 patent "by using the patented methodology to design one or more semiconductor devices ... in the United States."

78. BSLLC alleges Plaintiffs' Customers used Plaintiffs' EDA "design tools ... to perform incremental routing in implementing an ECO (the "Accused Processes") as recited in the '760 patent claims." In particular, BSLLC alleges the "Accused Processes" performed by Plaintiffs' EDA design tools perform every step of the methods recited in the '760 patent claims.

79. BSLLC further alleges the "Accused Processes" performed by Plaintiffs' EDA design tools "infringe and continue to infringe one or more claims of the '760 patent during the pendency of the '760 patent." BSLLC also alleges Plaintiffs' Customers "directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes [of Plaintiffs' EDA design tools] in violation of one or more claims of the '760 patent." As an example of infringement, BSLLC included a claim chart picking and choosing various features from Cadence's Innovus EDA design tool as exemplary of the infringement alleged with respect to Plaintiffs' EDA design tools.

80. As relief in each of the lawsuits involving the '760 patent, BSLLC seeks at least: (1) an award of damages from Customers; (2) an accounting of damages for alleged infringement; (3) enhanced damages; (4) pre- and post- judgment interest; (5) attorneys' fees and costs; and (6) a permanent injunction pursuant to 35 U.S.C. § 283, prohibiting Customers from continuing to engage in the Accused Processes (i.e., use of Plaintiffs' EDA design tools).

81. All 22 of the district court suits asserting infringement of the '760 patent against Plaintiffs' Customers remain pending.

6. BSLLC's '626 Patent and '803 Patent ITC Patent Assertion

78. On October 6, 2022, BSLLC burdened Plaintiffs' Customers with yet another litigation proceeding and filed a complaint with the ITC accusing Plaintiffs' Customers of infringing the '626 patent and the '803 patent. *In the Matter of Matter of Certain Electronic Devices and Semiconductor Devices, And Components Thereof*, Inv. No. 337-TA-1340 ("1340-Action') attached as Exhibit H. The complaint named as respondents NXP, SMC, Micron,

NVIDIA, AMD, Acer, Infineon, Qualcomm, Motorola, Western Digital and Qualcomm[2] (collectively, "3640-Action Customer Respondents"). The complaint seeks an exclusion order preventing the named customer respondents from importing into the United States semiconductor devices designed using Plaintiffs' EDA design tools.

79. As to the '626 Patent, BSLLC alleges infringement of Customer "circuit designs and/or semiconductor products" that are "made, produced, and/or processed by a ***design tool***, such as a Cadence Design Systems, Inc. …. tool." Exhibit I1, complaint Ex. 34A, at 1 (emphasis added). BSLLC further alleges Customers' use of Plaintiffs' EDA design tools infringe the '626 patent by "implementing an engineering change order through a window that is less than the entire area of the integrated circuit design." *Id.* BSLLC further alleges Plaintiffs' EDA "design tools all function similarly with respect to the functionality" identified as infringing. As an example of infringement, BSLLC included a claim chart picking and choosing various features from Cadence's Innovus EDA design tool as exemplary of the infringement alleged with respect to Plaintiffs' EDA design tools.

80. As to the '803 Patent, BSLLC alleges infringement of Customer "semiconductor integrated circuit devices made using a ***design tool***, such as a Cadence Design Systems, Inc. ... tool." Exhibit J, complaint Ex. 34B, at 1 (emphasis added). BSLLC contends Plaintiffs' EDA design tools infringe by "check[ing] for dummy metal objects intersecting any other objects in the design data following a change to a portion of the design data, and if so, delet[ing] any such intersecting dummy metal objects to avoid having to re-run the dummy fill tool." BSLLC further

[2] The ITC did not institute an investigation against Qualcomm.

contends Plaintiffs' EDA "***design tools*** all function similarly with respect to the functionality" identified as infringing. *Id.* As an example of infringement, BSLLC charted Cadence's Innovus EDA design tool as exemplary of the infringement alleged with respect to Plaintiffs' EDA design tools. Based on the Customers' purported infringing use of Plaintiffs' EDA design tools, BSLLC alleges the customer respondents directly infringed claims 1-4 of the '626 Patent and claims 1-6 and 9-11 of the '803 Patent. Exhibit H at ¶ 5.

81. In addition to alleging infringement of the '626 patent and '803 patent based on use of Plaintiffs' EDA design tools, BSLLC also alleges satisfaction of the technical prong of the ITC's domestic industry requirement under 19 U.S.C. § 1337(a)(2), based on the purported "use of Cadence design tools to lay out semiconductor designs for the Domestic Industry Product according to the Asserted Patents" by BSLLC's alleged licensee, Broadcom, Inc. ("Broadcom"). Exhibit H at ¶ 114; *see also id.* at ¶ 111. Plaintiff Cadence, however, neither agreed nor authorized the use of its *own* EDA design tools as grounds for BSLLC to file a complaint with the ITC against Plaintiffs' Customers, including Cadence customers. The perverse result is that BSLLC—as a non-practicing entity—has solely relied on a third-party's use of Cadence's EDA design tools to gain entry to the ITC for the detriment of Plaintiff Cadence and its customers.

82. BSLLC seeks as relief in the 1340-Action a limited exclusion orders against the individual Respondents excluding from entry into the United States the products accused of infringing the '626 patent and/or the '803 patent. BSLLC further seeks a cease-and-desist order, pursuant to 19 U.S.C. § 1337(d), prohibiting each customer respondent from importing, selling, offering for sale (including via the internet or electronic mail), advertising (including via the internet or electronic mail), or transferring products made using Plaintiffs' EDA design tools.

83. The Commission instituted the investigation in the 3640-Action on November 8, 2022. Certain of the 3640-Action Customer Respondents requested entry into the Commission's Early Disposition Program, but the Commission denied early disposition. On November 17, 2022, BSLLC served subpoenas on Plaintiffs in connection with the 1340-Action, seeking discovery in the form of documents and deposition testimony regarding Synopsys' and Cadence's EDA design tools. All of the district court suits and the 3640-Action asserting infringement of the '626 patent against Plaintiffs' Customers remain pending and none have been stayed.

6. BSLLC's '760 Patent ITC Patent Assertion

84. On October 14, 2022, BSLLC continued to pile on and filed another complaint with the ITC, accusing several of Plaintiffs' Customers of infringing the '760 patent. *In the Matter of Matter of Certain Electronic Devices and Semiconductor Devices, and Components Thereof*, Inv. 337-TA-3649 ("3649-Action'), attached as Exhibit K. The complaint named as respondents several of Plaintiffs' Customers, including: Analog Devices, Inc., Kioxia America, Inc., Kioxia Corporation, MACOM Technology Solutions Inc., Marvell Technology Group, Ltd., Silicon Laboratories, Inc., and Skyworks Solutions, Inc. (collectively, "3649-Action Customer Respondents"). The complaint seeks an exclusion order preventing the importation into the United States of semiconductor devices designed using Plaintiffs' EDA design tools by the customer respondents.

85. BSLLC alleges Plaintiffs' Customers' "circuit designs and/or semiconductor products" that are "made, produced, and/or processed by a ***design tool***, such as a Cadence" tool and "Synopsys" tool infringe the '760 patent. Exhibit. L, complaint Ex. 42, at 1 (emphasis added). BSLLC further alleges Customers' use of Plaintiffs' EDA design tools infringes the

'760 patent "by rearranging dummy fill features to minimize their overlap when viewed across adjacent layers." *Id.* BSLLC also alleges Plaintiffs' EDA "***design tools*** all function similarly with respect to the functionality" identified as infringing. *Id.* (emphasis added). As an example of infringement, BSLLC charted Cadence's Innovus design tool as exemplary of the infringement alleged with respect to use of Plaintiffs' EDA design tools.

86. Based on the purported infringing use of Plaintiffs' EDA design tools, BSLLC alleges the customer respondents directly infringed claims 1–6 and 11–13 of the '760 Patent. Exhibit K at ¶ 5.

87. In addition to alleging infringement of the '760 patent based on use of Plaintiffs' EDA design tools, BSLLC also alleges satisfaction of the technical prong of the ITC's domestic industry requirement under 19 U.S.C. § 1337(a)(2)), based on the purported "use of Cadence design tools to lay out semiconductor designs for the Domestic Industry Product according to the Asserted Patents" by BSLLC's alleged licensee, Broadcom. Exhibit K ¶ 105; *see also id.* ¶ 102. Plaintiff Cadence, however, neither agreed nor authorized the use of its *own* EDA design tools as grounds for BSLLC to file a complaint with the ITC against Plaintiffs' Customers, including Cadence customers. The perverse result is that BSLLC—as a non-practicing entity—has solely relied on a third-party's use of Cadence's EDA design tools to gain entry to the ITC for the detriment of Plaintiff Cadence and its customers.

88. BSLLC seeks as relief in the 3649-Action a limited exclusion order against the individual Respondents, excluding from entry into the United States the products accused of infringing the '760 patent. Exhibit K at ¶ 10. BSLLC further seeks cease-and-desist orders, pursuant to 19 U.S.C. § 1337(d), prohibiting each customer respondent from importing, selling,

offering for sale (including via the internet or electronic mail), advertising (including via the internet or electronic mail), or transferring products made using Plaintiffs' EDA design tools. Exhibit K at ¶ 11.

89. Plaintiffs anticipate that the ITC will render a decision on institution of the 3649-Action within days of the filing of this Declaratory Judgment Action. All of the district court suits asserting infringement of the '706 patent against Plaintiffs' Customers remain pending and none have been stayed.

90. Attached to this Complaint as Exhibits M and N, respectively, are tables of all the pending District Court cases and ITC investigations by filing date that are part of BSLLC's litigation campaign against Plaintiffs' Customers for their use of Plaintiffs' EDA design tools.

FIRST CLAIM FOR RELIEF

(Declaratory Judgment that Plaintiffs Do Not Infringe the '259 Patent)

91. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–90 of this Complaint as if fully set forth herein.

92. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy within the meaning of 28 U.S.C. § 2201 between Plaintiffs and Defendant regarding whether Plaintiffs and the methods performed by their EDA design tool products infringe any claim of the '259 Patent and/or contribute to or induce their respective Customers to infringe.

93. Plaintiffs do not infringe the '259 Patent because their EDA design tool products, including Cadence's Innovus and Pegasus EDA design tools and Synopsys' IC Compiler, IC Compiler II, and IC Validator EDA design tools, do not perform the methods claimed in claims

1–17 and 35–37, or make, sell, use or import products that contain the program instructions claimed in claims 18–34. For example, Plaintiffs and their EDA design tools, when used by Customers, do not "prioritiz[e] the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets" or "insert[] dummy metal into the sorted dummy regions such that the dummy regions located adjacent to increasingly wider clock nets are filled last, thereby minimizing any timing impact on the clock nets."

94. Plaintiffs are therefore entitled the declaratory judgment that their EDA design tools, and the uses thereof, do not infringe any claims of '259 Patent, directly or indirectly, literally or by equivalence.

SECOND CLAIM FOR RELIEF

(Declaratory Judgment that Plaintiffs Do Not Infringe the '626 Patent)

95. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–94 of this Complaint as if fully set forth herein.

96. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy within the meaning of 28 U.S.C. § 2201 between Plaintiffs and Defendant regarding whether Plaintiffs and the methods performed by their EDA design tool products infringe any claim of the '626 Patent and/or contribute to or induce their respective Customers to infringe.

97. Plaintiffs do not infringe the '626 Patent because their EDA design tool products, including Cadence's Innovus EDA design tools and Synopsys' IC Compiler and IC Compiler II EDA design tools, do not perform the methods claimed in claims 1–4, nor do Plaintiffs make,

sell, use or import products that contain the program instructions claimed in claims 5–8. For example, Plaintiffs and their EDA design tools, when used by Customers, do not "perform[] an incremental routing of the integrated circuit design only for each net in the integrated circuit design that is enclosed by the window."

98. Plaintiffs are therefore entitled the declaratory judgment that their EDA design tools, and the uses thereof, do not infringe any claims of '626 Patent, directly or indirectly, literally or by equivalence.

THIRD CLAIM FOR RELIEF

(Declaratory Judgment that Plaintiffs Do Not Infringe the '760 Patent)

99. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–98 of this Complaint as if fully set forth herein.

100. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy within the meaning of 28 U.S.C. § 2201 between Plaintiffs and Defendant regarding whether Plaintiffs and the methods performed by their EDA design tool products infringe any claim of the '760 Patent and/or contribute to or induce their respective Customers to infringe.

101. Plaintiffs do not infringe the '760 Patent because their EDA design tool products, including Cadence's Innovus and Pegasus EDA design tools and Synopsys' IC Compiler, IC Compiler II, and IC Validator EDA design tools, do not perform the methods claimed in claims 1–19. For example, Plaintiffs and their EDA design tools, when used by Customers, do not "determine[e] an overlap between the first dummy fill space and the second dummy fill space; and minimize[e] the overlap by re-arranging a plurality of first dummy fill features and a

plurality of second dummy fill features" or "determine[e] whether there is an overlap between the plurality of dummy fill features on the first layer and the plurality of dummy fill features on the second layer; and minimize[e]the overlap by re-arranging the plurality of dummy fill features on the first layer and the second layer, wherein a total inter-layer capacitance of the integrated circuit is minimized."

102. Plaintiffs are thus entitled the declaratory judgment that their EDA design tools, and the uses thereof, do not infringe any claims of '760 Patent, directly or indirectly, literally or by equivalence.

FOURTH CLAIM FOR RELIEF

(Declaratory Judgment that Plaintiffs Do Not Infringe the '803 Patent)

103. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–102 of this Complaint as if fully set forth herein.

104. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy within the meaning of 28 U.S.C. § 2201 between Plaintiffs and Defendant regarding whether Plaintiffs and the methods performed by their EDA design tool products infringe any claim of the '803 Patent and/or contribute to or induce their respective Customers to infringe.

105. Plaintiffs do not infringe the '803 Patent because their EDA design tool products, including Cadence's Innovus and Pegasus EDA design tools and Synopsys' IC Compiler, IC Compiler II, and IC Validator EDA design tools, do not perform the methods claimed in claims 1–11, nor do Plaintiffs make, sell, use or import products that contain the program instructions claimed in claims 12–22. For example, Plaintiffs and their EDA design tools, when used by

Customers, do not "after a portion of the design data is changed, perform[] a check to determine whether any dummy metal objects intersect with any other objects in the design data; and … delet[e] the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool."

106. Plaintiffs are therefore entitled the declaratory judgment that their EDA design tools, and the uses thereof, do not infringe any claims of '803 Patent, directly or indirectly, literally or by equivalence.

FIFTH CLAIM FOR RELIEF

(Declaratory Judgment that Plaintiffs Do Not Infringe the '807 Patent)

107. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–106 of this Complaint as if fully set forth herein.

108. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy within the meaning of 28 U.S.C. § 2201 between Plaintiffs and Defendant regarding whether Plaintiffs and the methods performed by their EDA design tool products infringe any claim of the '807 Patent and/or contribute to or induce their respective Customers to infringe.

109. Plaintiffs do not infringe the '807 Patent because their EDA design tool products, including Cadence's Innovus and Pegasus EDA design tools and Synopsys' IC Compiler, IC Compiler II, and IC Validator EDA design tools, do not perform the methods claimed in claims 1–18. For example, Plaintiffs and their EDA design tools when used by Customers do not "add[] dummy fill features … [where] the adding compris[es] defining a minimum dummy fill lateral

dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer."

110. Plaintiffs are therefore entitled the declaratory judgment that their EDA design tools, and the uses thereof, do not infringe any claims of '807 Patent, directly or indirectly, literally or by equivalence.

SIXTH CLAIM FOR RELIEF

(Declaratory Judgment that Plaintiffs Do Not Infringe the '989 Patent)

111. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–110 of this Complaint as if fully set forth herein.

112. In view of the facts and allegations set forth above, there is an actual, justiciable, substantial, and immediate controversy within the meaning of 28 U.S.C. § 2201 between Plaintiffs and Defendant regarding whether Plaintiffs and the methods performed by their EDA design tool products infringe any claim of the '989 Patent and/or contribute to or induce their respective Customers to infringe.

113. Plaintiffs do not infringe the '989 Patent because their EDA design tool products, including Cadence's PVS and Pegasus EDA design tools and Synopsys' IC Validator EDA design tool, do not perform the methods claimed in claims 1–6, nor do Plaintiffs make, sell, use or import products that contain the program instructions claimed in claims 7–12. For example, Plaintiffs and their EDA design tools, when used by Customers, do not "generat[e] a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design."

114. Plaintiffs are therefore entitled the declaratory judgment that their EDA design tools, and the uses thereof, do not infringe any claims of '989 Patent, directly or indirectly, literally or by equivalence.

SEVENTH CLAIM FOR RELIEF

(Declaratory Judgment of the Invalidity and Unenforceability of the '259 Patent)

115. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–114 of this Complaint as if fully set forth herein.

116. The claims of the '259 patent are invalid and unenforceable because each claim fails to comply with the applicable requirements of the Patent Act, including, but without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

117. The claims of the '259 patent fail to comply with 35 U.S.C. § 101 because the '259 patent lacks patentable subject matter. The claims cover abstract ideas on mental processes that lack an inventive concept and raise preemption issues.

118. Further, the claims of the '259 patent are also invalid under 35 U.S.C. § 112 because the specification does not enable the claimed invention. For example, the claims require the recited method to provide for "minimizing any timing impact on the clock nets," but the specification explains that the recited methods actually sacrifice timing impact on the clock nets in order to increase density. Further, each claim, when viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty. For example, each of the claims contains one or more of the terms "identifying," "prioritizing," "suitable," and/or "minimizing any timing impact on the clock nets," each of which are undefined and lack guidance from the specification and prosecution

history about the meaning and scope of the terms. Those skilled in the art cannot therefore ascertain the proper scope of the invention with reasonable certainty.

119. The claims of the ’259 patent are also invalid under 35 U.S.C. §§ 102 and/or 103, as anticipated and/or obvious in view of the prior art. For example, claims of the ’259 patent are rendered obvious by U.S. Pat. No. 7,124,386, titled “Dummy Fill for Integrated Circuits,” to Smith et al (“Smith patent”), in combination with U.S. Pat. No. 5,793,643, titled “Method for Handling Variable Width Wires in a Grid-based Channel Router,” to Cai (“Cai patent”), and/or Friedman, “Clock Distribution Networks in Synchronous Digital Integrated Circuits,” Proceedings of the IEEE, Vol. 89, No. 5, 665-692 (May 2001) (“Friedman”). By way of further example, the claims of the ’259 patent are rendered obvious by Kahng *et al.*, “Area Fill Synthesis for Uniform Layout Density,” IEEE Transactions on Computer-Aided Designing of Integrated Circuits and Systems 21(10):1132–1147 (Oct. 2002) (“Kahng”) in view of Grobman et al., “Reticle Enhancement Technology: Implications and Challenges for Physical Design,” DAC '01: Proceedings of the 38th Annual Design Automation Conference (June 2001) (“Grobman”).

120. The Smith patent was filed on Jun. 7, 2002 and issued on Oct. 17, 2006. Because the Jun. 7, 2002 filing date of the Smith patent precedes the July 31, 2003 filing date of the ’259 patent, the Smith patent is prior art to the ’259 patent under at least pre-AIA 35 U.S.C. § 102(e). The Cai patent was filed on April 30, 1996 and issued on August 11, 1998. Because the Cai patent was published long before the July 31, 2003 filing date of the ’259 patent, the Cai patent is prior art to the ’259 patent under at least pre-AIA 35 U.S.C. §§ 102(a)-102(b). Friedman was published in May of 2001 as part of Proceedings of the IEEE. Because Friedman was published more than a year before the July 31, 2002 filing date of the ’259 patent,

Friedman is prior art to the '259 patent under at least pre-AIA 35 U.S.C. § 102(a)-(b). Grobman was published on June 22, 2001 as part of the Proceedings of the 38th Annual Design Automation Conference. Because the '259 patent filing date of July 31, 2002 is more than a year after the Grobman publication, Grobman is prior art to the '259 patent under at least pre-AIA 35 U.S.C. § 102(a)-(b). Kahng was published on Oct. 2002 as part of the IEEE Transactions on Computer-Aided Designing of Integrated Circuits and Systems. Because the '259 patent filing date of July 31, 2002 is after the Kahng publication, Kahng is prior art to the '259 patent under at least pre-AIA 35 U.S.C. § 102(a).

121. The Smith patent teaches use of "dummy fill rules" to guide performance of dummy fill operations based on a "priority" scheme. Smith explains that the dummy fill rules may be specified by a circuit designer based on design goals including a specified minimum dummy fill density and specified timing constraints of the critical nets in the design, including the clock nets. Smith also describes exemplary dummy fill rules with a priority scheme dictating that dummy regions adjacent to wider nets should be filled after dummy regions adjacent to narrower nets. Upon information and belief, a person of ordinary skill in the art ("POSITA") at the time of filing of the '259 patent would have understood that in a given design, clock nets near a clock source are among the widest nets in the design and can be among the most timing-critical because they can be sensitive to capacitive coupling, which may result in "clock skew." For example, Friedman explains that clock nets near a clock source are usually designed to be the widest of all the clock nets, and that "clock skew is particularly sensitive to changes in linewidth close to the clock source." Similarly, the Cai patent explains that "in many designs, it is desirable to implement time sensitive paths and critical nets, such as those used to route CLOCK

and RESET signals, with wider wires. This helps minimize skew, crosstalk power, and timing problems. Of course, it would be uneconomical to use the wider wires for all connections since this would substantially increase the overall die size." Based on these teachings, upon information and belief a POSITA would have understood that clock nets can be among the most timing-critical nets, and in such cases, a POSITA would have configured the priority scheme in Smith's dummy fill rules to fill dummy regions adjacent clock nets last, and to fill dummy regions adjacent wider clock nets after filling dummy regions adjacent narrower clock nets. Thus, the claims of the '259 patent are rendered obvious by the Smith patent in combination with the Cai patent and/or Friedman

122. Khang teaches a method whereby a density analysis of features present on an integrated circuit is performed which determines the area available for placing dummy fill. Following the density analysis, Kahng teaches that dummy fill placed too close to an interconnect can increase parasitic capacitance which requires minimizing both the size and amount of fill. For this reason, Kahng teaches dynamically adjusting the size of the area abutting an interconnect that must not contain dummy fill. Grobman explains that during production of an integrated circuit, a process engineer may decide to extend the gap between dummy fill and a clock net in order to further reduce parasitic capacitance. On information and belief, a person of ordinary skill in the art ("POSITA") would have understood this teaching of Grobman to require adjusting the spacing between dummy fill and a critical path, such as a clock net, by placing fill adjacent to said path last. Grobman further discloses that different dummy fill will have a lesser or greater impact on parasitic capacitance depending on its size and shape. On information and belief, it would have been obvious to a POSITA to adapt the teaching of Kahng such that dummy

fill was excluded from the immediate region surrounding critical nets, such as clocks. On information and belief, a POSITA would also look to the same teachings of Grobman to modify the method of Kahng to render obvious the remaining limitations of the ’259 patent and combine the method of Kahng with the teaching from Grobman that different fill is used in instances where the fill’s dimensions will result in different properties and that fill should be placed at the border of a guard band last in order to avoid having to remove fill placed inadvertently.

123. Plaintiff is therefore entitled to a declaratory judgment that the claims of the ‘259 Patent are invalid and unenforceable.

EIGHTH CLAIM FOR RELIEF

(Declaratory Judgment of the Invalidity and Unenforceability of the ’626 Patent)

124. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–123 of this Complaint as if fully set forth herein.

125. The claims of the ’626 patent are invalid and unenforceable because each claim fails to comply with the applicable requirements of the Patent Act, including, but without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

126. The claims of the ’626 patent fail to comply with 35 U.S.C. § 101 because the ’626 patent lacks patentable subject matter. The claims cover abstract ideas on mental processes that lack an inventive concept and raise preemption issues.

127. Further, the claims of the ’626 patent are also invalid under 35 U.S.C. §112 because the invention is not enabled by the specification and because each claim, when viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty. For example, each of the claims contains

one or more of the following terms that are undefined and lack guidance from the specification and prosecution history as to meaning and scope of the terms: "window," "a change," "an entire area of the integrated circuit design," and "replacing an area in a copy of the integrated circuit design that is bounded by the coordinates of the window with results of the incremental routing." Those skilled in the art cannot therefore ascertain the proper scope of the invention with reasonable certainty.

128. In addition, the claims of the '626 patent are also invalid under 35 U.S.C. §§ 102 and/or 103, as anticipated and/or obvious in view of the prior art. For example, claims of the '626 patent are anticipated and/or rendered obvious by H. Arslan and S. Dutt, "A Depth-First-Search Controlled Gridless Incremental Routing Algorithm for VLSI Circuits," ICCD '04 proceedings, October 11–13, 2004 ("Arslan"), alone or in combination with U.S. Patent No. 5,983,277, titled "Work group computing for electronic design automation," issued to Heile et al. ("Heile patent"). Arslan was published on or before November 8, 2004 and is prior art under at least pre-AIA 35 U.S.C. § 102(a). The Heile patent was filed on October 27, 1997, was issued on November 9, 1999, and is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), 102(b), and/or 102(e). Aslan explains incremental routing concepts and provides an incremental routing algorithm for grid-based routing using a bounding box that surrounds the nets added or impacted by an ECO. Those nets within the bounding box are routed using Arslan's incremental routing algorithm. The Heile patent describes an EDA design tool that incrementally compiles changes to the netlist description of an integrated circuit design. A minimum region surrounding the changes to the design is used to limit the work done by the EDA tool to only the minimum region with the changed portion of the design. The Heile patent additionally uses a bounding

box or window to surround the changed area in a design and limit the incremental routing to that area that is smaller than the entire design.

129. Plaintiffs are therefore entitled to a declaratory judgment that the claims of the '626 Patent are invalid and unenforceable.

NINTH CLAIM FOR RELIEF

(Declaratory Judgment of the Invalidity and Unenforceability of the '760 Patent)

130. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–129 of this Complaint as if fully set forth herein.

131. The claims of the '760 patent are invalid and/or unenforceable because each claim fails to comply with the applicable requirements of the Patent Act, including, but without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

132. The claims of the '760 patent fail to comply with 35 U.S.C. § 101 because the '760 patent lacks patentable subject matter. The claims cover abstract ideas on mental processes that lack an inventive concept and raise preemption issues.

133. The claims of the '760 patent are also invalid under 35 U.S.C. §112 because the specification does not enable the claimed invention and each claim, when viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty. For example, each of the claims contains on or more of the following terms that are undefined and lack guidance from the specification and prosecution history as to meaning and scope of the term: "a first dummy fill space," "a second dummy fill space," "overlap between the first dummy fill space and the second dummy fill space," "overlap between the plurality of dummy fill features on the first layer and the second layer," "minimizing

the overlap," "determining a second layer," "low density spaces," "local density pattern obtained based on an initial layout design," "non-signal carrying lines," and "total inter-layer capacitance." Those skilled in the art cannot therefore ascertain the proper scope of the invention with reasonable certainty.

134. In addition, the claims of the '760 patent is also invalid under 35 U.S.C. §§ 102 and/or 103, as anticipated and/or obvious in view of the prior art. For example, claims of the '760 patent are anticipated and/or obvious in view of U.S. Patent Pub. No. 2004/0188849, titled "Semiconductor Device and Pattern Generating Method," and issued to M. Suga et al. ("Suga patent") alone or in combination with U.S. Patent No. 6,815,811, titled "Semiconductor Integrated Circuit with Dummy Patterns," and issued to H. Ozawa et al. ("Ozawa patent"), and/or U.S. Patent No. 6,609,235, titled "Method for Providing a Fill Pattern for an Integrated Circuit Design," issued to S. Ramaswamy et al. ("Ramaswamy patent"). The Suga patent was filed on February 26, 2004, published on September 30, 2004, and is prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and/or 102(e). The Ozawa patent was filed on November 28, 2001, was published May 30, 2002, issued on November 9, 2004, and is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), 102(b), and/or 102(e). The Ramaswamy patent was filed on June 22, 2001, published as U.S. Patent Pub. No. 2002/01996162 on December 26, 2002, issued on August 19, 2003, and is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), 102(b), and/or 102(e).

135. The Suga patent discloses obtaining dummy fill spaces of successive layers based on the received integrated circuit layout data and reducing overlap between the dummy patterns in successive layers by re-arranging the center points of the dummy patterns away from each

other. Relatedly, the Ozawa patent teaches these dummy patterns can be square-shaped and do not carry any signal. Further, the Ramaswamy patent discloses placing dummy fill metal in a checkerboard pattern. To the extent the Suga patent alone does not anticipate the '803 patent, the Suga patent's teaching of re-arranging by off-centering dummy patterns, obtained based on received layout data, to reduce the overlap in view of the Ozawa patent's teaching of square-shaped dummy patterns that include non-signal carrying lines and the Ramaswamy patent's teaching of placing dummy metal in a checkerboard pattern renders the '760 patent obvious.

136. Plaintiff is therefore entitled to a declaratory judgment that the claims of the '760 Patent are invalid.

TENTH CLAIM FOR RELIEF

(Declaratory Judgment of the Invalidity and Unenforceability of the '803 Patent)

137. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–136 of this Complaint as if fully set forth herein.

138. The claims of the '803 patent are invalid and/or unenforceable because each claim fails to comply with the applicable requirements of the Patent Act, including, but without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

139. The claims of the '803 patent fail to comply with 35 U.S.C. § 101 because the '803 patent lacks patentable subject matter. The claims cover abstract ideas on mental processes that lack an inventive concept and raise preemption issues.

140. Further, the claims of the '803 patent are also invalid under 35 U.S.C. §112 because the specification does not enable the claimed invention and each claim, when viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the

scope of the invention with reasonable certainty. For example, each of the claims contains on or more of the following terms that are undefined and lack guidance from the specification and prosecution history as to meaning and scope: "rerun," "a check to determine," "remaining dummy metal objects," "the dummy metal identifications," "nets of respective wires," "net identified as dummy metal," "net of a different name," and "a modified rule check." Those skilled in the art cannot therefore ascertain the proper scope of the invention with reasonable certainty.

141. In addition, one or more claims of the '803 patent is also invalid under 35 U.S.C. §§ 102 and/or 103, as anticipated and/or obvious in view of the prior art. For example, claims of the '803 patent are anticipated and/or rendered obvious by the Ramaswamy patent alone or in combination with U.S. Patent No. 6,530,073, titled "RTL Annotation Tool for Layout Induced Netlist Changes," and issued to D. Morgan ("Morgan patent"), and/or with Hercules by Synopsys ("Hercules"). The Ramaswamy patent was filed on June 22, 2001, published as U.S. Patent Pub. No. 2002/01996162 on December 26, 2002, issued on August 19, 2003, and is prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and/or 102(e). The Morgan patent was filed on April 30, 2001, published as U.S. Patent Pub. No. 2002/0162086 on October 31, 2002, issued on March 4, 2003, and is prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and/or 102(e). Hercules was released as a system at least prior to September 30, 2002, and is prior art under at least pre-AIA 35 U.S.C. § 102(a).

142. The Ramaswamy patent discloses comparing a chip layout file against a fill pattern file, which can include dummy layout shapes, after modification in the design database of the integrated circuit design and removing, from the final layout design file, any fill patterns that

overlap with "keepout" regions where fill patterns cannot be placed. Relatedly, the Morgan patent teaches annotating an integrated circuit layout file before and after an engineering change order ("ECO") to track changes in the circuit while avoiding restarting the layout process. To the extent the Ramaswamy patent alone does not anticipate the claims of the '803 patent, the Ramaswamy patent's teaching of checking for and deleting overlaps between dummy pattern and other objects after a design modification in view of the Morgan patent's teaching of tracking ECO changes in a way that avoids rerunning the dummy fill tool and renders the '803 patent obvious.

143. Plaintiff is therefore entitled to a declaratory judgment that the claims of the '803 Patent are invalid.

ELEVENTH CLAIM FOR RELIEF

(Declaratory Judgment of the Invalidity and Unenforceability of the '807 Patent)

144. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–143 of this Complaint as if fully set forth herein.

145. The claims of the '807 patent are invalid and/or unenforceable because each claim fails to comply with the applicable requirements of the Patent Act, including, but without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

146. The claims of the '807 patent fail to comply with 35 U.S.C. § 101 because the '807 patent lacks patentable subject matter. The claims cover abstract ideas on mental processes that lack an inventive concept and raise preemption issues.

147. The claims of the '807 patent are also invalid under §112 because the specification does not enable the claimed invention and each claim, when viewed in light of the

specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty. For example, each of the claims contains on or more of the terms "defining a minimum dummy fill feature lateral dimension," "active interconnect feature density," "layout regions," "desired density of active interconnect features," "suitable" and "deposition bias," which are undefined and lack guidance from the specification and prosecution history as to meaning and scope of the terms. Those skilled in the art cannot therefore ascertain the proper scope of the invention with reasonable certainty.

148. The claims of the '807 patent are also invalid under 35 U.S.C. §§ 102 and/or 103, as anticipated and/or obvious in view of the prior art. The '807 patent issued on August 20, 2002 and claims priority to its filing date of January 18, 2000. U.S. Pat. No. 5,923,563, titled "Variable Density Fill Shape Generation," and issued to Lavin et al ("Lavin patent") anticipates the claims of the '807 patent. The Lavin patent issued on July 13, 1999 and is prior art under at least pre-AIA § 102(a). The Lavin patent discloses a method whereby a virtual grid, breaking the chip surface into sections containing a discrete portion of the chip, is imposed over an integrated circuit. The method determines a "pattern density" of the features contained in each discrete section of the virtual grid, generates fill shapes of various sizes and determines where to place them based on the measured pattern density. The Lavin patent teaches that the disclosed method is used to minimize the adverse effects of varying pattern density across an integrated circuit resulting from the fabrication process, such as deposition of a dielectric followed by chemical-mechanical polishing ("CMP"). The Lavin patent additionally teaches that the "size," or dimensions of, the fill shape should be adjusted in order to minimize ~~Based on~~ the adverse effect of varying pattern density. As such, the 'Lavin patent inherently teaches adjusting the

width of the dummy fill based on a resulting deposition bias because CMP is used where a deposition bias necessarily results from a step in the fabrication process.

149. Alternatively, the Lavin patent renders the '807 patent obvious in view of Ouma, "*Modeling of Chemical Mechanical Polishing for Dielectric Planarization*," Massachusetts Institute of Technology, Dept. of Electrical Eng. and Comp. Sci. (1998), which was published, indexed, and available from MIT as of February 1999. Ouma is prior art under at least pre-AIA 35 U.S.C. §§ 102(a)-(b). Ouma expressly teaches adjusting the width of dummy fill based on the width of the overlaying deposition bias.

150. Additionally, the '807 patent is invalid as anticipated by U.S. Patent No. 5,618,757, titled "Method for Improving the Manufacturability of the Spin-on Glass Etchback Process," issued to Bothra et al ("Bothra patent"). The Bothra patent issued on April 8, 1997 and is prior art under at least pre AIA §§ 102(a)-(b). The Bothra patent discloses a method for maintaining planarization during the fabrication of an integrated circuit by determining standardized pattern densities of dummy fill and active features on the chip surface depending on the different capacitance needs of the various sections of the chip. Dummy fill into open spaces between the active features depending on the respective standardized pattern densities. An oxide layer is then added to the chip surface which has an increased planarity over that of a chip that lacks the inclusion of dummy fill. The Bothra patent also teaches accounting for the width of the dummy fill based on the size of the overlaying deposition bias because it teaches that the oxide layer deposited over the dummy fill is raised compared to the adjacent areas without fill. Upon information and belief, a POSITA would have understood that there is a necessary relationship between deposition bias and the size of the underlying dummy fill. Alternatively, the Bothra

patent renders the ’807 patent obvious in view of Ouma based on the same disclosures identified in relation to the Lavin patent. Specifically, Ouma expressly teaches that the width of dummy fill should be adjusted based on the overlaying deposition bias.

151. Plaintiffs are therefore entitled to a declaratory judgment that the claims of the ‘807 Patent are invalid.

TWELFTH CLAIM FOR RELIEF

(Declaratory Judgment of the Invalidity and Unenforceability of the ’989 Patent)

152. Plaintiffs repeat and re-allege each and every allegation contained in paragraphs 1–151 of this Complaint as if fully set forth herein.

153. The claims of the ’989 patent are invalid and/or unenforceable because each claim fails to comply with the applicable requirements of the Patent Act, including, but without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

154. The claims of the ’989 patent fail to comply with 35 U.S.C. § 101 because the ’989 patent lacks patentable subject matter. The claims cover abstract ideas on mental processes that lack an inventive concept and raise preemption issues.

155. The claims of the ’989 patent are also invalid under 35 U.S.C. §112 because the specification does not enable the claimed invention and each claim, when viewed in light of the specification and prosecution history, fails to inform those skilled in the art about the scope of the invention with reasonable certainty. For example, each of the ’989 patent claims contains on or more of the following terms that are undefined and lack guidance from the specification and prosecution history as to meaning and scope: “between different signal sources in addition to power and ground,” “physical design rule deck,” “specifies rule checks,” “specific rule deck,”

and "physical design rules specific to texted metal shorts." Those skilled in the art cannot therefore ascertain the proper scope of the invention with reasonable certainty.

156. The claims of the '989 patent are also invalid under 35 U.S.C. §§ 102 and/or 103, as anticipated and/or obvious in view of the prior art. For example, claims of the '989 patent are anticipated and/or rendered obvious by Japanese Patent Application Publication No. JP 2001175703A to Hiroka ("Hiroka") alone or in combination with "Calibre Verification User's Manual" ("Calibre") and by Calibre alone or in combination with Hiroka. Hiroka was published on June 29, 2001 and is prior art under at least pre-AIA §§ 102(a) and/or 102(b). Calibre was published in May 2002 and is prior art under at least pre-AIA §§ 102(a) and/or 102(b). Hiroka discloses a method for verifying wiring in a circuit design layout that includes a process of determining whether it contains texted short circuits using physical design rules. Calibre describes an LVS EDA tool that identifies texted short circuits where different text names are on the same net in a semiconductor chip design, including shorts between power, ground, and other signal nets. Calibre includes a "select checks" dialog box that allows the user to control which design rule checks to run from the larger rule deck and uses the subset of design rules to perform checking, such as checking for texted short circuits.

157. Plaintiff is therefore entitled to a declaratory judgment that the claims of the '989 Patent are invalid.

DEMAND FOR A JURY TRIAL

In accordance with Federal Rules of Civil Procedure 38, Plaintiffs demand a jury trial on all issues and claims so triable.

PLAINTIFFS' PRAYER FOR RELIEF

Plaintiffs respectfully request this Court grant judgment and relief as follows:

(a) Declaring that Plaintiffs do not directly or indirectly infringe any claim of the '259 Patent, either literally or under the doctrine of equivalents;

(b) Declaring that Plaintiffs do not directly or indirectly infringe any claim of the '807 Patent, either literally or under the doctrine of equivalents;

(c) Declaring that Plaintiffs do not directly or indirectly infringe any claim of the '803 Patent, either literally or under the doctrine of equivalents;

(d) Declaring that Plaintiffs do not directly or indirectly infringe any claim of the '989 Patent, either literally or under the doctrine of equivalents;

(e) Declaring that Plaintiffs do not directly or indirectly infringe any claim of the '626 Patent, either literally or under the doctrine of equivalents;

(f) Declaring that Plaintiffs do not directly or indirectly infringe any claim of the '760 Patent, either literally or under the doctrine of equivalents;

(g) Declaring the claims of the '259 Patent to be invalid, unenforceable, and void in law;

(h) Declaring the claims of the '807 Patent to be invalid, unenforceable, and void in law;

(i) Declaring the claims of the '803 Patent to be invalid, unenforceable, and void in law;

(j) Declaring the claims of the '989 Patent to be invalid, unenforceable, and void in law;

(k) Declaring the claims of the '626 Patent to be invalid, unenforceable, and void in law;

(l) Declaring the claims of the '760 Patent to be invalid, unenforceable, and void in law;

(m) A temporary restraining order, preliminary injunction, and permanent injunction against BSLLC, its officers, employees, agents, subsidiaries, affiliates, assigns, successors, and any person acting for or on their behalf, in active concert or participation with them or who receives actual notice of this Court's order,

ordering each of them to refrain from participation in and take all necessary actions to secure a stay of each of the District Court Customer Suits.

(n) A temporary restraining order, preliminary injunction, and permanent injunction against BSLLC, its officers, employees, agents, subsidiaries, affiliates, assigns, successors, and any person acting for or on their behalf, in active concert or participation with them or who receives actual notice of this Court's order, ordering each of them to refrain from participation in and take all necessary actions to secure withdrawal of claims of patent infringement at the ITC in the 1340-Action and 3649-Action.

(o) Order that this case is "exceptional" pursuant to 35 U.S.C. § 285 entitling Plaintiffs an award of its reasonable and necessary attorneys' fees, expenses, and costs, and pre-judgment interest thereon;

(p) Order awarding Plaintiffs its costs of suit incurred in this action; and

(q) Granting to Plaintiffs such other and further relief as this Court deems just and proper.

Dated: November 18, 2022

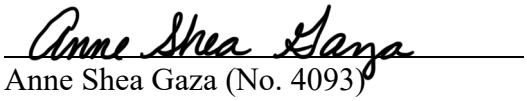
OF COUNSEL:

Krista S. Schwartz
Barrington Dyer
WILLKIE FARR & GALLAGHER LLP
One Front Street
San Francisco, CA 94111
(415) 858-7400
kschwartz@willkie.com
bdyer@willkie.com

Shaimaa Hussein
WILLKIE FARR & GALLAGHER LLP
787 Seventh Avenue
New York, NY 10019
(212) 728-8000
shussein@willkie.com

Aliza George Carrano
WILLKIE FARR & GALLAGHER LLP

YOUNG CONAWAY STARGATT & TAYLOR, LLP



Anne Shea Gaza (No. 4093)
Pilar G. Kraman (No. 5199)
Robert M. Vrana (No. 5666)
Alexis M. Stombaugh (No. 6702)
Rodney Square
1000 North King Street
Wilmington, DE 19801
(302) 571-6600
agaza@ycst.com
pkraman@ycst.com
rvrana@ycst.com
astombaugh@ycst.com

Attorneys for Synopsys, Inc. and Cadence Design Systems, Inc.

1875 K Street, N.W.
Washington, DC 20006
(202) 303-1000
acarrano@willkie.com

Attorneys for Synopsys, Inc.

Jeffrey A. Miller
Joseph Palmieri
ARNOLD & PORTER KAYE
SCHOLER LLP
3000 El Camino Real
Five Palo Alto Square, Suite 500
Palo Alto, CA 94306
(650) 319-4538
jeffrey.miller@arnoldporter.com
joseph.palmieri@arnoldporter.com

Matthew M. Wolf
Jennifer Sklenar
ARNOLD & PORTER KAYE
SCHOLER LLP
601 Massachusetts Ave, NW
Washington, DC 20001
(202) 942-5786
matthew.wolf@arnoldporter.com
jennifer.sklenar@arnoldporter.com

Kurt Riester
Lindsay Strong
ARNOLD & PORTER KAYE
SCHOLER LLP
70 West Madison Avenue, Suite 4200
Chicago, IL 60602
(312) 583-2300
kurt.riester@arnoldporter.com
lindsay.strong@arnoldporter.com

Attorneys for Cadence Design Systems, Inc.