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Attorneys for Plaintiff

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF OREGON

PORTLAND DIVISION

BELL SEMICONDUCTOR, LLC

Plaintiff,

v.

LATTICE SEMICONDUCTOR CORPORATION

Defendant.

Case No. 3:22-cv-1542

COMPLAINT FOR PATENT INFRINGMENT

JURY TRIAL DEMANDED

Plaintiff Bell Semiconductor, LLC ("Bell Semic" or "Plaintiff") brings this Complaint against Defendant Lattice Semiconductor Corporation ("Lattice") for infringement of U.S. Patent No. 7,231,626 ("the '626 patent"). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1. This is a patent infringement suit relating to Lattice's unauthorized and unlicensed use of the '626 patent. The circuit design methodologies claimed in the '626 patent are used by Lattice in the production of one or more of its semiconductor chips, including at least the Lattice PS2251-17-43 ("Lattice Accused Product").

2. Traditionally, the process flow for IC design is highly linear, with each phase of the design process depending on the previous steps. Accordingly, when revisions to portions of the physical design are made, as typically happens numerous times during the design process, all the subsequent steps typically need to be redone in their entirety for at least the layer, if not the entire device. This is because regardless of the size or extent of the revision to the physical design, the changes must be merged into a much larger integrated circuit design and then the remaining steps of the design process flow re-run.

3. Before the inventions claimed in the '626 patent, the typical turnaround time for implementing a change to the physical design for cutting edge devices was approximately one week regardless of the size of the change. This is extremely inefficient in most instances where the change relates to only a small fraction of the overall design. *See* Ex. A at 3:16–18 & Fig. 1.

4. The '626 patent's inventors solved this problem by defining a window that encloses a change specified by the revision to physical design. The window defines an area that is less

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than the area of the entire circuit design. Only the nets within that window are routed pursuant to the revision, leaving the remaining nets in the design unaffected. Then, the results of that incremental routing are inserted into a copy of the original IC design to produce a revised IC design that effects the physical design change without needing to redo the entire process flow.

5. Semiconductor devices include different kinds of materials to function as intended. For example, these devices typically include both metal (*i.e.*, conductor) and insulator materials, which are deposited or otherwise processed sequentially in layers to form the final device. These layers—and the interconnects and components formed within them—have gotten much smaller over time, increasing the performance of these devices dramatically. As a result, it has become even more important to keep the layers planar as the device is being built because defects and warpage can cause fabrication issues and malfunctioning of the device. Manufacturers use a process called Chemical Mechanical Planarization/Polishing ("CMP") to smooth out the surface of the device to prepare the device for further processing, such as deposition of another layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be "polished" away at different rates, leading to erosion or dishing on the surface. To reduce this problem "dummy" material, also known as "dummy fill," is typically inserted into low-density regions of the device to increase the overall uniformity of the structures on the surface of the layer and reduce the density variability across the surface of the device. However, dummy fill can increase capacitance if it is placed too close to signal wires, which slows the transmission speed of signals and degrades the overall performance of the device.

6. Bell Semic brings this action to put a stop to Lattice's unauthorized and

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unlicensed use of the inventions claimed in the '626 patent.

THE PARTIES

7. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

8. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America's greatest technology incubators. Bell Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

9. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor–related inventions was developed over many years by some of the world's leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation ("LSI"). This portfolio reflects technology that underlies many important innovations in the development of semiconductors and integrated circuits for high–tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

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10. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since those early days at Bell Labs. For example, Bell Semic's CTO was a LSI Fellow and Broadcom Fellow. He is known throughout the world as an innovator with more than 300 patents to his name, and he has a sterling reputation for helping semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from the semiconductor world to work with Nortel Networks in the telecom industry during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees and employees. In addition, several Bell Semic executives previously served as engineers at many of these companies and were personally involved in creating the ideas claimed throughout Bell Semic's extensive patent portfolio.

11. On information and belief, Lattice is an Oregon company with its principal place of business and headquarters at 5555 NE Moore Ct, Hillsboro, OR 97124.

12. On information and belief, Lattice develops, designs, and/or manufactures products in the United States, including in this District, according to the '626 patented processes/methodologies; and/or uses the '626 patented processes/methodologies in the United States, including in this District, to make products; and/or distributes, markets, sells, or offers to sell in the United States and/or imports products into the United States, including in this District, that were manufactured or otherwise produced using the patented process. Additionally, Lattice introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

JURISDICTION AND VENUE

13. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction

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under 28 U.S.C. §§ 1331 and 1338(a).

14. This Court has personal jurisdiction over Lattice under the laws of the State of Oregon, due at least to its substantial business in Oregon and in this District. Lattice has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of Oregon, and in this District by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of Oregon and in this District, Lattice, directly or through intermediaries: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the '626 patented process/methodology; (iii) distributes, markets, sells, or offers to sell products formed according to the '626 patented process/methodology; and/or (iv) imports products formed according to the '626 patented processes/methodologies.

15. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because Lattice has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. Lattice maintains a regular and established place of business at its corporate headquarters, which is located in the District at 5555 NE Moore Ct, Hillsboro, OR 97124. *See About Us*, Lattice Semiconductor (available at https://www.latticesemi.com/About) (last visited September 20, 2022).

16. On information and belief, Lattice employs more than 80 engineers in the State of Oregon. *See* Search Results for Current Lattice Employees, LinkedIn (available at https://www.linkedin.com/search/results/people/?currentCompany=%5B%226994%22%5D&geoUrn=%5B%22101685541%22%5D&keywords=engineer&origin=FACETED_SEARCH&sid=POi) (last visited October 13, 2022). In addition, Lattice is advertising 21 jobs in the Portland

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area, including product development and engineering positions. These positions include those that relate to the '626 patented technology, including Product Engineer, Product Test Engineering Manager, and Senior Reliability Engineer. *See Lattice Semiconductor Careers*, Lattice (https://recruiting2.ultipro.com/LAT1001LATT/JobBoard/e7f50c7c-43f9-46e9-86ed-b31eaa369842/?q=&o=postedDateDesc&f4=shWMTo1HzVuSJsTCE90ghw) (last visited October 12, 2022).

17. Venue is also convenient in this District. This is at least true because of this District's close ties to this case—including the technology, relevant witnesses, and sources of proof noted above—and its ability to quickly and efficiently move this case to resolution.

18. On information and belief, Bell Semic's causes of action arise directly from Lattice's circuit design work and other activities in this District. Moreover, on information and belief, Lattice has derived substantial revenues from its infringing acts occurring within the State of Lattice and within this District.

U.S. PATENT NO. 7,231,626

19. Bell Semiconductor owns by assignment the entire right, title, and interest in the '626 patent, entitled "Method Of Implementing An Engineering Change Order In An Integrated Circuit Design By Windows."

20. A true and correct copy of the '626 patent is attached as Exhibit A.

21. The '626 patent issued to inventors Jason K. Hoff, Viswanathan Lakshmanan, Michael Josephides, Daniel W. Prevedel, Richard D. Blinne, and Johathan P. Kuppinger.

22. The application that resulted in issuance of the'626 patent, United States Patent Application No. 11/015,123, was filed December 17, 2004. It issued on June 12, 2007 and expires on July 26, 2025.

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23. The ’626 patent generally relates to “methods of implementing an engineering change order (ECO) in an integrated circuit design.” Ex. A at 1:1–13.

24. The background section of the ’626 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior circuit design methodology was disadvantageous because “[i]n previous methods for implementing an engineering change order (ECO) request in an integrated circuit design, design tools are run for the entire integrated circuit design, even though the engineering change order typically is only a small fraction of the size of the integrated circuit design” Ex. A at 2:15–19.

25. The ’626 patent elaborates that because “cell placement, routing, design rule check validation, and timing closure run times typically scale with the size of the entire integrated circuit design,” Ex. A at 2:20–22, this produced a “typical turnaround time” of “about one week regardless of the size of the engineering change order. . . . because although the engineering change order may only have a size of a few cells, it must be merged with an integrated circuit design that typically has a much greater size.” *Id.* at 2:37–44. Certain of these steps “may be especially time consuming and resource intensive.” *Id.* at 3:16–17.

26. The inventions disclosed in the ’626 patent provide many advantages over the prior art. In particular, they provide a simple and efficient method for ensuring that revisions to the physical design of the IC do not unduly delay the completion of the design process. As the ’626 patent explains, “significant savings in the resources required to perform routing, design rule check verification, net delay calculation, and parasitic extraction may be realized by creating windows in the integrated circuit design that include only the incremental changes to the overall integrated circuit design.” Ex. A at 3:19–23.

27. As mentioned above, this is very beneficial because it substantially reduces the run

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time of the routing tools and related follow-on steps of the layout portion of the design process flow (such as calculation of net delay, design rule check, and parasitic extraction). Thus, it shortens the overall design timeline, and avoids cost overruns and delays, making it less costly to make changes later in the design process or more often. *See id.*

28. Given the aforementioned increased complexity of circuit designs and the corresponding delays from design changes, these efficiency gains have become more and more important in completing the design process without affecting time-to-market. These significant advantages are achieved through the use of the patented inventions and thus the ’626 patent presents significant commercial value for chip designers.

29. In light of the drawbacks of the prior art, the ’626 patent’s inventors recognized the need for a circuit design methodology in which the time required to implement an ECO “depend[s] on the number of net changes in the [ECO] rather than on the total number of nets in the entire integrated circuit design.” Ex. A at 2:51–53. The inventions claimed in the’626 patent address this need.

30. The ’626 patent contains two independent claims and 8 total claims, covering a method and computer readable medium for implementing a change order in an integrated circuit design. Claim 1 reads:

> 1. A method comprising steps of:
>
> (a) receiving as input an integrated circuit design;
>
> (b) receiving as input an engineering change order to the integrated circuit design;
>
> (c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;

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(d) performing an incremental routing of the integrated circuit design only for each net in the integrated circuit design that is enclosed by the window;

(e) replacing an area in a copy of the integrated circuit design that is bounded by the coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and

(f) generating as output the revised integrated circuit design.

31. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device design process, *e.g.,* providing a novel and substantially more efficient process flow in which only the affected nets would be considered in the incremental routing. This results in substantial reduction in the expected time of the design portion of producing semiconductor devices.

32. The claims of the ’626 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to post-ECO routing. The claims of the ’626 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the ’626 patent specification, the claimed inventions improve upon the prior art processes by ignoring nets that are unaffected by an ECO in performing routing following the ECO. This has the advantage of substantially reducing the impact on design schedule of ECOs and other layout changes, thus increasing the efficiency of the design process and making it easier to improve the design and fix design errors without unduly delaying time-to-market. By making it easier to fix errors as they are found, and causing substantially less incremental delay upon finding and fixing errors, the claimed inventive processes also increase the performance and reliability of the finished product. Because of the claimed inventive processes, individual less impactful design issues that still impact design performance (albeit not on a critical scale) can be caught and fixed without costing the same delay as more substantial errors.

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COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,231,626

33. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

34. The ’626 patent is valid and enforceable under the United States Patent Laws.

35. Bell Semic owns, by assignment, all right, title, and interest in and to the ’626 patent, including the right to collect for past damages.

36. A copy of the ’626 patent is attached at Exhibit A.

37. On information and belief, Lattice has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’626 patent by using the patented methodology to design one or more semiconductor devices, including as one example the Lattice Accused Prodcut, in the United States.

38. On information and belief, Lattice employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to perform incremental routing in implementing an ECO (the “Accused Processes”) as recited in the ’626 patent claims. As one example, Lattice’s Accused Processes perform a method for only routing the nets affected by the ECO and merging that changed area into the overall circuit layout as required by claim 1 of the ’626 patent. Miccron does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to perform incremental routing as part of implementing an ECO for the Lattice Accused Product to generate a revised integrated circuit design.

39. Lattice’s Accused Processes also calculate and perform a parasitic extraction only for each net in the IC design enclosed by the window defining the ECO. (This parasitic extraction is also how the Accused Processes further calculate a net delay only for each net in the IC design enclosed by the window defining the ECO.) Lattice does so by employing a design tool, such as

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at least one of the Cadence, Synopsys, and/or Siemens tools, to perform the incremental routing during implementation of the ECO for the Lattice Accused Product's circuit designs.

40. Lattice's Accused Processes also perform a design rule check only for each net in the IC design enclosed by the ECO window. Lattice does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, perform the incremental ECO and automatically perform a DRC for those nets to ensure that the ECO did not violate any design rules when it fixed other issues.

41. An exemplary infringement analysis showing infringement of one or more claims of the '626 patent is set forth in Exhibit B. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit C and further describes Lattice's infringement of the '626 patent.

42. Lattice's Accused Processes infringe and continue to infringe one or more claims of the '626 patent during the pendency of the '626 patent.

43. On information and belief, Lattice has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the '626 patent. Lattice has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the '626 patent.

44. Lattice's infringement of the '626 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

45. Bell Semic has been damaged by Lattice's infringement of the '626 patent and will

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continue to be damaged unless Lattice is enjoined by this Court. Bell Semic has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

46. Bell Semic is entitled to recover from Lattice all damages that Bell Semic has sustained as a result of Lattice's infringement of the '626 patent, including without limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

(a) a judgment declaring that Lattice has infringed one or more claims of the '626 patent in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;

(b) an award of damages adequate to compensate Bell Semic for infringement of the '626 patent by Lattice, in an amount to be proven at trial, including supplemental post-verdict damages until such time as Lattice ceases its infringing conduct;

(c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting Lattice and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with Lattice from committing further acts of infringement;

(d) a judgment requiring Lattice to make an accounting of damages resulting from Lattice's infringement of the '626 patent;

(e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;

(f) pre-judgment and post-judgment interest at the maximum amount permitted by law;

(g) all other relief, in law or equity, to which Bell Semic is entitled.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

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Dated: October 13, 2022

/s/ Jeff S. Pitzer

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Attorneys for Plaintiff Bell Semiconductor, LLC

EXHIBIT A

US007231626B2

(12) **United States Patent**
Hoff et al.

(10) **Patent No.: US 7,231,626 B2**
(45) **Date of Patent: Jun. 12, 2007**

(54) **METHOD OF IMPLEMENTING AN ENGINEERING CHANGE ORDER IN AN INTEGRATED CIRCUIT DESIGN BY WINDOWS**

(75) Inventors: **Jason K. Hoff**, Houston, TX (US); **Viswanathan Lakshmanan**, Thornton, CO (US); **Michael Josephides**, Broomfield, CO (US); **Daniel W. Prevedel**, Fort Collins, CO (US); **Richard D. Blinne**, Ft. Collins, CO (US); **Johathan P. Kuppinger**, Windsor, CO (US)

(73) Assignee: **LSI Corporation**, Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 221 days.

(21) Appl. No.: **11/015,123**

(22) Filed: **Dec. 17, 2004**

(65) **Prior Publication Data**

US 2006/0136855 A1 Jun. 22, 2006

(51) **Int. Cl.**
G06F 17/50 (2006.01)

(52) **U.S. Cl.** **716/13**; 716/14; 716/9; 716/10; 716/6

(58) **Field of Classification Search** 716/13, 716/14, 9, 10, 5, 6
See application file for complete search history.

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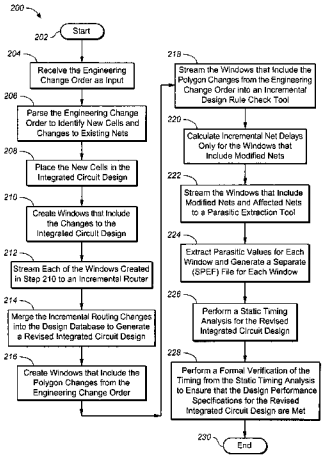
Primary Examiner—Phallaka Kik
(74) *Attorney, Agent, or Firm*—Eric J. Whitesell

(57) **ABSTRACT**

A method of implementing an engineering change order includes steps of: (a) receiving as input an integrated circuit design; (b) receiving as input an engineering change order to the integrated circuit design; (c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design; (d) performing a routing of the integrated circuit design that excludes routing of any net that is not enclosed by the window; (e) replacing an area in a copy of the integrated circuit design that is bounded by the coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and (f) generating as output the revised integrated circuit design.

8 Claims, 5 Drawing Sheets



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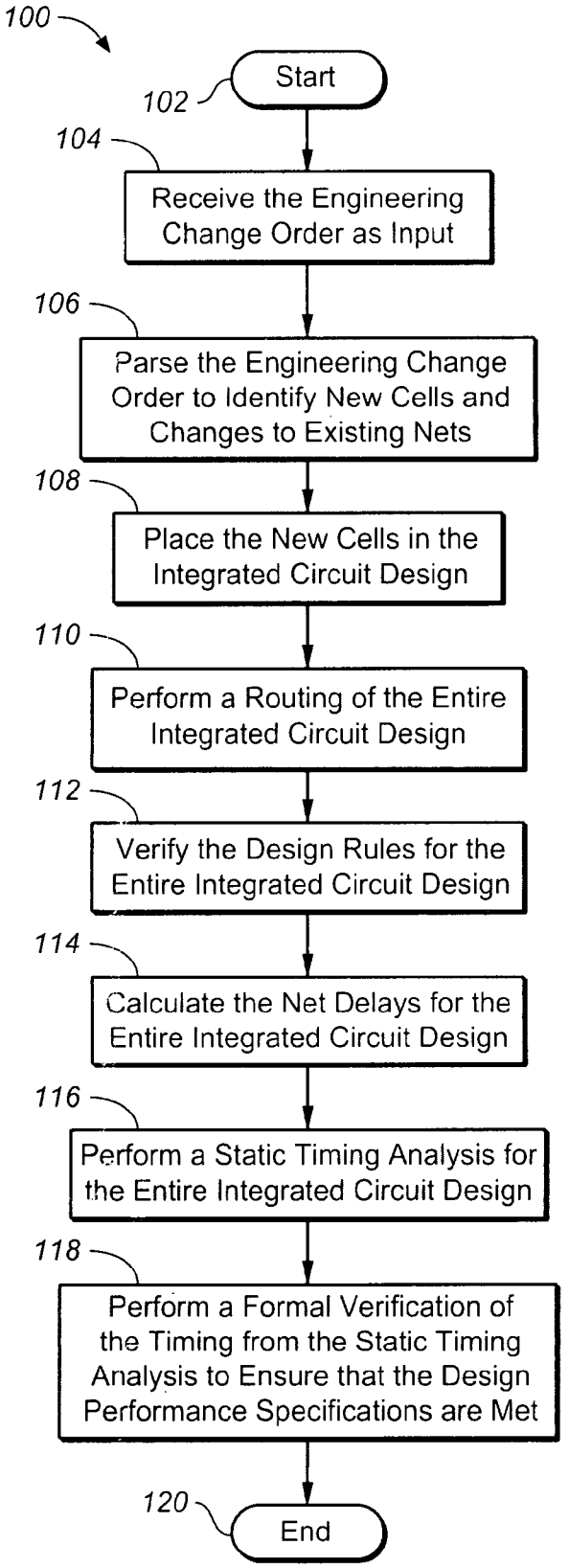

100
Start
102
104
Receive the Engineering Change Order as Input
106
Parse the Engineering Change Order to Identify New Cells and Changes to Existing Nets
108
Place the New Cells in the Integrated Circuit Design
110
Perform a Routing of the Entire Integrated Circuit Design
112
Verify the Design Rules for the Entire Integrated Circuit Design
114
Calculate the Net Delays for the Entire Integrated Circuit Design
116
Perform a Static Timing Analysis for the Entire Integrated Circuit Design
118
Perform a Formal Verification of the Timing from the Static Timing Analysis to Ensure that the Design Performance Specifications are Met
120
End

FIG. 1

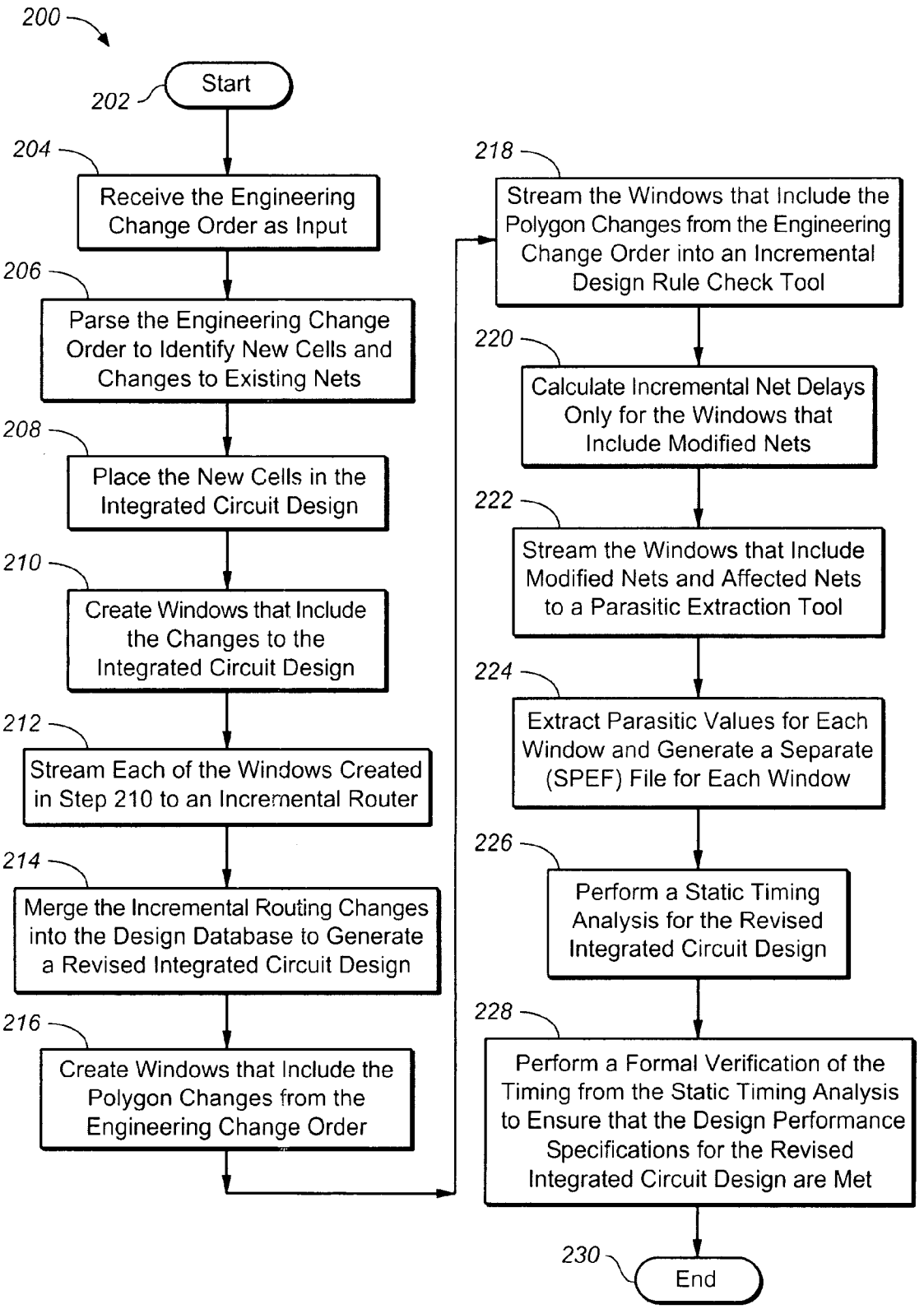

200
Start
202
204
Receive the Engineering Change Order as Input
206
Parse the Engineering Change Order to Identify New Cells and Changes to Existing Nets
208
Place the New Cells in the Integrated Circuit Design
210
Create Windows that Include the Changes to the Integrated Circuit Design
212
Stream Each of the Windows Created in Step 210 to an Incremental Router
214
Merge the Incremental Routing Changes into the Design Database to Generate a Revised Integrated Circuit Design
216
Create Windows that Include the Polygon Changes from the Engineering Change Order
218
Stream the Windows that Include the Polygon Changes from the Engineering Change Order into an Incremental Design Rule Check Tool
220
Calculate Incremental Net Delays Only for the Windows that Include Modified Nets
222
Stream the Windows that Include Modified Nets and Affected Nets to a Parasitic Extraction Tool
224
Extract Parasitic Values for Each Window and Generate a Separate (SPEF) File for Each Window
226
Perform a Static Timing Analysis for the Revised Integrated Circuit Design
228
Perform a Formal Verification of the Timing from the Static Timing Analysis to Ensure that the Design Performance Specifications for the Revised Integrated Circuit Design are Met
230
End

FIG. 2

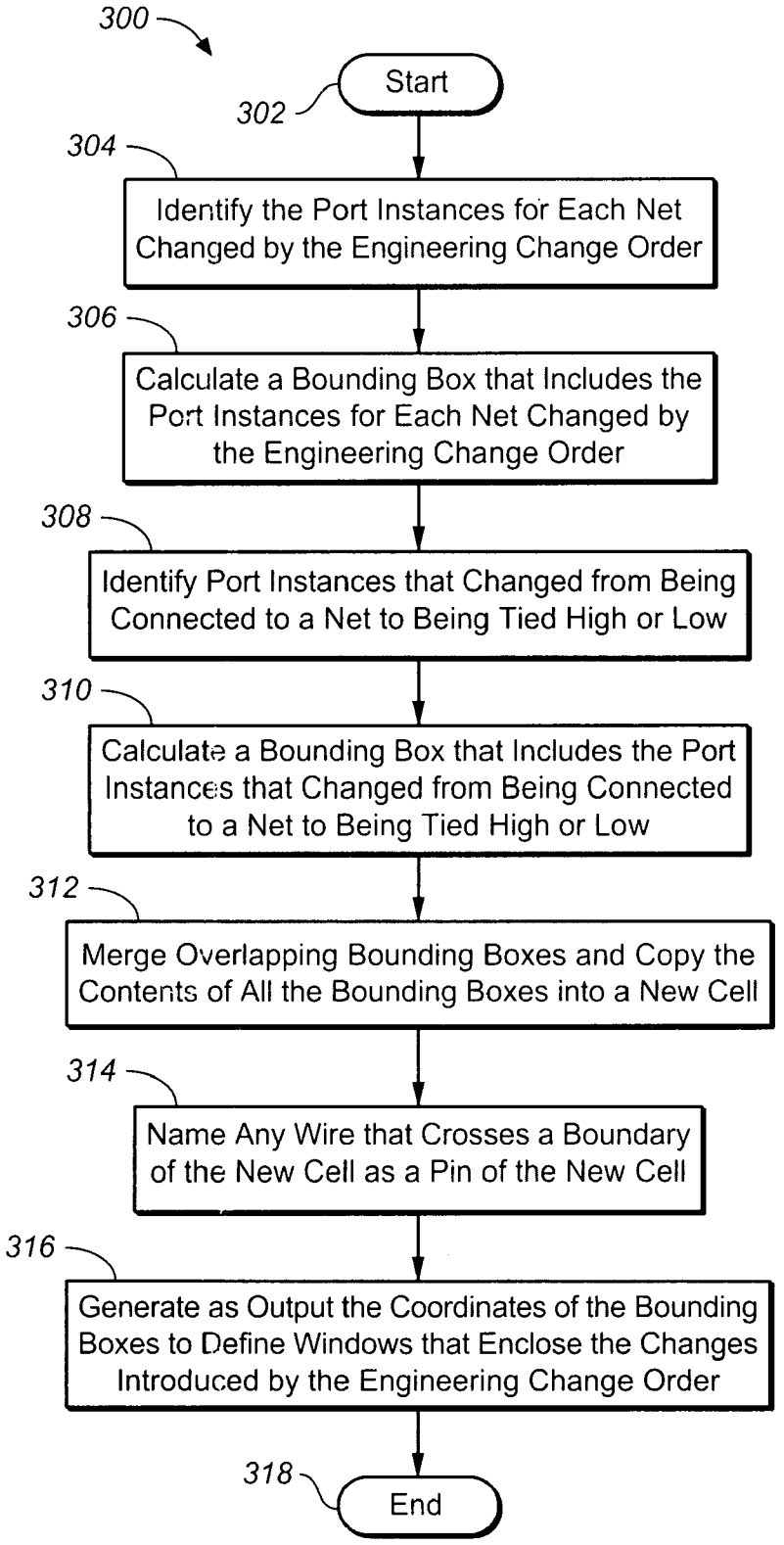

300
Start
302
304
Identify the Port Instances for Each Net Changed by the Engineering Change Order
306
Calculate a Bounding Box that Includes the Port Instances for Each Net Changed by the Engineering Change Order
308
Identify Port Instances that Changed from Being Connected to a Net to Being Tied High or Low
310
Calculate a Bounding Box that Includes the Port Instances that Changed from Being Connected to a Net to Being Tied High or Low
312
Merge Overlapping Bounding Boxes and Copy the Contents of All the Bounding Boxes into a New Cell
314
Name Any Wire that Crosses a Boundary of the New Cell as a Pin of the New Cell
316
Generate as Output the Coordinates of the Bounding Boxes to Define Windows that Enclose the Changes Introduced by the Engineering Change Order
318
End

FIG. 3

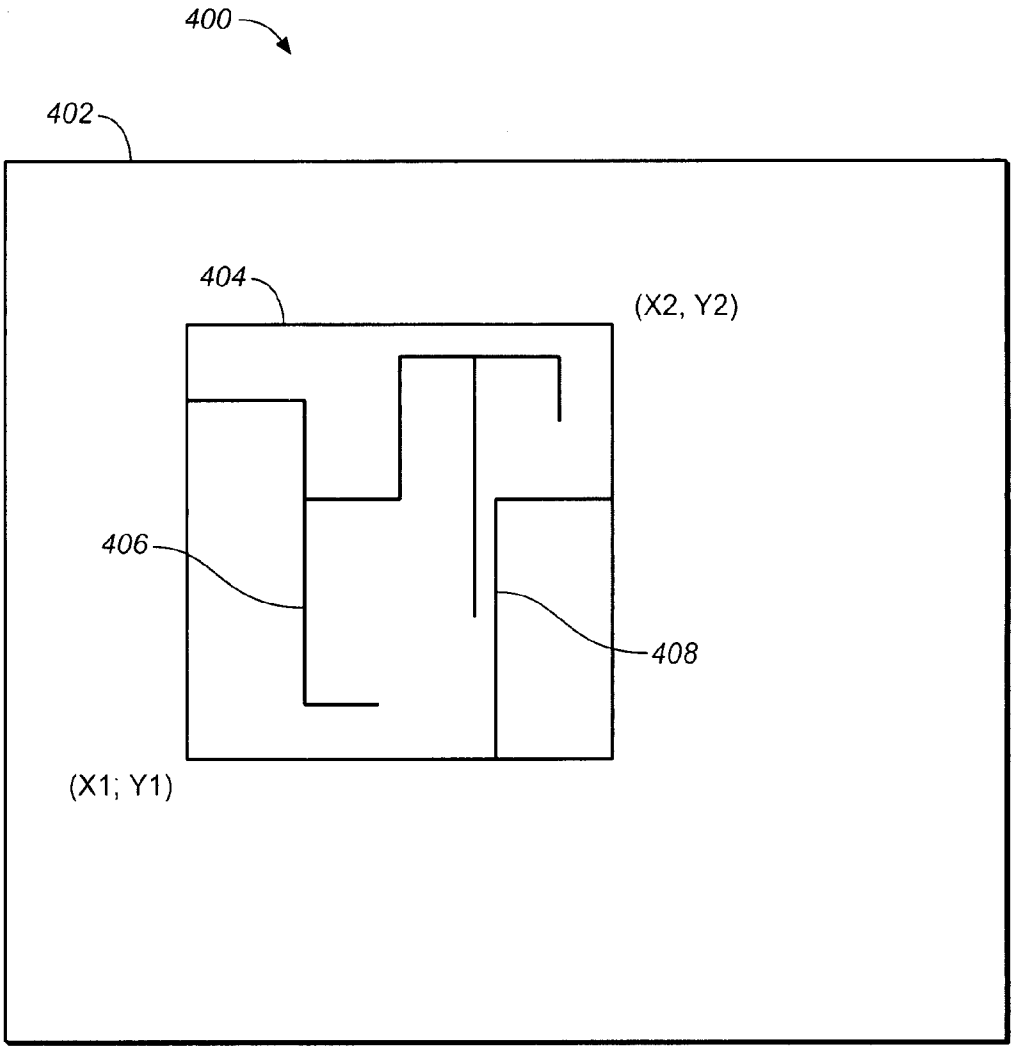


FIG. 4

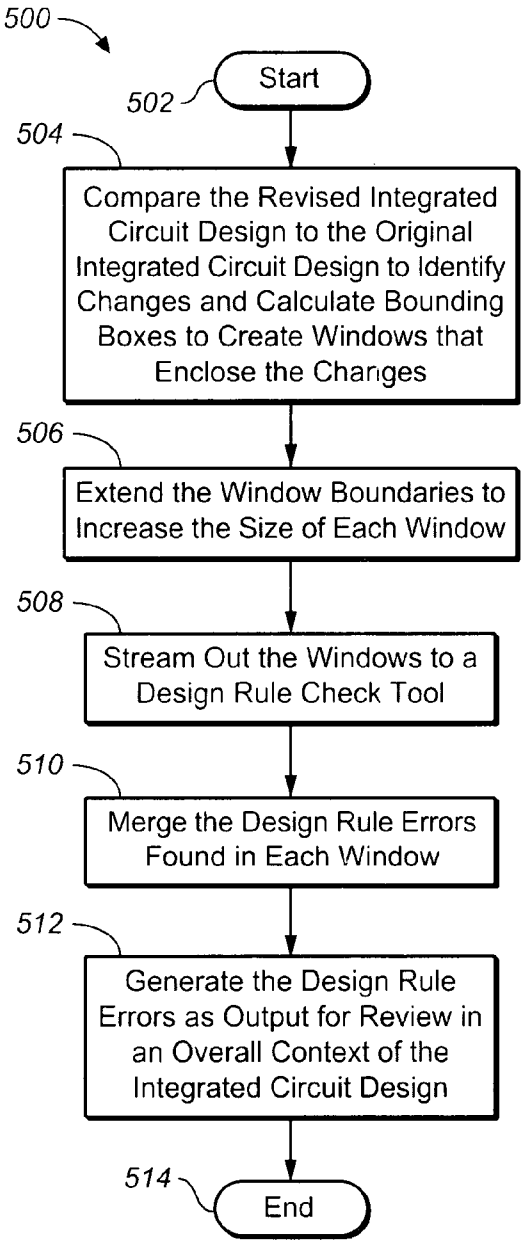

500
Start
502
504
Compare the Revised Integrated Circuit Design to the Original Integrated Circuit Design to Identify Changes and Calculate Bounding Boxes to Create Windows that Enclose the Changes
506
Extend the Window Boundaries to Increase the Size of Each Window
508
Stream Out the Windows to a Design Rule Check Tool
510
Merge the Design Rule Errors Found in Each Window
512
Generate the Design Rule Errors as Output for Review in an Overall Context of the Integrated Circuit Design
514
End

FIG. 5

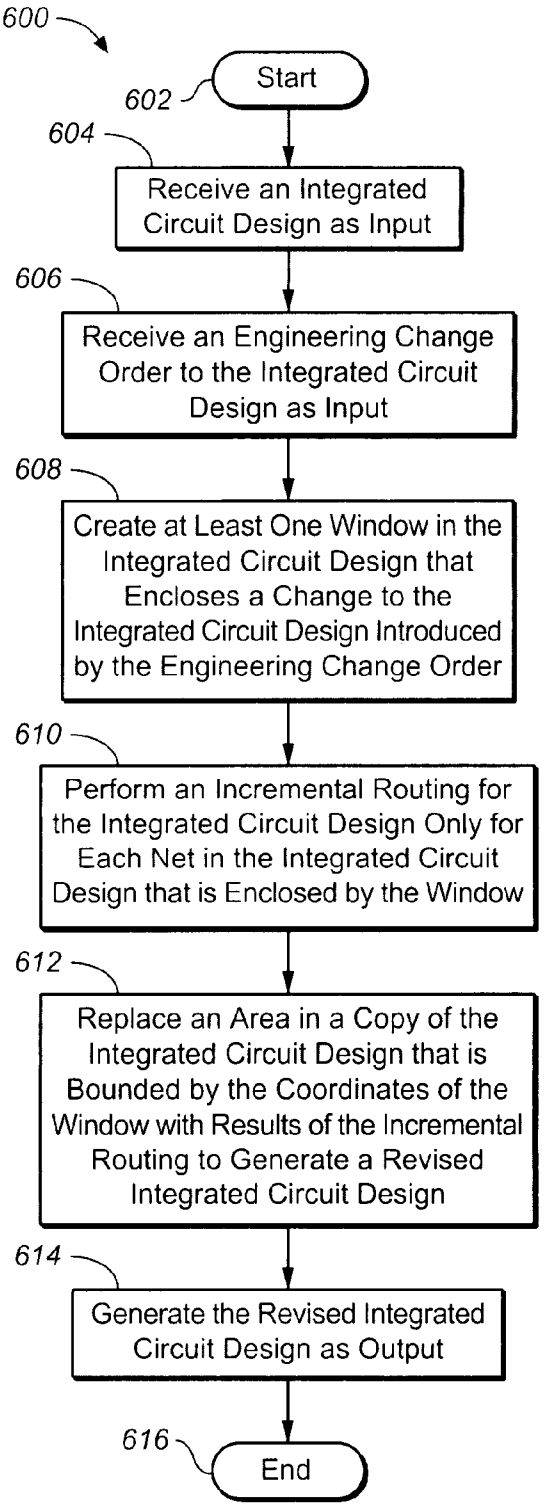

600
Start
602
604
Receive an Integrated Circuit Design as Input
606
Receive an Engineering Change Order to the Integrated Circuit Design as Input
608
Create at Least One Window in the Integrated Circuit Design that Encloses a Change to the Integrated Circuit Design Introduced by the Engineering Change Order
610
Perform an Incremental Routing for the Integrated Circuit Design Only for Each Net in the Integrated Circuit Design that is Enclosed by the Window
612
Replace an Area in a Copy of the Integrated Circuit Design that is Bounded by the Coordinates of the Window with Results of the Incremental Routing to Generate a Revised Integrated Circuit Design
614
Generate the Revised Integrated Circuit Design as Output
616
End

FIG. 6

METHOD OF IMPLEMENTING AN ENGINEERING CHANGE ORDER IN AN INTEGRATED CIRCUIT DESIGN BY WINDOWS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the design of integrated circuits. More specifically, but without limitation thereto, the present invention relates to methods of implementing an engineering change order (ECO) in an integrated circuit design.

2. Description of Related Art

In previous methods for implementing an engineering change order (ECO) request in an integrated circuit design, design tools are run for the entire integrated circuit design, even though the engineering change order typically is only a small fraction of the size of the integrated circuit design. For example, cell placement, routing, design rule check validation, and timing closure run times typically scale with the size of the entire integrated circuit design.

SUMMARY OF THE INVENTION

In one embodiment of the present invention, a method of implementing an engineering change order in an integrated circuit design by windows includes steps of:

(a) receiving as input an integrated circuit design;

(b) receiving as input an engineering change order to the integrated circuit design;

(c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;

(d) performing a routing only for each net in the integrated circuit design that is enclosed by the window;

(e) replacing an area in a copy of the integrated circuit design that is bounded by coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and

(f) generating as output the revised integrated circuit design.

In another embodiment of the present invention, a computer program product for implementing an engineering change order in an integrated circuit design by windows includes:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input an integrated circuit design;

(b) receiving as input an engineering change order to the integrated circuit design;

(c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;

(d) performing a routing of the integrated circuit design only for each net in the integrated circuit design that is enclosed by the window;

(e) replacing an area in a copy of the integrated circuit design that is bounded by coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and

(f) generating as output the revised integrated circuit design.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements throughout the several views of the drawings, and in which:

FIG. **1** illustrates a flow chart for a method of implementing an engineering change order in an integrated circuit design according to the prior art;

FIGS. **2**A and **2**B illustrate a flow chart for a method of implementing an engineering change order in an integrated circuit design by windows;

FIG. **3** illustrates a flow chart for creating an engineering change order window for FIGS. **2**A and **2**B;

FIG. **4** illustrates a diagram of a window in an integrated circuit design;

FIG. **5** illustrates a flow chart for performing an incremental design rule check for FIGS. **2**A and **2**B; and

FIG. **6** illustrates a flow chart of a computer program for implementing an engineering change order in an integrated circuit design by windows.

Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some elements in the figures may be exaggerated relative to other elements to point out distinctive features in the illustrated embodiments of the present invention.

DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

In previous methods for implementing a functional or timing engineering change order (ECO) to an integrated circuit design, the typical turnaround time is typically about one week regardless of the size of the engineering change order. This is because although the engineering change order may only have a size of a few cells, it must be merged with an integrated circuit design that typically has a much greater size. For example, if an engineering change order for five cells may be required for an integrated circuit design that includes five million cells. As a result, design tool run times generally scale with the size of the entire integrated circuit design for routing, design rule check verification, net delay calculation, and parasitic extraction. Preferably, the time required to implement an engineering change order should depend on the number of net changes in the engineering change order rather than on the total number of nets in the entire integrated circuit design.

FIG. **1** illustrates a flow chart **100** for a method of implementing an engineering change order according to the prior art.

Step **102** is the entry point for the flow chart **100**.

In step **104**, the engineering change order is received as input.

In step **106**, the engineering change order is parsed to identify new cells and changes to existing nets.

In step **108**, the new cells are placed in the integrated circuit design by a software place and route design tool.

In step **110**, a routing of the entire integrated circuit design is performed by the place and route design tool.

In step **112**, the design rules for the technology used to manufacture the integrated circuit are verified for the entire

integrated circuit design, for example, by design rule check software such as Mentor Calibre™.

In step **114**, the net delays are calculated for the entire integrated circuit design.

In step **116**, a parasitic extraction is performed for the entire integrated circuit design to determine the values of net coupling capacitance and parasitic resistance.

In step **118**, a static timing analysis is performed for the entire integrated circuit design to determine the effect of net delay including net parasitic capacitance and resistance on the integrated circuit design.

In step **120**, a formal verification of the timing is performed from the static timing analysis to ensure that the design timing specifications are met.

Step **122** is the exit point of the flow chart **100**.

In the method of FIG. **1**, steps **110**, **112**, **114** and **116** may be especially time consuming and resource intensive, depending on the complexity of the integrated circuit design. A significant savings in the resources required to perform routing, design rule check verification, net delay calculation, and parasitic extraction may be realized by creating windows in the integrated circuit design that include only the incremental changes to the overall integrated circuit design as follows.

In one embodiment of the present invention, a method of implementing an engineering change order in an integrated circuit design includes steps of:

(a) receiving as input an integrated circuit design;

(b) receiving as input an engineering change order to the integrated circuit design;

(c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;

(d) performing a routing only for each net in the integrated circuit design that is enclosed by the window;

(e) replacing an area in a copy of the integrated circuit design that is bounded by coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and

(f) generating as output the revised integrated circuit design.

FIGS. **2**A and **2**B illustrate a flow chart **200** for a method of implementing an engineering change order in an integrated circuit design by windows.

Step **202** is the entry point for the flow chart **200**.

In step **204**, the engineering change order is received as input as in FIG. **1**.

In step **206**, the engineering change order is parsed to identify new nets and changes to existing nets that constitute the changes to the integrated circuit design in the same manner as in FIG. **1**.

In step **208**, the new cells are placed in the integrated circuit design, for example, by a software place and route design tool in the same manner as FIG. **1**.

In step **210**, windows are created that include the new cells and the net changes that constitute the changes to the integrated circuit design that are to be routed. The term "window" as used herein is defined as a rectilinear boundary that encloses an area of the integrated circuit design that is less than the entire area of the integrated circuit design. For example, a window may include a subset of nets that have been changed by the engineering change order. Alternatively, a window may include polygons that have been introduced or changed by the engineering change order. The window boundaries are calculated from the coordinates of the new polygons and the changed nets in the integrated circuit design database so that each of the changes to the integrated circuit design is enclosed by a window.

In step **212**, each of the windows created in step **210** is streamed to an incremental router. The incremental routing may be performed by the same routing tool used in FIG. **1**, however, only the nets that are modified by the engineering change order are routed, in contrast to routing the entire integrated circuit design as in FIG. **1**. Windows that do not overlap may be routed in parallel, while windows that do overlap are routed serially so that any duplicated routing may be removed. If any nets in a window are found open, that is, not all of the net connections are included in the window, then the net is "frozen", which means that the net may not be changed by the router. In addition, a partition manager is preferably included in the incremental router that allows the user to expand the size of the windows and merge overlapping windows.

In step **214**, the incremental routing changes are merged into the design database, for example, by replacing the contents enclosed by the coordinates of each window in a copy of the original integrated circuit design by the contents of the window to generate a revised integrated circuit design.

In step **216**, windows are created that include the polygon changes from the engineering change order.

In step **218**, the windows that include the polygon changes from the engineering change order are streamed into an incremental design rule check tool. The incremental design rule check tool checks only the polygons that were changed, advantageously avoiding unnecessary re-checking of the all the polygons in the integrated circuit database.

In step **220**, incremental net delays are calculated only for the windows that include modified nets, advantageously avoiding unnecessary re-calculation of all the net delays in the integrated circuit design.

In step **222**, the windows that include modified nets and affected nets are streamed to a parasitic extraction tool. An affected net is a net that has a coupling capacitance with a modified net that exceeds a predefined coupling capacitance threshold.

In step **224**, parasitic values are extracted for each window, and a separate standard parasitic extraction format (SPEF) file is generated by the parasitic extraction tool for each window.

In step **226**, a static timing analysis is performed for the revised integrated circuit design in the same manner as in FIG. **1**.

In step **228**, a formal verification of the timing is performed from the static timing analysis to ensure that the design performance specifications for the revised integrated circuit design are met in the same manner as in FIG. **1**.

Step **230** is the exit point of the flow chart **200**.

FIG. **3** illustrates a flow chart **300** for creating an engineering change order window for FIG. **2**.

Step **302** is the entry point of the flow chart **300**.

In step **304**, the port instances for each net changed by the engineering change order are identified. A net change may be, for example, a net that has moved or has different connections.

In step **306**, a bounding box that includes the port instances for each net changed by the engineering change order is calculated from the net coordinates in the design database of the original integrated circuit design.

In step **308**, port instances that changed from being connected to a net to being tied high or low are identified.

In step **310**, a bounding box that includes the port instances that changed from being connected to a net to being tied high or low is calculated from the coordinates in the design database.

In step **312**, overlapping bounding boxes are merged, and the contents of all the bounding boxes are copied into a new cell.

In step **314**, any wire that crosses a boundary of the new cell is named as a pin of the new cell.

In step **316**, the coordinates of the bounding boxes are generated as output to define windows that enclose the changes introduced by the engineering change order.

Step **318** is the exit point of the flow chart **300**.

FIG. **4** illustrates a diagram of a window in an integrated circuit design. Shown in FIG. **4** are an integrated circuit design **402**, a window **404**, a changed net **406**, and an affected net **408**.

In FIG. **4**, The window **404** is bounded by the coordinates (X**1**, Y**1**):(X**2**, Y**2**) that enclose the changed net **406** and the affected net **408**. The area enclosed by the window **404** is less than the entire area of the integrated circuit design **402**, thereby reducing the number of calculations required to implement the engineering change order.

In this example, the changed net **406** has been moved, resulting in a coupling capacitance with the affected net **408** that exceeds a threshold coupling capacitance. The affected net **408** is therefore included in the window for calculating the incremental net delay and for performing the parasitic extraction.

FIG. **5** illustrates a flow chart **500** for performing an incremental design rule check for FIGS. **2**A and **2**B

Step **502** is the entry point of the flow chart **500**.

In step **504**, the revised integrated circuit design is compared to the original integrated circuit design to identify changes, and bounding boxes are calculated to create windows that enclose only the physical changes and not the entire nets.

In step **506**, the window boundaries are extended to increase the size of each window, forming a halo margin or region around each window. The halo region allows the design rule check software to examine objects that are nearby each window. The size of the halo margin may be determined, for example, by the design rule check tool or by the user to ensure that there is sufficient room for the spacing rules to work correctly.

In step **508**, the windows are streamed out, for example, in GDSII format, to a design rule check tool, which may be the same as that used in FIG. **1**.

In step **510**, the design rule errors found in each window are merged together, removing any errors in the halo region.

In step **512**, the design rule errors are generated as output for review in an overall context of the integrated circuit design.

Step **514** is the exit point of the flow chart **500**.

The flow chart described above may also be implemented by instructions for being performed on a computer. The instructions may be embodied in a disk, a CD-ROM, and other computer readable media according to well known computer programming techniques.

In another aspect of the present invention, a computer program product for analyzing noise for an integrated circuit design includes:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input an integrated circuit design;

(b) receiving as input an engineering change order to the integrated circuit design;

(c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;

(d) performing a routing only for each net in the integrated circuit design that is enclosed by the window;

(e) replacing an area in a copy of the integrated circuit design that is bounded by coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and

(f) generating as output the revised integrated circuit design.

FIG. **6** illustrates a flow chart **600** of a computer program for implementing an engineering change order in an integrated circuit design by windows.

Step **602** is the entry point of the flow chart **600**.

In step **604**, an integrated circuit design is received as input.

In step **606**, an engineering change order to the integrated circuit design is received as input.

In step **608**, at least one window is created in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order. The window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design.

In step **610**, an incremental routing is performed for the integrated circuit design only for each net in the integrated circuit design that is enclosed by the window, advantageously avoiding repeating calculations for nets that are not changed or affected by the engineering change order.

In step **612**, an area in a copy of the integrated circuit design that is bounded by the coordinates of the window is replaced with results of the incremental routing to generate a revised integrated circuit design.

In step **614**, the revised integrated circuit design is generated as output.

Step **616** is the exit point of the flow chart **600**.

Although the methods illustrated by the flowchart descriptions above are described and shown with reference to specific steps performed in a specific order, these steps may be combined, sub-divided, or reordered without departing from the scope of the claims. Unless specifically indicated herein, the order and grouping of steps are not limitations of the claims.

The specific embodiments and applications thereof described above are for illustrative purposes only and do not preclude modifications and variations that may be made thereto by those skilled in the art within the scope of the following claims.

What is claimed is:

1. A method comprising steps of:

(a) receiving as input an integrated circuit design;

(b) receiving as input an engineering change order to the integrated circuit design;

(c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;

(d) performing an incremental routing of the integrated circuit design only for each net in the integrated circuit design that is enclosed by the window;

(e) replacing an area in a copy of the integrated circuit design that is bounded by the coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and

(f) generating as output the revised integrated circuit design.

2. The method of claim **1** further comprising a step of calculating a net delay only for each net in the integrated circuit design that is enclosed by the window.

3. The method of claim **1** further comprising a step of performing a design rule check only for each net in the integrated circuit design that is enclosed by the window.

4. The method of claim **1** further comprising a step of performing a parasitic extraction only for each net in the integrated circuit design that is enclosed by the window.

5. A computer readable storage medium tangibly embodying instructions for a computer that when executed by the computer implement a method for implementing an engineering change order in an integrated circuit design by windows, the method comprising steps of:

(a) receiving as input an integrated circuit design;

(b) receiving as input an engineering change order to the integrated circuit design;

(c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;

(d) performing an incremental routing only for each net in the integrated circuit design that is enclosed by the window;

(e) replacing an area in a copy of the integrated circuit design that is bounded by coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and

(f) generating as output the revised integrated circuit design.

6. The computer readable storage medium of claim **5** wherein the method further comprises a step of calculating a net delay only for each net in the integrated circuit design that is enclosed by the window.

7. The computer readable storage meduim of claim **5** wherein the method further comprises a step of performing a design rule check only for each net in the integrated circuit design that is enclosed by the window.

8. The computer readable storage medium of claim **5** wherein the method further comprises a step of performing a parasitic extraction only for each net in the integrated circuit design that is enclosed by the window.

* * * * *

EXHIBIT B

BELL SEMICONDUCTOR LLC'S ANALYSIS OF INFRINGEMENT

U.S. Patent No. 7,231,626

Claims 1-4

Bell Semiconductor, LLC ("Bell Semiconductor") provides evidence of infringement of exemplary claims 1-4 of U.S. Patent No. 7,231,626 ("the '626 patent") by the LCMX02-7000HC produced by Lattice Semiconductor Corporation ("Lattice"). In support thereof, Bell Semiconductor provides the following claim charts.

"Accused Products" as used herein refers to the Lattice circuit designs and/or semiconductor products, including at least the LCMX02-7000HC, that are made, produced, and/or processed by a design tool, such as a Cadence Design Systems, Inc. ("Cadence") tool, by implementing an engineering change order through a window that is less than the entire area of the integrated circuit design. On information and belief, these design tools all function similarly with respect to the functionality described herein. For simplicity, the Cadence tool will be the primary tool cited herein to illustrate infringement of the claimed methods. These claim charts demonstrate infringement by comparing each element of the asserted claims to corresponding components, aspects, and/or features of the Accused Products. These claim charts are not intended to constitute an expert report on infringement. These claim charts include information provided by way of example, and not by way of limitation.

The analysis set forth below is based only upon information from publicly available resources regarding the Accused Products, as Lattice and relevant third parties have not yet provided any non-public information. An analysis of non-public technical documentation may assist in further identifying all infringing features and functionality. Accordingly, Bell Semiconductor reserves the right to supplement this infringement analysis once such information is made available to Bell Semiconductor. Furthermore, Bell Semiconductor reserves the right to revise this infringement analysis, as appropriate, upon issuance of a court order construing any terms recited in the asserted claims or as other circumstances so merit.

Bell Semiconductor contends that each element of each claim asserted herein is literally met, and would also be met under the doctrine of equivalents, as there are no substantial differences between the Accused Products and the elements of the patent claims in function, way, and result. If Lattice attempts to argue that there is no literal infringement and/or if Lattice attempts to draw any distinction between the claimed functionality and the Accused Products, then Bell Semiconductor reserves the right to rebut the alleged distinction as a matter of literal infringement and/or as to whether any such distinction is substantial under the doctrine of equivalents.

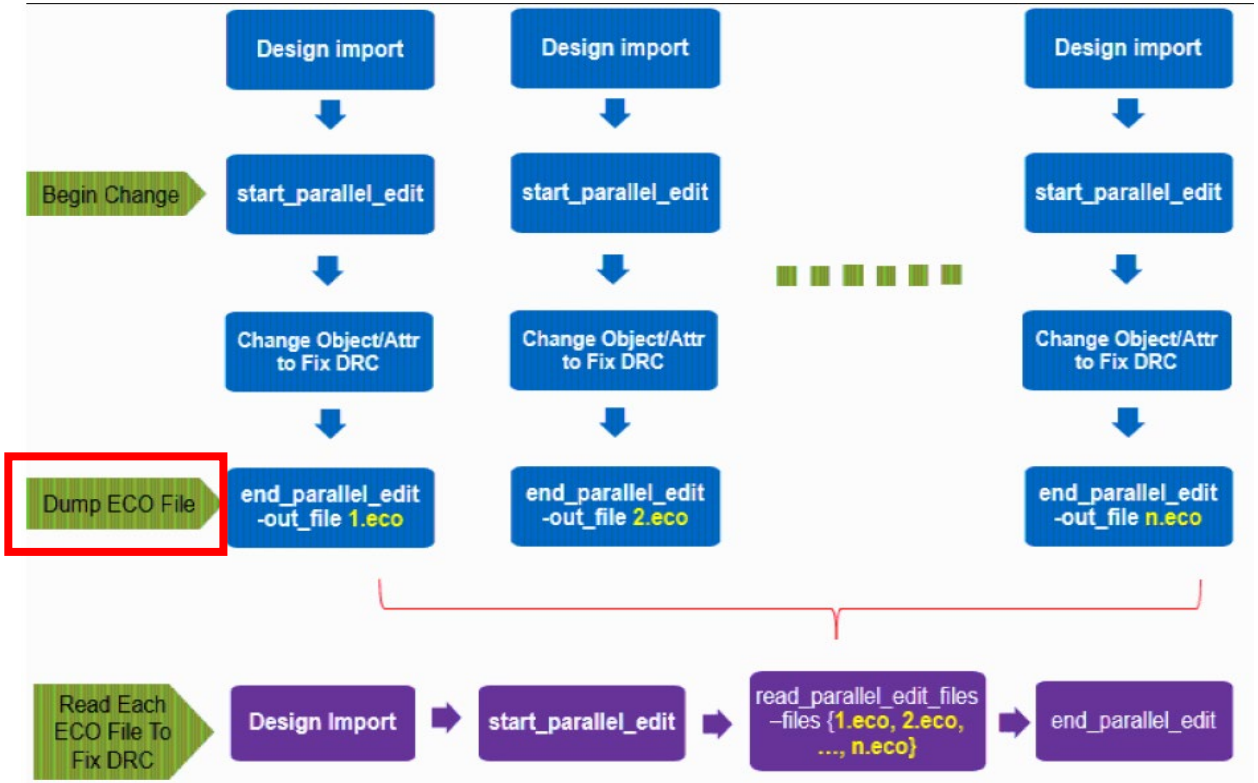
Unless otherwise noted, the cited evidence applies across each of Lattice's products that were made, produced, or processed from a circuit design using windows, including but not limited to LCMX02-7000HC. Bell Semiconductor reserves the right to amend this infringement analysis based on other products made, produced, or processed in the same or similar manner to that identified herein.

CLAIM CHARTS
U.S. Patent No. 7,231,626

Claim 1	Accused Product
1. A method comprising steps of:	To the extent the preamble is limiting, the Accused Products are produced by performing the method steps outlined in the remaining claim elements. **Running ECO Routing** The NanoRoute router performs ECO routing by completing partial routes with added logic while maintaining the existing wire segments as much as possible. ECO routing is useful in cases such as the following: • After the chip is initially routed, the customer or chip owner gives you a new netlist with minor changes. • After the chip is initially routed, buffers were added to repair setup or hold violations or DRVs during physical optimization. • Buffers were added or gates were resized during hand editing of a routed design. • Antenna diodes were added interactively after routing to repair process antenna violations. • After metal fill is added to the design.

Parallel Edit Flow

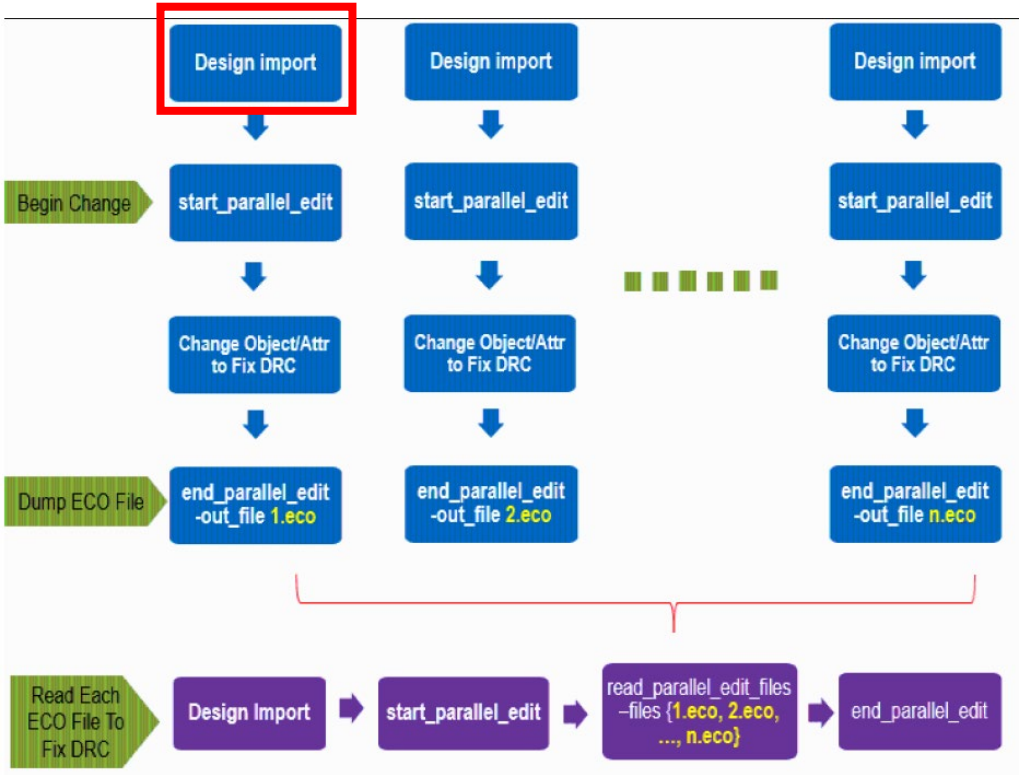
The parallel editing flow can enable multiple users to make physical and logic ECO changes at the same time on different areas of a design. It can support a wide range of basic wire editing and ECO operations, such as modifying or adding a wire or via or modifying logical connections.



See Innovus User Guide product version 20.10, March 2020, pages 682 and 1583.

For example, Lattice creates a circuit design for LCMX02-7000HC, which was made, produced, or processed from that circuit design created using one or more of the above-identified and described design tools that use windows.

CLAIM CHARTS
U.S. Patent No. 7,231,626

(a) receiving as input an integrated circuit design;	The Accused Products are made, produced, or processed from a circuit design that is created by receiving as input an integrated circuit design. For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from that circuit design that is created using one or more of the above-identified and described design tools such that it receives a design through its import and/or loading procedures. The steps in the parallel edit flow are detailed below: 1. Import or restore the design in which you want to make parallel edits along with other users. 

	Step 1
	Load the entire chip into Innovus and use `start_parallel_edit -region {Area1_coordinates}` to specify the area in which ECO changes are required. After the relevant operation is completed, use the `end_parallel_edit -out_file 1.eco` command to record the changes to the chip in the `1.eco` file. The specific example script and ECO file are as follows:
	Example script
	`restoreDesign fullchip.enc.dat fullchip`
	`start_parallel_edit -area_restricted -region {0.0 0.0 104.04 102.976}`
	`ecoDeleteRepeater -inst instB/A0B_inst`
	`end_parallel_edit -out_file diff_1`
	`exit`
	See Innovus User Guide product version 20.10, March 2020, pages 1583 and 1590.

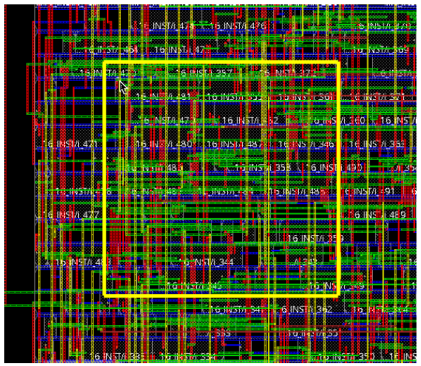
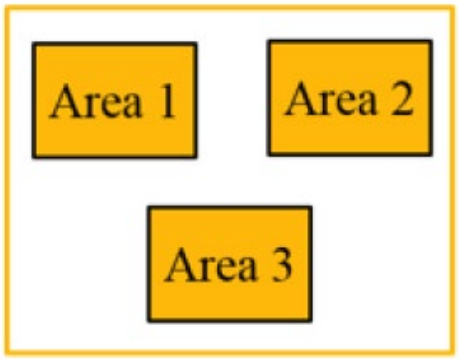
(b) receiving as input an engineering change order to the integrated circuit design;	The Accused Products are made, produced, or processed from a circuit design that is created by receiving as input an engineering change order to the integrated circuit design. 2. Initialize parallel editing by using the `start_parallel_edit` command. The `start_parallel_edit` command is used to define the area where you need to perform DRC fixing or ECO operations. The command draws a yellow square on the main window to indicate the edit area and saves the physical data, net attributes, via cell names, and Non-Default Rules (NDRs) to multiple binary files. Use the `-region {x1 y1 x2 y2}` parameter to specify the coordinates of the edit area. Specify the `-area_restricted` parameter to write out only the different objects inside or touching the specified edit area. This is a strict interpretation of the region, and ignores the changes made outside of the region. The other engineers should also initialize `start_parallel_edit` in their sessions separately to specify their own operating areas. Area overlap is not recommended because it might cause ECO conflicts.

Example ECO File

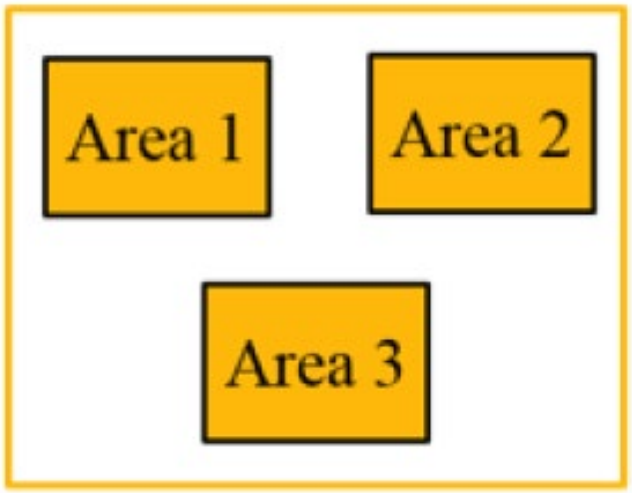
```
#####################################################
# Generated by:      Cadence Innovus 18.10-XXX_1
# OS:                Linux x86_64(Host ID ip-172-19-133-30)
# Generated on:      XXX XXX XXX
# Design:            fullchip
# Command:           end_parallel_edit -out_file 1.eco
#####################################################

##############################################
###  The difference for each net           ###
##############################################
DEL NET {{name instB/n_1} }
##############################################
###  The difference for each wire/via      ###
##############################################
ADD VIA {{bot_mask 0} {cut_mask 0} {net b_1} {pt {139050 114621}} {status unknown} {top_mask 0} {via_cell VIA23_1cut_N} }
ADD VIA {{bot_mask 0} {cut_mask 0} {net b_1} {pt {139050 64896}} {status unknown} {top_mask 0} {via_cell VIA12_1cut_E} }
ADD VIA {{bot_mask 0} {cut_mask 0} {net b_1} {pt {125176 114621}} {status unknown} {top_mask 0} {via_cell VIA12_1cut_E} }
ADD WIRE {{ext {32 32}} {layer M2} {mask 0} {net b_1} {pts {125176 114621 139050 114621}} {status unknown} }
ADD VIA {{bot_mask 0} {cut_mask 0} {net b_1} {pt {139050 64896}} {status unknown} {top_mask 0} {via_cell VIA23_1cut_N} }
ADD WIRE {{ext {32 32}} {layer M3} {mask 0} {net b_1} {pts {139050 64896 139050 114621}} {status unknown} }
DEL WIRE {{layer M3} {net b_1} {pts {139008 64896 139008 99712}} }
DEL WIRE {{layer M2} {net b_1} {pts {121296 99712 139008 99712}} }
DEL WIRE {{layer M2} {net b_1} {pts {139008 64896 139050 64896}} }
DEL VIA {{net b_1} {pt {121296 99712}} {via_cell NR_VIA1_VH} }
DEL VIA {{net b_1} {pt {139008 99712}} {via_cell NR_VIA2_HV} }
DEL VIA {{net b_1} {pt {139008 64896}} {via_cell NR_VIA2_HV} }
DEL VIA {{net b_1} {pt {139050 64896}} {via_cell NR_VIA1_VH} }
##############################################
### The difference for each instance       ###
##############################################
DEL INST {{name instB/AOB_inst} }
MODIFY INSTTERM {{inst instB/iso_pd2_0_out} {name I} {net b_1} }
```

See Innovus User Guide product version 20.10, March 2020, pages 1584 and 1591.

For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created by receiving as input an engineering change order ("ECO") to the integrated circuit design.

(c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;	The Accused Products are made, produced, or processed from a circuit design that is created by creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design. 2. Initialize parallel editing by using the `start_parallel_edit` command. The `start_parallel_edit` command is used to define the area where you need to perform DRC fixing or ECO operations. The command draws a yellow square on the main window to indicate the edit area and saves the physical data, net attributes, via cell names, and Non-Default Rules (NDRs) to multiple binary files. Use the `-region {x1 y1 x2 y2}` parameter to specify the coordinates of the edit area. Specify the `-area_restricted` parameter to write out only the different objects inside or touching the specified edit area. This is a strict interpretation of the region, and ignores the changes made outside of the region. The other engineers should also initialize `start_parallel_edit` in their sessions separately to specify their own operating areas. Area overlap is not recommended because it might cause ECO conflicts.   In the above step, ECO changes were made in `Area1` in the parallel editing mode. Similarly, ECO changes are made in `Area2` and `Area3`, and then `end_parallel_edit` is used to write the modified physical and logical information in these areas to the `2.eco` and 3.eco files, respectively. *See Innovus User Guide product version 20.10, March 2020, pages 1584 and 1590-91.*

	For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from that circuit design that is created by a using a parallel edit command that draws a square to enclose the edit area for the ECO. The edit area is less than an entire area of the integrated circuit design.

(d) performing an incremental routing of the integrated circuit design only for each net in the integrated circuit design that is enclosed by the window;	The Accused Products are made, produced, or processed from a circuit design that is created by performing an incremental routing of the integrated circuit design only for each net in the integrated circuit design that is enclosed by the window.
	
	3. Make DRC fixes on ECO changes in your assigned area in the design. Multiple engineers can work simultaneously on different areas in the design in the parallel edit mode.
	The following example shows the report information generated by `start_parallel_edit`.
	`<CMD> start_parallel_edit -region 0.0 0.0 500.4 431.6`
	`Saving net attribute and regular wire/via information`
	`Saving instance information`
	`Saving physical pin information`
	`Saving NDR rule information`
	`Saving routing blockage information`
	`Saving placement blockage information`
	`Saving special wire/via information`
	 

```
#############################################################
# Generated by:      Cadence Innovus 18.10-XXX_1
# OS:                Linux x86_64(Host ID ip-172-19-133-30)
# Generated on:      XXX XXX XXX
# Design:            fullchip
# Command:           end_parallel_edit -out_file 1.eco
#############################################################

################################################
##  The difference for each net               ##
################################################
DEL NET {{name instB/n_1} }
################################################
##  The difference for each wire/via          ##
################################################
ADD VIA {{bot_mask 0} {cut_mask 0} {net b_1} {pt {139050 114621}} {status unknown} {top_mask 0} {via_cell VIA23_1cut_N} }
ADD VIA {{bot_mask 0} {cut_mask 0} {net b_1} {pt {139050 64896}} {status unknown} {top_mask 0} {via_cell VIA12_1cut_E} }
ADD VIA {{bot_mask 0} {cut_mask 0} {net b_1} {pt {125176 114621}} {status unknown} {top_mask 0} {via_cell VIA12_1cut_E} }
ADD WIRE {{ext {32 32}} {layer M2} {mask 0} {net b_1} {pts {125176 114621 139050 114621}} {status unknown} }
ADD VIA {{bot_mask 0} {cut_mask 0} {net b_1} {pt {139050 64896}} {status unknown} {top_mask 0} {via_cell VIA23_1cut_N} }
ADD WIRE {{ext {32 32}} {layer M3} {mask 0} {net b_1} {pts {139050 64896 139050 114621}} {status unknown} }
DEL WIRE {{layer M3} {net b_1} {pts {139008 64896 139008 99712}} }
DEL WIRE {{layer M2} {net b_1} {pts {121296 99712 139008 99712}} }
DEL WIRE {{layer M2} {net b_1} {pts {139008 64896 139050 64896}} }
DEL VIA {{net b_1} {pt {121296 99712}} {via_cell NR_VIA1_VH} }
DEL VIA {{net b_1} {pt {139008 99712}} {via_cell NR_VIA2_HV} }
DEL VIA {{net b_1} {pt {139008 64896}} {via_cell NR_VIA2_HV} }
DEL VIA {{net b_1} {pt {139050 64896}} {via_cell NR_VIA1_VH} }
################################################
### The difference for each instance          ##
################################################
DEL INST {{name instB/AOB_inst} }
MODIFY INSTTERM {{inst instB/iso_pd2_0_out} {name I} {net b_1} }
```

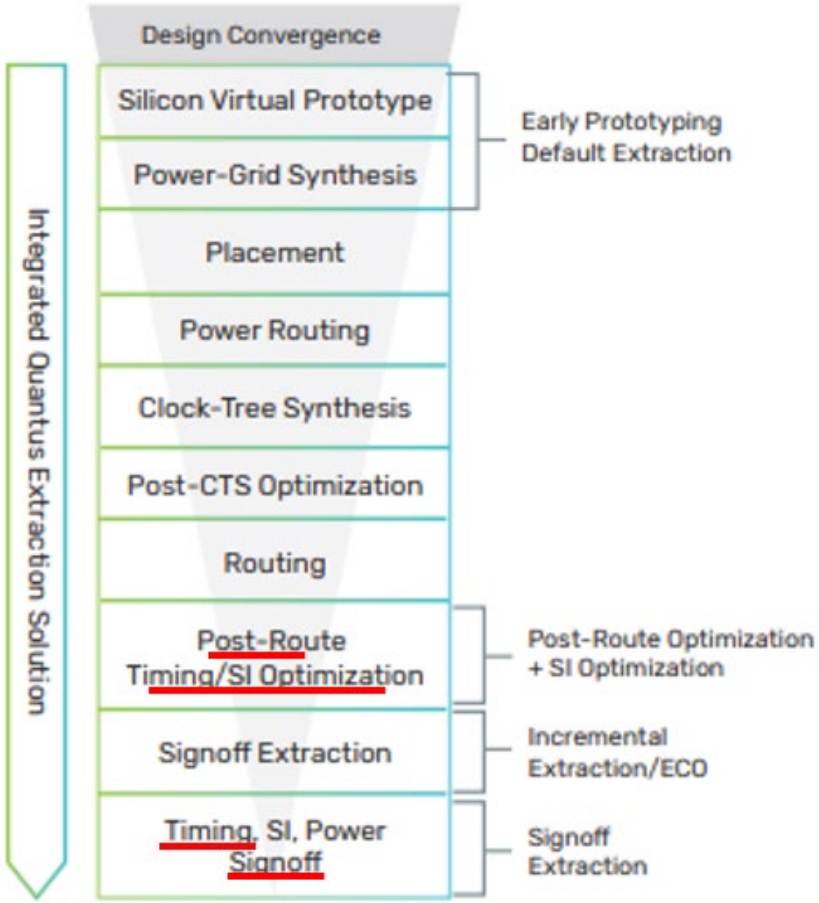
See Innovus User Guide product version 20.10, March 2020, pages 1585 and 1590-91.

For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from that circuit design that is created by performing an incremental routing of the integrated circuit design only for each net in the integrated circuit design that is enclosed by the square of the edit area.

(e) replacing an area in a copy of the integrated circuit design that is bounded by the coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and	The Accused Products are made, produced, or processed from a circuit design that is created by replacing an area in a copy of the integrated circuit design that is bounded by the coordinates of the window with results of the incremental routing to generate a revised integrated circuit design. **Step 2** Load the entire chip first and then read the eco files generated in the previous step by using the `read_parallel_edit_files` command. All the changes in different areas will be reflected in the chip. *See Innovus User Guide product version 20.10*, March 2020, pages 1585 and 1591. For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from that circuit design that is created by replacing an area in a copy of the integrated circuit design that is bounded by the square of the edit area with results of the incremental routing to generate a revised integrated circuit design.

(f) generating as output the revised integrated circuit design.	The Accused Products are made, produced, or processed from a circuit design that is created by generating as output the revised integrated circuit design.
	
	5. Load all parallel edit files by using the `read_parallel_edit_files` command.
	The `read_parallel_edit_files` command loads all the specified parallel edit files and implements the editing changes recorded in them. In case of any conflict in the parallel edit files, the tool implements changes as per the specified conflict mode and writes the conflicting information to a report file.
	`restoreDesign fullchip.enc.dat fullchip`
	`read_parallel_edit_files -files 1.eco 2.eco 3.eco`
	`exit`
	
	See Innovus User Guide product version 20.10, March 2020, pages 1585 and 1592.
	
	For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from that circuit design that is created by implementing the revised integrated circuit design as an output.

CLAIM CHARTS
U.S. Patent No. 7,231,626

2. The method of claim 1 further comprising a step of calculating a net delay only for each net in the integrated circuit design that is enclosed by the window.	The Accused Products are made, produced, or processed from a circuit design that is created by the method of claim 1 further comprising a step of calculating a net delay only for each net in the integrated circuit design that is enclosed by the window.  *Figure 1: Enabling in-design in the Innovus environment* https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/quantus-extraction-ds.pdf, page 2.

Post-Route Timing Optimization and Timing Signoff after an ECO both require calculation of net delays for the nets in the IC design enclosed by the incremental window.

Better design convergence via integration with Innovus and Virtuoso platforms

As an integral part of the silicon analysis function inside the Virtuoso custom IC design platform, the Quantus solution provides critical parasitic information for optimizing chip performance and yield.

Essentially, the extraction tool brings the physics of inter-connect parasitics into the Virtuoso environment for designing, characterizing, and optimizing chip layouts. Through the tool's integration with the Innovus environment, you benefit from a seamless solution for timing, IR, EM, signal integrity analysis, and power verification. The integration of the two tools equips you to reduce design turnaround time by performing incremental extraction, use integrated virtual metal fill for faster convergence, and to reach timing closure faster by using signoff-accurate extraction data for timing and noise optimization.

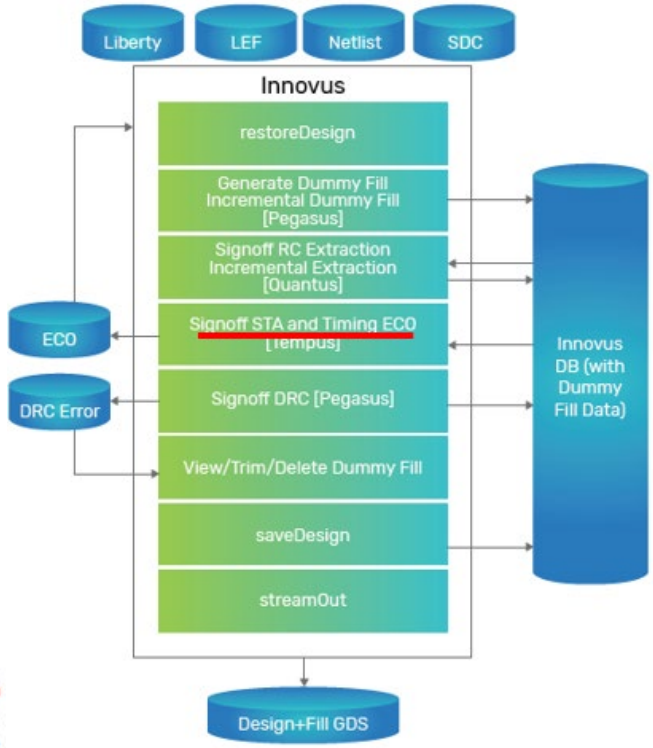


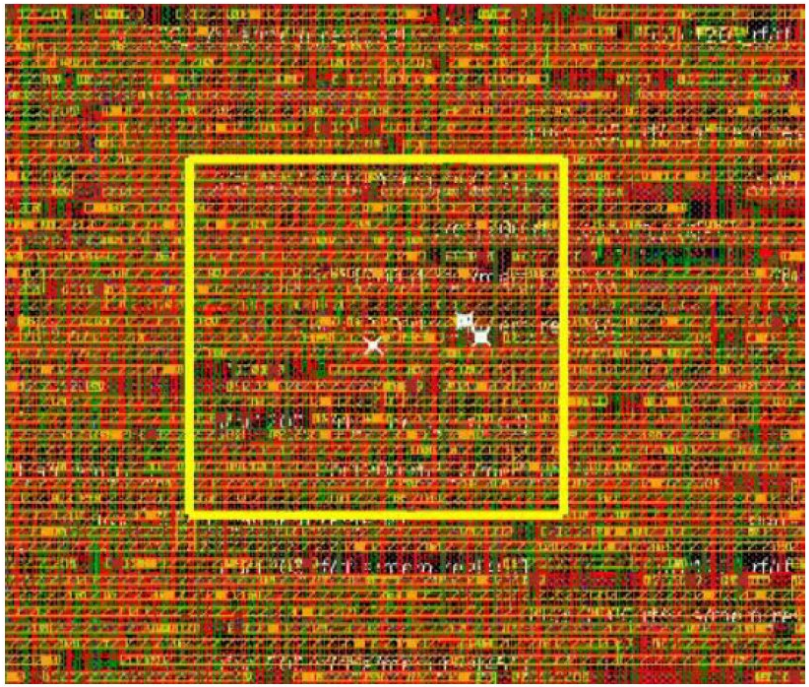
Figure 6: Hierarchical database flow

https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf, pages 2, 3, 4

For example, Lattice creates a circuit design for the LCMX02-7000HC, which was further made, produced, or processed from that circuit design for which a net delay was calculated only for the nets enclosed by the window, as indicated by Cadence's signoff of Timing ECO step.

3. The method of claim 1 further comprising a step of performing a design rule check only for each net in the integrated circuit design that is enclosed by the window.	The Accused Products are made, produced, or processed from a circuit design that is created by the method of claim 1 further comprising a step of performing a design rule check only for each net in the integrated circuit design that is enclosed by the window. **Parallel Editing Example for DRC Corrections** By using the parallel editing capability, you can divide the entire chip into different areas to enable multiple engineers to correct DRC violations in different areas of the design at the same time. After all the changes are done, you can apply the correction results to the entire chip. The following example shows how DRC corrections are done in a specific area of a real chip in parallel editing mode: **Step 1** Load the entire chip into Innovus and use `start_parallel_edit -region {x1 y1 x2 y2}` to specify the area in which DRC correction is required. **Step 2** After the DRC violations in the specified area are completely fixed, you need to save the changes made to the design. `end_parallel_edit -out_file drc_diff` will save all the changes to the **Step 3** Reload the original chip, and use `read_parallel_edit_files -files drc_diff` to read in the corrections from the previous step. The DRC corrections will be applied to the original chip layout so that DRC violations will be removed from the original area as shown below.

The specified area is highlighted in the GUI at this point. The `verify_drc` command can report all DRC violations in the highlighted area as shown below:



```
*** Starting Verify DRC (MEM: 998.2) ***

 VERIFY DRC ..... Starting Verification
 VERIFY DRC ..... Initializing
 VERIFY DRC ..... Deleting Existing Violations
 VERIFY DRC ..... Creating Sub-Areas
 VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {50.043 3.872 51.772 5.645} 1 of 1
 VERIFY DRC ..... Sub-Area : 1 complete 5 Viols.

 Verification Complete : 5 Viols.
```

As shown above, there are 5 DRC violations in the defined area. At this point, you can fix the DRC violations manually or through some automated method in the tool. After DRC fixing is complete, use the `verify_drc` command again to check whether or not the DRC violations are completely fixed.

```
*** Starting Verify DRC (MEM: 1054.7) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {50.043 3.872 51.772 5.645} 1 of 1
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

  Verification Complete : 0 Viols.
```

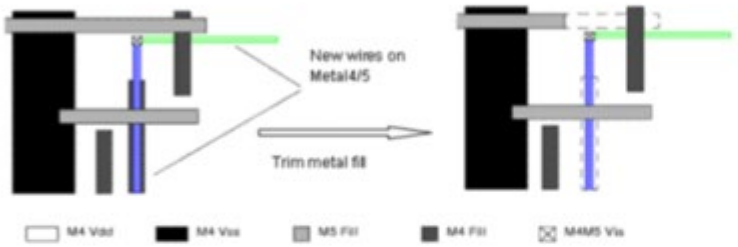
See Innovus User Guide product version 20.10, March 2020, pages 1585-88.

Trimming Metal Fill

The automatic routers, including the NanoRoute® router, ignore metal fill (`FILLWIRE` and `FILLWIREOPC`) shapes and might create routes that cause shorts or DRC violations.

The following case illustrates the DRC violation after NanoRoute ECO. You can use `trimMetalFill` to clean the violations according to user setting, LEF setting, and default parameters.

```
trimMetalFill -deleteViol
```



This command deletes metal fill shapes that cause DRC violations or shorts. After running the `trimMetalFill` command, the remaining shapes are still rectangles.

This means you need not delete the metal fill before ECO and then add it again after ECO. Instead, you can trim metal fill in the window that has been impacted by ECO. `trimMetalFill` can minimize the impact caused by the ECO on the timing of other paths (due to cross-coupling changes) that were not involved in the ECO.

To remove the shorts and violations, complete the following steps:

- To remove floating metal fill that causes shorts or violations, run the following command:

  ```
  trimMetalFill [-deleteViol] [-ignoreSpecialNet]
  ```

  This command repairs violations caused by the metal fill shapes. If the metal density drops below the target after trimming the metal fill, re-run the `addMetalFill` command.

  The `trimMetalFill` command trims metal and via fill shapes based on the following spacing rules:

- Between `FILLWIRE` and `FILLWIREOPC` shapes, the active spacing value or minimum spacing based on DRC rules, whichever is larger, is required.

See Innovus User Guide product version 20.10, March 2020, pages 722-23.

When the initial signoff metal fill generation, RC extraction, timing analysis, and ECO are performed, some wiring patterns disappear, while some new patterns are generated. The newly added wiring pattern will cause a DRC violation between the initial metal fill and may be required to be removed. So, it is also essential to add metal fill to the empty spaces of the disappearing patterns of wires.

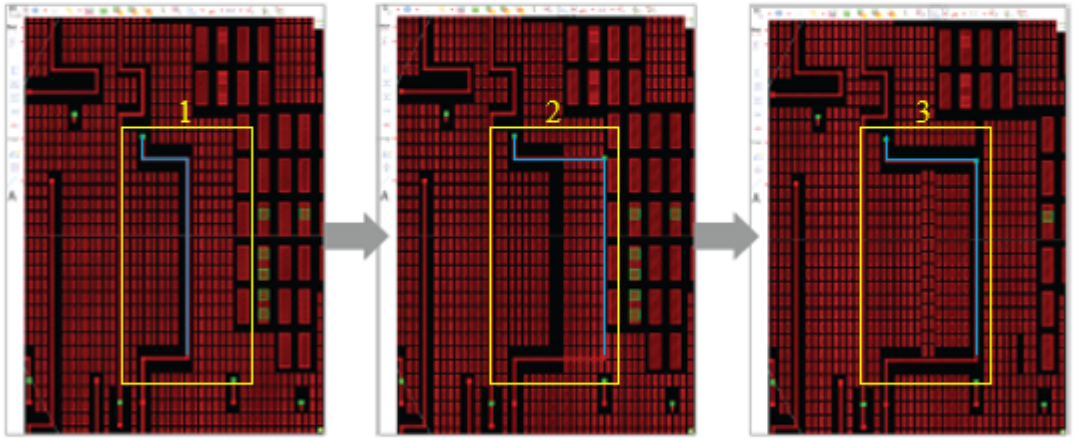


Figure 8: Pegasus incremental metal fill generation

https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf, pages 4 and 5

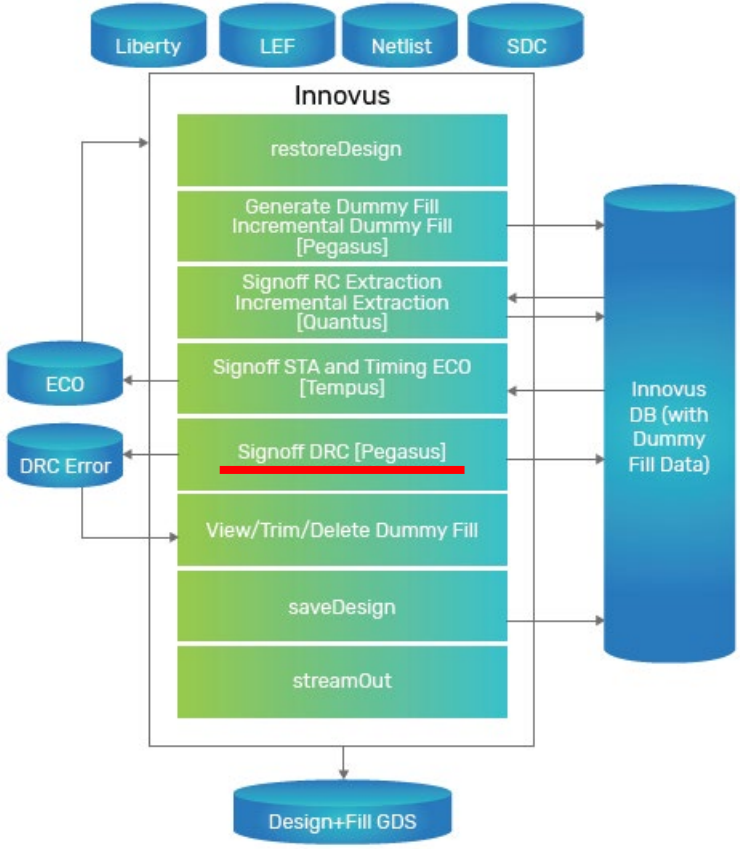
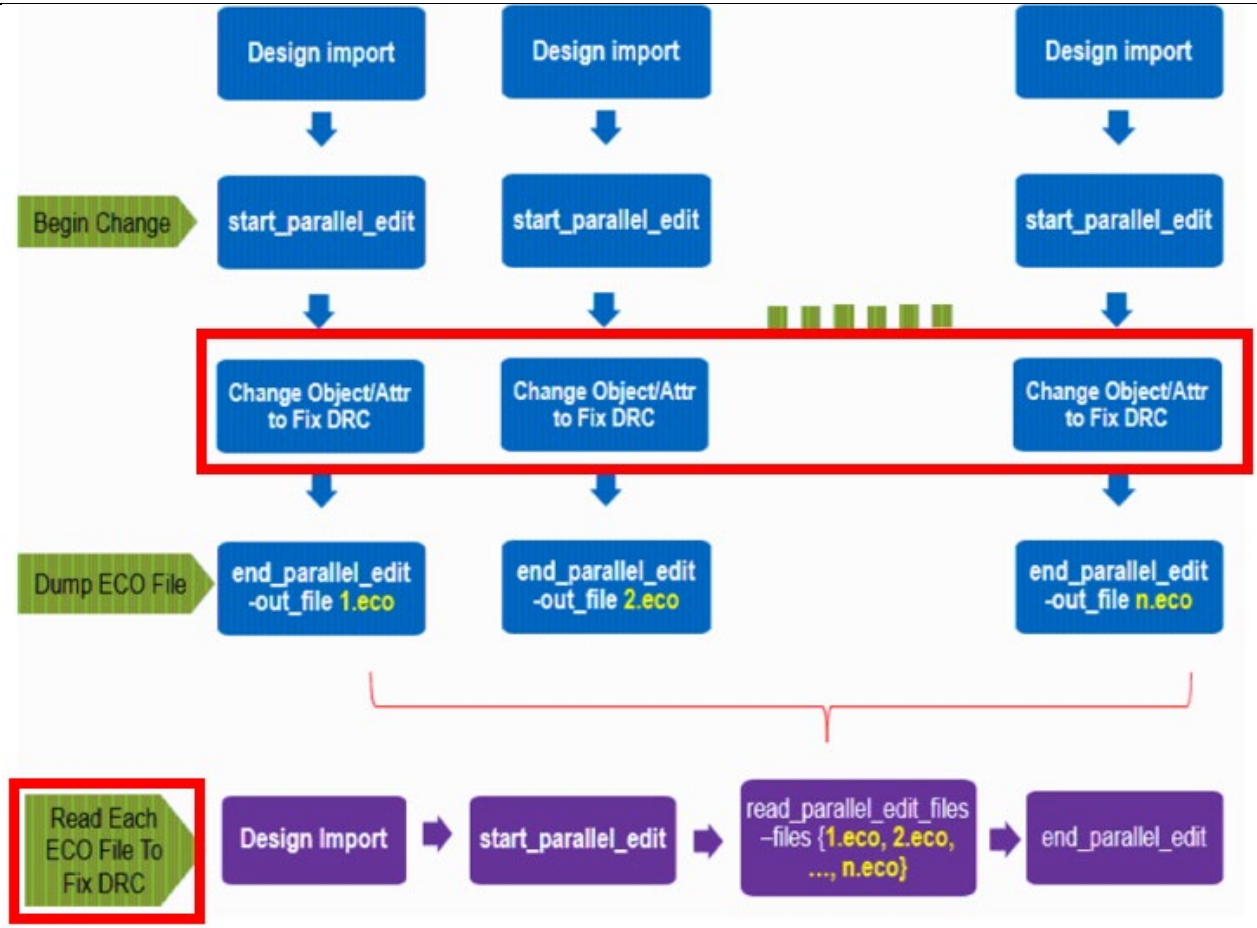


Figure 6: Hierarchical database flow

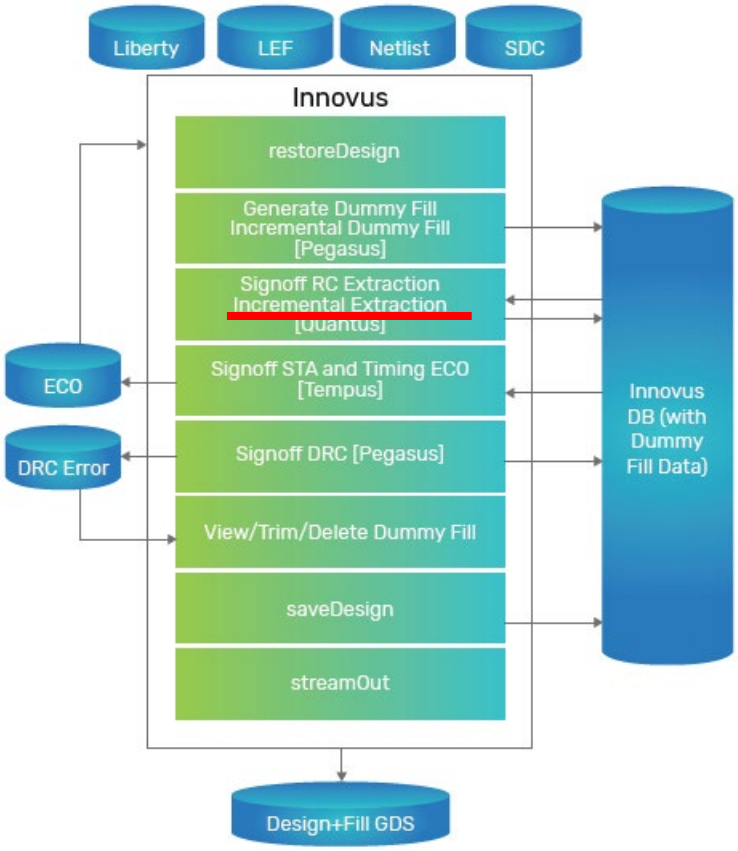
https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf, page 4



See Innovus User Guide product version 20.10, March 2020, pages 1583 and 1590.

For example, Lattice creates a circuit design for the LCMX02-7000HC, which was further made, produced, or processed from that circuit design that was further created by performing a design rule check separately for each net in the integrated circuit design that is enclosed by the window.

CLAIM CHARTS
U.S. Patent No. 7,231,626

4. The method of claim 1 further comprising a step of performing a parasitic extraction only for each net in the integrated circuit design that is enclosed by the window.	The Accused Products are made, produced, or processed from a circuit design that is created by the method of claim 1 further comprising a step of performing a parasitic extraction only for each net in the integrated circuit design that is enclosed by the window.  *Figure 6: Hierarchical database flow* *https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf, page 4*

Quantus Extraction Solution

Next-generation tool with the fastest performance and scalability, best- in-class accuracy using smart solvers, and in-design and signoff parasitic extraction that customers trust

Key Benefits

- Best-in-class accuracy for FinFET designs versus foundry golden
- 5G-ready to support all design types
- Tighter accuracy against field solver, with a near-zero mean
- Highly accurate critical net extraction with integrated field solver, Quantus FS
- High performance and scalability with massively parallel architecture, supporting a linear gain when the number of CPUs used is doubled
- Scalability for single- and multi-corner extraction runs, with up to 3X faster performance in multi-corner runs
- Accurate and fastest runtimes for functional ECOs via automated incremental extraction

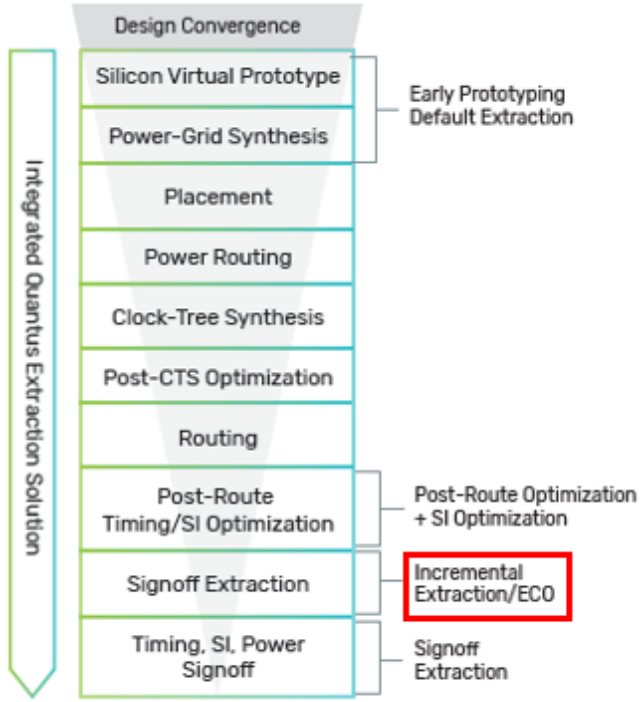


Figure 1: Enabling in-design in the Innovus environment

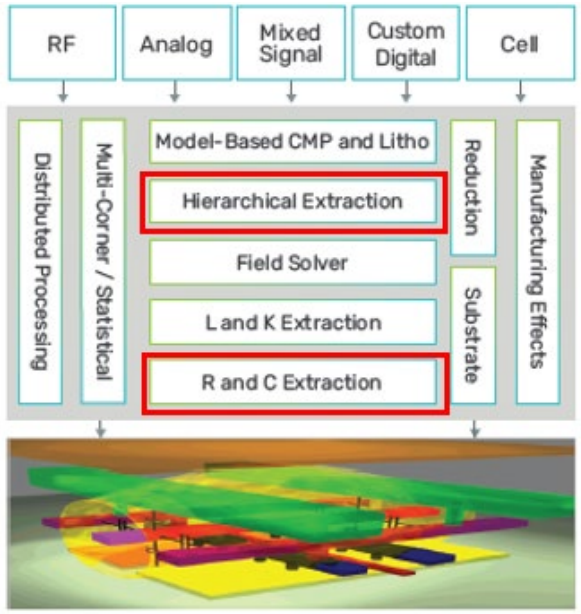


Figure 2: Key functionalities of Quantus Extraction Solution

	Better design convergence via integration with Innovus and Virtuoso platforms As an integral part of the silicon analysis function inside the Virtuoso custom IC design platform, the Quantus solution provides critical parasitic information for optimizing chip performance and yield. Essentially, the extraction tool brings the physics of inter-connect parasitics into the Virtuoso environment for designing, characterizing, and optimizing chip layouts. Through the tool's integration with the Innovus environment, you benefit from a seamless solution for timing, IR, EM, signal integrity analysis, and power verification. The integration of the two tools equips you to reduce design turnaround time by performing incremental extraction, use integrated virtual metal fill for faster convergence, and to reach timing closure faster by using signoff-accurate extraction data for timing and noise optimization. *https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/quantus-extraction-ds.pdf*, pages 1-3 For example, Lattice creates a circuit design for the LCMX02-7000HC, which was further made, produced, or processed from that circuit design that was created by performing a parasitic extraction for each net in the integrated circuit design that is enclosed by the window, as indicated by Cadence's incremental parasitic extraction functionality.

Caveat: The notes and/or cited excerpts utilized herein are set forth for illustrative purposes only and are not meant to be limiting in any manner. For example, the notes and/or cited excerpts, may or may not be supplemented or substituted with different excerpt(s) of the relevant reference(s), as appropriate. Further, to the extent any error(s) and/or omission(s) exist herein, all rights are reserved to correct the same.

EXHIBIT C

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF OREGON

BELL SEMICONDUCTOR, LLC Plaintiff, v. LATTICE SEMICONDUCTOR CORPORATION Defendant.	**Case No.** **JURY TRIAL DEMANDED**

DECLARATION OF LLOYD F. LINDER

1. I make this declaration on behalf of Bell Semiconductor, LLC ("Bell Semic"). I understand that Bell Semic will offer my declaration as evidence in support of the Complaint in the above-captioned action.

2. My qualifications to testify concerning the relevant technology are set forth in my curriculum vitae, which is attached hereto as **Exhibit 1**.

3. I received my Bachelor of Science degree in Electrical Engineering (BSEE) from UCLA in 1985. I received my Master of Science degree in Electrical Engineering (MSEE), also from UCLA, in 1987. Thereafter, I continued studying Electrical Engineering at USC, where I received an Engineer's Degree in 1989 and researched and completed my thesis towards a doctoral degree in 2002. Following the completion of my BSEE, I began work at Hughes Aircraft, where I worked for 12 years.

4. When Hughes Aircraft was acquired by Raytheon in 1997, my title was "Senior Scientist." At Hughes Aircraft, I was the technical lead for RF/analog/mixed signal IC

development and was a subject matter expert (SME) in integrated circuits, serving as a company-wide resource for review of integrated circuit designs and technical support of new business.

5. My next position was as an Engineering Fellow at Raytheon from 1997–2002, where I again was the technical lead for RF/analog/mixed signal IC development and was a subject matter expert (SME) in integrated circuits, serving as a company-wide resource for review of integrated circuit designs and technical support of new business.

6. In February 2002, I began a role as Director of Technology at TelASIC Communications, a company that I also founded. In this role, I served as the technical lead for the development of state-of-the-art ADC (analog-to-digital converter) and DAC (digital-to-analog converter) commercial products for the cellular base station market.

7. In 2006, I began working under "Lloyd Linder Consulting" as an Independent Integrated Circuit Design, Systems, Intellectual Property, and Wireless Consultant, a role that continues to this day. In this role, I have served as a consultant to over 100 companies in the commercial and military contractor semiconductor component market space and have served as an expert witness in semiconductor cases.

8. From 2008–2009, overlapping with my consulting, I took a position at Menara Networks for approximately 10 months, where I was involved with the development of an electronic dispersion compensation (EDC) IC and the development of quad transceiver for next-generation 10 Gb/s ASICs with integrated FEC / EFEC in CMOS.

9. I have received various honors over the course of my education and career. In 1985, I was named UCLA's most outstanding senior electrical engineering student, graduating Phi Beta Kappa and Summa Cum Laude. I am an IEEE Senior Member and served as a Judge for the San Fernando Valley Section Entrepreneurial Business Plan Competition in 2008. I am a named inventor on over 100 issued United States Patents (with several currently pending) and over 300

international patents, and have published over a dozen journal and conference papers focusing on semiconductor design and layout. I am a two-time Hughes Aircraft Division Patent Award Winner, and was named by Hughes as a Masters Fellow, Engineers Fellow, and Doctoral Fellow.

10. I have reviewed U.S. Patent No. 7,260,803 to Lakshmanan et al. ("Lakshmanan '803"), and its file history. I have also reviewed U.S. Patent No. 7,231,626 to Hoff et al. ("Hoff '626"), which is asserted in the Complaint, and its file history. In addition, I have reviewed the claim charts accompanying the Complaint supported by this Declaration.

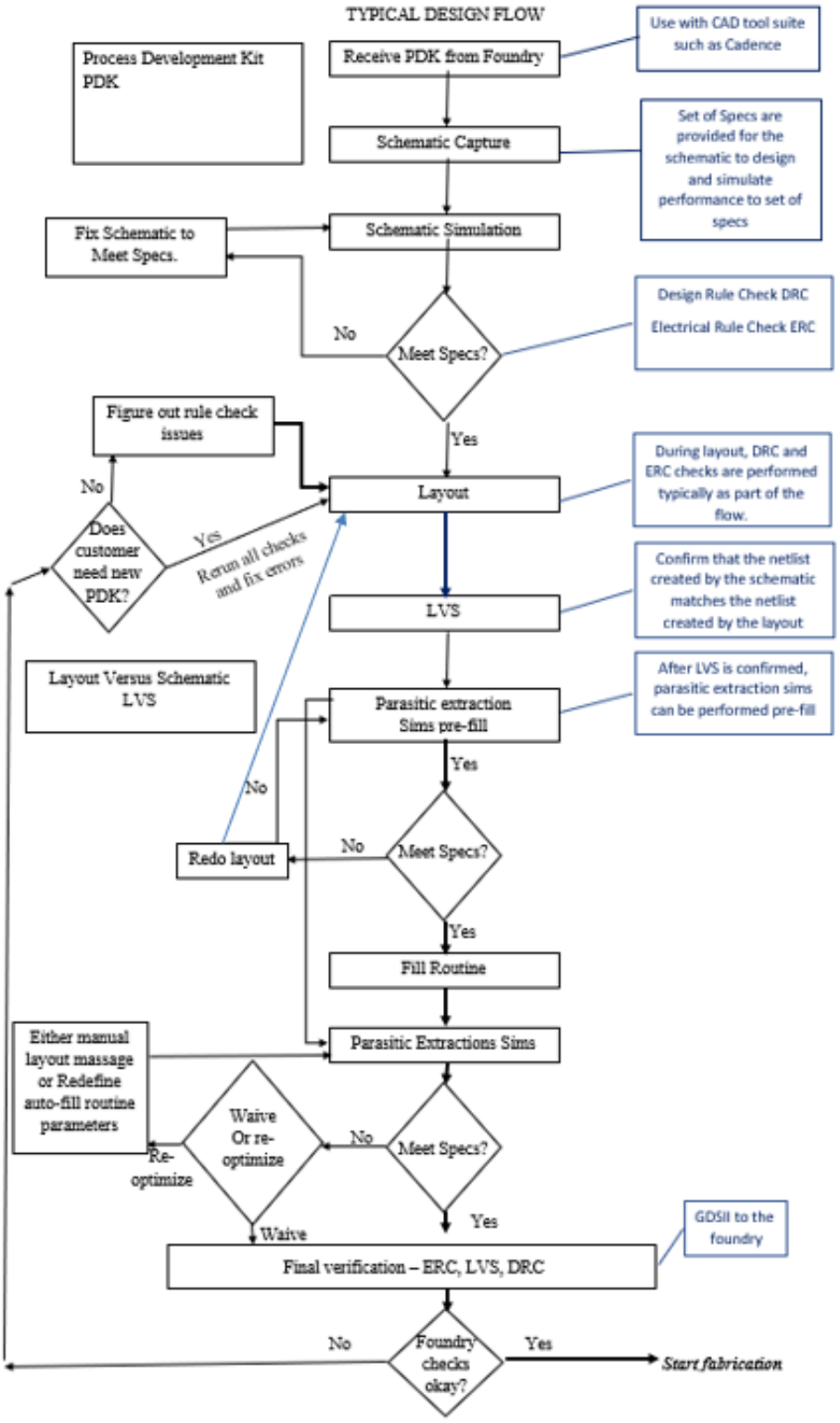
11. My college education over 15 years and 35 years of knowledge and experience in integrated circuit design, layout, and fabrication provides the necessary experience to support my stated conclusions set forth below.

Background on Integrated Circuit Manufacture, and Specifically the Layout Process Flow Segment of the Manufacturing Process and Subsequent Changes to the Physical Design

12. Semiconductor manufacture begins with the creation of a set of specialized electronic files that dictate the three-dimensional structure and features of the semiconductor device. These files, which are normally referred to as Graphic Design System (GDSII) files, are specifically formatted for and serve as necessary inputs for the devices that build the semiconductor device layer-by-layer according to the instructions contained in the GDSII files. Any changes to the structures in the GDSII files will result in changes to the structures in the fully fabricated device.[1] The manufacturing process ends with the wafer containing the individual semiconductor devices being fully fabricated and sawed into individual semiconductor dies.

[1] The physical design validation of an integrated circuit design ensures that all spatial constraints are satisfied for the traces and devices formed in various layers of an integrated circuit die. The structures formed in the several layers of an integrated circuit die are represented in a GDSII format file that contains the chip topological information for creating the masks used in manufacturing the integrated circuit dies. This is also called the "layout," and which patents in this area typically call a "design". The GDSII format is an industry standard used by commercially available physical verification tools to represent physical design data. All structures affecting the performance of the circuit die must and will be present in the layout.

13. I have created the image below, which provides a simplified schematic showing, at a high level, a commonly-used integrated circuit design flow process that is representative of many (if not most) process flows in current use for creation of circuit layouts:



14. The integrated circuit design flow process includes a design engineer, using design tools, to create a design for an integrated circuit to be processed.

15. Design tools from vendors such as Cadence, Synopsys, or MentorGraphics (now Siemens) will then be used to design, simulate, and lay out integrated circuits. The typical design tool suite includes[2] schematic capture, simulation, layout, verification (layout versus schematic (LVS) and design rule check (DRC)), and fill generation routines. These fill routines can be automated or manual, and can be provided by the design tool company in whole or in part.

16. To be sure, the precise capabilities of each design tool available to a particular design engineer may differ within a company (based on what options in the design suite are available to a particular user or on a particular device), and between different design tool suites. However, based on my experience, at a high level, the design tools used by design engineers in the semiconductor industry, all operate in substantially similar fashion for schematic capture, simulation, layout, verification, design rule check, and fill-generation. In particular, based on my experience as a consultant, the design tools commonly used in the industry to place dummy fill operate in substantially similar fashion in providing incremental and timing-aware fill generation for integrated circuit layouts. This also applies to the design tools commonly used to identify texted metal shorts, which likewise operate in substantially similar fashion.

17. In the design process, the schematic is created first. The layout design tool is used to place and route all of the active (i.e., transistors) and passive components (i.e., resistors, capacitors, and inductors), and the interconnections between devices (represented as wires) in the schematic. It represents the circuit function that is to be physically implemented in the silicon. The schematic is created and simulated, using the CAD tools, to confirm that the circuit functions to a desired specification.

[2] Sometimes electrical rule check (ERC) is also included in design tool suite capabilities.

18. Once that performance specification is confirmed from the schematic simulation, the layout of the circuit is performed to physically place each of the individual elements necessary to implement the circuit functions set forth in the schematic in the GDSII file. During layout, layout rules for active and passive devices must be followed, but conformance is not checked until a DRC is run (typically at least as part of the final verification, though it can be run at any point or points in the layout process). Instead of only checking conformance at the end, it is possible to use a subset of the DRC deck to check for texted metal shorts in the layout of the schematic at an early or incremental point in the process flow. This allows the top-level routing to be completed in parallel with the block-level schematic and layout. Doing this will help accelerate the design timeline and avoid any delays occasioned by only finding such rule violations at the end of the design process flow for that particular schematic.

19. Once the layout is completed, it is compared to the schematic of the circuit using layout-versus-schematic (LVS) tool to confirm that the two are identical. From the schematic, a netlist (a list of devices and the associated nodes) is generated. From the netlist, the schematic could be re-generated by hand by drawing the devices and connecting the device nodes. From the layout of devices and associated nodes, a corresponding netlist is generated, from which a similar schematic could be generated by hand by drawing the devices and connecting the device nodes from the layout netlist. Then the schematic netlist is compared to the layout netlist using the LVS tool. The LVS tool compares the schematic netlist to the layout netlist to see if they match—i.e., whether they contain the same devices connected in the same fashion. If they do not match, the discrepancies between the two must be found and corrected, and LVS re-run. Any violations of layout rules must be corrected and DRC re-run for the layout.

20. After passing LVS, the process of performing parasitic extraction simulations before the fill has been placed (pre-fill) can be performed on an extracted netlist created from the

layout. If parasitic simulations are performed prior to the fill placement, the designer can get an idea of the impact on circuit performance from the basic layout parasitics pre-fill. From the layout, a netlist is extracted that includes any of parasitic resistance (R), parasitic inductance (L), parasitic capacitance (C), or any combination of the three. Additionally, the parasitic extraction can include what is termed "coupled" capacitance (parasitic capacitance between metal lines) as well as the parasitic capacitance to the substrate. The extracted netlist, with the selected added parasitics, can be used to run simulations on the baseline layout to determine if there is any performance degradation due to the baseline layout routing.

21. The simulated performance of the layout, which includes the parasitics, needs to be as close as possible to the specification that was already satisfied by the schematic. That is why parasitic extraction is performed, and why it is iterated pre-fill and post-fill. So if there is performance degradation due to the baseline layout, the layout is redone until its performance is at acceptable parameters. Ideally, the extracted simulation results match the schematic simulation results, which means that the layout parasitics had no impact on the circuit performance.

22. Once the layout passes pre-fill, the design tool is used to insert dummy fill at appropriate locations in the layout that do not contain devices or other features. As is well-known in the industry, the purpose of adding dummy fill is to achieve a higher and more uniform density of interconnect across the surface of each layer of the chip, to improve the outcomes of the chemical-mechanical polishing/planarization (CMP) step during fabrication. If individual pieces of fill are below a certain minimum size, they may not planarize properly during CMP, which will result in the dielectric material deposited on top of those too-small features not planarizing properly,[3] which will produce in dishing in the dielectric and result in a non-planarized surface.

[3] The effect on the dielectric from underlying interconnect is known as the deposition bias. A "positive bias" or "positive deposition" bias is when the width of the protrusion in the dielectric is

Thus, in practice, the fill pieces added cannot be below a certain minimum feature size. Adding dummy fill at or exceeding the minimum feature size and to achieve a higher and more uniform density of interconnect lowers the likelihood of defects caused by the CMP process step and thus improves the yield of modern integrated circuits.

23. Once all components of the integrated circuit design have been placed and routed, a physical design validation is typically performed at the very end of the design cycle. This ensures that all spatial constraints are satisfied for the traces and devices in each layer of an IC, that the die complies to all process rules, and that any additional required steps specific to manufacturability for a selected technology have been performed (e.g., metal utilization).

24. Even after a physical design validation, the physical design may change for any one of a number of reasons, including but not limited to timing delays, performance, or functionality. In such instances, the various steps in the process flow will have to be redone to accommodate the changes in the physical design. This includes placement of dummy fill as well.

25. As the pre-fill step confirms that parasitics of the baseline layout, pre-fill, do not degrade the performance of the integrated circuit, it is desirable that the fill likewise does not degrade performance. However, depending on its placement, dummy fill can also degrade the performance of the integrated circuit, which is undesirable. To minimize this, the design suites include timing-aware fill tools that minimize, if not prevent, any degradation to circuit performance caused by dummy fill insertion. These tools also incorporate details on fill density,

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greater than that of the underlying active interconnect feature. Conversely, a "negative bias" or "negative deposition bias" is when the width of the protrusion in the dielectric is less than that of the underlying active interconnect feature. In either case, large density variations of the active interconnect features will typically result in interconnect that is insufficiently planarized during CMP, and thus, overpolishing of the dielectric that produces significant dishing. This is particularly detrimental in fabrication of multi-layer chips and packages.

size, and position necessary to meet the requirements of the fabrication process and allow the user to specify the minimum and maximum dimensions of the dummy fill.

26. Based on my experience, use of such timing-aware fill tools has become standard practice in designing modern integrated circuits. In fact, modern integrated circuit designs are required to have fill included as part of the database submitted for fabrication. Due to the complicated nature of these designs, such as SoCs and highly integrated circuits with many layers, the fill process cannot be manual at least for the practical reason of there being far too many locations and options for fill position and dimension to designate by hand for fill insertion. Moreover, the chip has many critical nets (i.e., important timing-sensitive signal lines), so there is a need for the fill-placement to be aware of any impact on the timing and resulting performance impact of the circuit. Timing-aware fill tools are used to attempt to simultaneously meet interconnect density (including feature size) and timing closure requirements, but they are not guaranteed to do so 100% of the time. When this occurs, a decision must be made to compromise performance at the expense of yield, or vice-versa.

27. Once the fill routine is completed, the fill checks are done, and final verification is performed again (LVS, DRC). The fill checks are performed based on percentage requirement on a specified area in the layout.

28. Once the layout database has been verified, it is sent for fabrication in the form of a GDSII database, which is the industry standard format for delivery of the chip database. As previously mentioned, fill is required to be included as part of the GDSII database.

29. The design resource is provided with a process design kit (PDK), which includes all of the information necessary to capture a schematic, run a simulation, do a layout, and perform all of the checks on the layout to make sure that the final GDSII is in an acceptable form to be ready for fabrication. It is the design resource / customer's responsibility to make sure that the

designed chip meets all of the expected requirements for fabrication and bears the risk of failing to follow any steps in the design flow. For example, if the circuit does not work, that is the customer's responsibility. If the layout does not match the schematic, that is the customer's responsibility. The GDSII does have to meet all of the DRCs in order to be fabricated.

30. In order to develop an integrated chip product, tools are needed to develop the schematic, the layout, verification of the layout, and the final GDSII database for fabrication. Many companies use different tools (from different vendors) to accomplish this process either typically due to cost or preference of internal proprietary tools. Regardless of the process and specific tools that are used, the GDSII database goes through an internal DRC after it is received and before fabrication of the integrated chip:

a. The design resource receives a PDK that contains all of the information is included to create a GDS database to release for fabrication. This includes circuit symbols for the creation of the schematic, models for the circuit symbols to run simulation, and associated layout devices that have been created with all of the process layers needed.

b. Additionally, there are what are known as "rule decks" in the PDK that allow for LVS and DRC. A rule deck is typically a file that specifies all of the available rules (for example, minimum feature sizes such as line width and minimum fill dimensions), the layers to process on each rule, and the parameters of each rule. The LVS deck compares the schematic to the layout, and the DRC deck covers all of the design rules for placing and routing devices. For LVS, a netlist of the layout is created. This netlist is compared to a netlist created for the schematic. The LVS tool compares the two to determine if they match or not.

c. Additionally, there is a parasitic extraction deck that extracts all of the parasitics of the layout that is used to run simulations to close timing or to confirm that the layout still meets all of the chip requirements.

d. There can also be an electrical rule check (ERC) deck as well, depending on the fabrication involved.

31. If the DRC rules at pre-fabrication do not match those at the design resource, it is possible that there will be DRC errors. This could be due to a number of reasons, including the DRC in the provided process design kit (PDK) is not up to date, and so the PDK will be updated with the updated DRC and the design resource will have to redo everything and fix the DRC errors, providing a new GDSII database before fabrication can begin. These DRC checks at pre-fabrication will include checks for the fill on all layers to confirm that the fill requirement is met, on a granular level, for all tiles at the chip boundary level.

Even Minor Design Changes Can Lead to Substantial Delays

32. Traditionally, each step in the design process flow was performed on a layer-by-layer basis, including but not limited to routing, parasitic extraction, calculation of delays, DRC, and placement of dummy fill. Any change would result in needing to redo the process steps for the design as a whole, as these changes usually came at the end of the process flow after all the layout and rule-checking steps were performed. Thus, it made sense to do any and all changes after all the layout steps have been performed.

33. However, it is rarely (if ever) that any modern IC proceeds through the design process flow without changes to the physical design along the way, especially as designs have become more complex. This can occur, for example, when interconnect density is not met, when a connection error is discovered, when timing characteristics are not met, or for one or more of

any number of other reasons. These changes can occur at various points throughout the design process.

34. The problem with such revisions to the physical design during or after the layout process flow is not just that the particular step in the process flow will need to be redone, but also that all subsequent steps (which depend on the prior step) will also need to be redone, even if the change was extremely minor and only affected a small segment of the device and/or relatively few nets. For example, any revisions to routing after dummy fill has been placed will require at least revisions to the dummy fill locations.

35. And, as mentioned above, each such step and all subsequent steps would traditionally need to be done on a layer-by-layer basis. Thus, the amount of time it would take to implement changes to the physical design of the chip would not scale with the size of the change itself (which could be relatively minor), but rather with the complexity and size of the IC as a whole. This started to become especially burdensome by the early 2000s as cutting-edge devices grew to encompass numerous layers and the number of nets and complexity grew exponentially.

36. For example, the typical turnaround time for a design change implementing a functional or timing ECO was, with traditional design tools and process flow, typically on the order of one week regardless of the size of the design change. (Hoff '626 at 2:37–40.) That is because even a design change of just a few cells would still need to be merged into the overall design of substantially greater size, with the routing, DRC verification, net delay, and parasitic extraction, among others, scaling with the overall size of the IC. (*Id.* at 2:40–49.)

37. Likewise, re-running the dummy fill tool after a layout change would, given the chip designs, tools, and computers available in the early 2000s, typically take on the order of 30 hours for cutting-edge designs. (Lakshmanan '803 at 1:47–50.) This would be the case even if

the layout change were relatively insignificant, to ensure that the dummy fill would still satisfy the fabrication and timing requirements as much as possible.

38. To make matters worse, each time an ECO is received, the process flow will need to be repeated. This sort of iterative process could and did significantly impact the design schedule and typically resulted in substantial cost overruns.

39. Prior to Hoff '626, every revision to the physical design or an implementation of another ECO during the design process typically required turnaround time on the order of approximately one week regardless of the extent of the revision. (Hoff '626 at 2:36–44.) That is because even small revisions needed to be merged with the overall design and all the parameters (including cell placement, routing, DRC and physical validation, parasitic extraction, timing closure, and dummy fill) rechecked for every net in the design. (*Id.* at 2:44–52.) This prior art process flow is depicted in Figure 1 of Hoff '626:

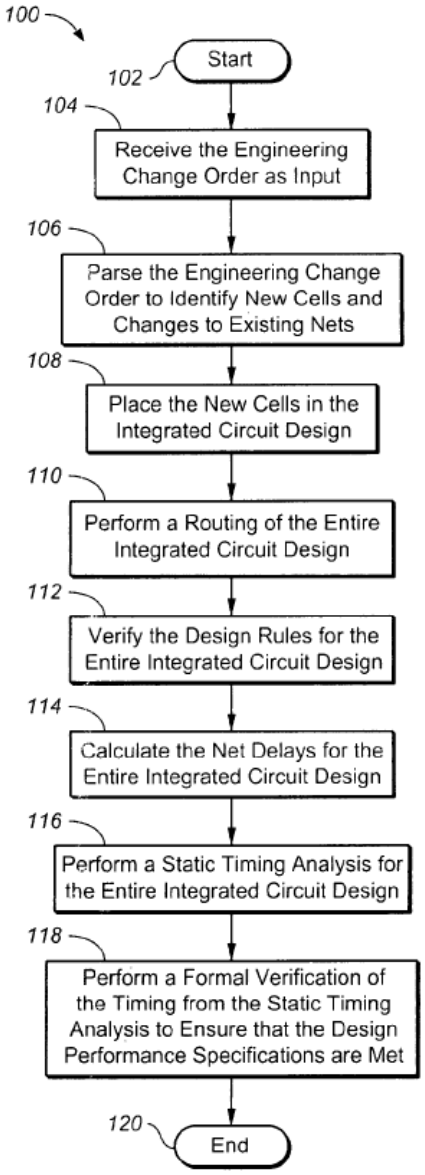


FIG. 1

Explanation of Hoff '626

40. In place of having to deal with redoing all of the subsequent process steps for the entire layer (or design as a whole) at a time whenever a change to the physical design is implemented, Hoff '626 teaches a technique that permits changes to the physical design that proceed incrementally, rather than for the layer or design as a whole. (1:25–2:3.) Specifically, Hoff '626 teaches that by enclosing the physical design change in a window that is a subset of the IC design, that change can be implemented incrementally by performing routing only for the nets

enclosed by the window encompassing the physical design change. (*Id.* & Fig. 2.) Thereafter, that revised routing in that window replaces the original area in a copy of the IC design to generate a revised IC design. (*Id.* & Fig. 2)

41. Optionally, other steps in the design process flow can also be performed incrementally following the incremental routing, i.e., only for the nets encompassed by the window needed to implement the physical design change. Those can include calculation of net delay for each such net, DRC for each such net, and/or parasitic extraction for each such net. (*See, e.g.*, Fig. 2, 4:32–52.)

42. The significant efficiency gains from the ability to implement ECOs without having to rerun the routing tool for the entire design are repeatedly described within Hoff '626. (*E.g.*, 1:15–22, 2:37–53, 3:19–24, 4:26–32, 6:29–33.) This helps IC manufacturers "avoid[] repeating calculations for nets that are not changed or effected by the [ECO]." (*Id.* at 6:31–33.) These substantial time savings allow designers to meet aggressive design schedules. Based on my experience in semiconductor layout and design I agree that this new and improved incremental process flow results in substantial efficiency gains in the design process for modern semiconductor devices. These gains are so substantial, and these incremental methods of routing and subsequent layout steps are so widely used today that it is hard to quantify just how important the inventions claimed by Hoff '626 are to achieving current time-to-market for modern chip designs. It is also difficult to quantify how much the typical IC production schedule would be delayed for modern chip designs without the use of the methods claimed in Hoff '626.

43. Based on my experience in semiconductor layout and design, it was not well-understood, routine, or conventional at the time of Hoff '626 to perform routing and subsequent layout process steps in an incremental fashion following receipt of an ECO. In particular, it was not well-understood, routine, or conventional to create a window in the IC design, defining an area

less than the entire IC design, that enclosed a revision introduced by the ECO; nor was it well-understood, routine, or conventional to perform an incremental routing of the IC design only for each net enclosed by that window. Accordingly, it was also not well-understood, routine, or conventional to create a revised integrated circuit design by replacing the area bounded by the window in the original IC design with the results of the incremental routing. These features, central to Hoff '626, is required by every claim in the patent and recited explicitly in both independent claims. This is not only true in considering those elements by themselves, but also in an ordered combination with the other recited claim elements in creating a novel process flow that did not require a full-layer re-routing and subsequent process steps simply to account for the relatively few nets affected by an ECO.

44. This also applies to the dependent claims, which similarly recite performing subsequent process flow steps that would be affected by performing the ECO on an incremental basis (i.e., only for the nets enclosed by the window). Thus, the features recited by these dependent claims were also not well-understood, routine, or convention because the conventional design tools available at the time did not perform such process flow steps on an incremental basis.

45. Hoff '626 explains that "[i]n previous methods for implementing an [ECO] request . . . design tools are run for the entire integrated circuit design." (1:15–17.) As a result, "the typical turnaround time is typically about one week regardless of the size of the [ECO]." (2:38–41.) As I have explained, the typical process flows and all the routing and layout tools of which I was aware lacked the capability to accommodate ECOs without a full-layer re-run of the routing tool and subsequent calculations such as net delay and parasitic extraction. Nor am I aware of any "unconventional" tools or process flows dating to the time of Hoff '626 that had such capabilities.

46. During prosecution of the application that matured into Hoff '626, the applicant specifically amended the claims to clarify that the routing of the incremental circuit within the

window was an incremental routing, rather than for the circuit design as a whole. The applicant explained that incremental routing was not disclosed in the prior art cited by the examiner, and the examiner agreed with applicant's arguments in allowing the claims. I agree with the examiner and the applicant.

Dummy Fill is Required in Design and Layout of Multi-Layer Semiconductor Chips

47. To the best of my knowledge, adding dummy fill is a requirement for every integrated circuit using the latest technology nodes. Certain older nodes still in fabrication (>350nm) may not require fill, but I believe that even some of these older technology nodes have incorporated fill requirement to enhance yield.

48. As mentioned above, it is required that the GDS database include fill within the database submitted for fabrication. In particular, most fabrication processes used in modern semiconductor chip designs require both a minimum density and a minimum feature size for the interconnects (i.e., pieces of metal or semiconductor) placed on each layer of a multi-layer chip design. This is the case both for the layer as a whole and for individual subunits of each layer, and is fundamental to the creation of consistent fabrication of multi-layer devices with minimal defects.

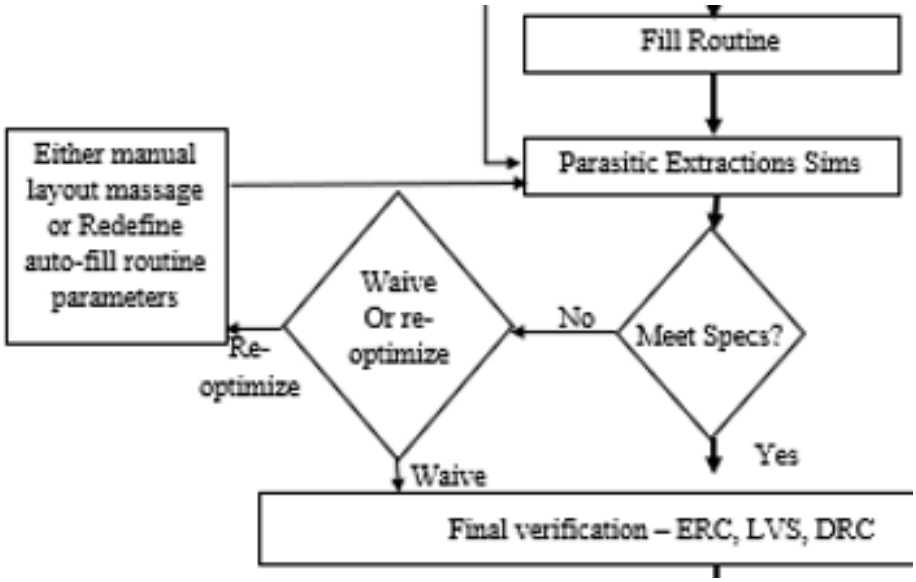
49. Fabrication processes typically partition each layer of the chip design into rectangular regions called tiles, each of which must also meet a minimum density requirement. For any given region of the chip, the interconnect density is the area of all of the interconnect in that region divided by the total area of that region.

50. Sufficient interconnect density and substantial uniformity of interconnect are required for the chemical mechanical polishing (CMP) portion of the chip fabrication process. CMP is crucial to achieve planarity, which allows for multi-layer chip designs and high yield of functional devices. Insufficient interconnect density and/or insufficient uniformity of interconnect

between various regions will increase the likelihood of defects during the chip manufacturing process, which will resultantly degrade the yield.

51. Once the functional features of the chip design (such as power lines, signal nets, vias, and the like) have been laid out as needed in the first instance, there will usually be substantial portions of the chip design that have insufficient interconnect density to permit CMP without incurring substantial likelihood of defects.

52. To increase the interconnect density of the layer as a whole, and of regions within each layer, numerous individual pieces of interconnect are inserted into available space in low-density regions of the chip until the minimum interconnect density specified for the particular fabrication process is achieved for each tile. Because these pieces of interconnect are not intended to carry signal or power, but instead are added to provide structural stability to the chip architecture, they are generally known as "dummy fill."



53. Placement of dummy fill is typically performed by a dummy fill software tool, and is one of the last steps in the chip design flow, with its extent and placement typically occurring after routing and timing closure. The time it takes the dummy fill tool to complete its task depends on the complexity of the circuit layout, and correspondingly, the size of the design database. If

dummy fill must be run (or re-run) for the entire layer, even small changes in layout can result in significant delays while the dummy fill tool runs each time the layout changes.

54. In operation, the dummy fill software tool typically partitions each layer of the design into rectangles called tiles, which it examines in each layer of the design. If the interconnect density in each tile does not meet (or exceed) the specified minimum interconnect density for the fabrication process, the dummy fill tool inserts dummy fill into free regions of that tile where no interconnect is present.

55. For large integrated circuits, commonly called system-on-a-chip (SoC) with either large analog content and small digital content ("big A, little D") or large digital content and small analog content ("big D, little A"), it is not practical to manually add dummy fill, so automated fill routines are almost always used. Because there are so many critical signals in a large SoC, the process cannot be done manually due to the time it would require. Thus, the design timelines and practical realities require that the automated fill routines are used instead.

56. However, placing the dummy fill that is too large in size, too extensive, and/or too close to signal nets increases capacitance between the signal wires and the dummy fill in the physical device if fabricated without taking additional measures. That increase in capacitance in the fabricated physical device would in turn slow the transmission speed of signals and degrades the overall performance of the integrated circuit. This effect is undesirable and is known as "parasitic capacitance."

57. The added parasitic capacitance will degrade parameters, such as operating frequency and rise/fall time, for a critical clock or signal, and this must be avoided in order for the circuitry to work properly.

58. The parasitic capacitance is inversely proportional to the distance between the dummy fill and the signal wire. Thus, parasitic capacitance from dummy fill will be minimized if the dummy fill is placed far from signal nets.

59. Conversely, the parasitic capacitance from dummy fill on signal lines is directly proportional to the lateral dimension of the dummy fill (i.e., the extent to which the dummy fill runs parallel to the signal line). Thus, parasitic capacitance from dummy fill will be minimized if the same area of dummy fill is placed in many narrow pieces oriented perpendicular to the signal line (which also places more of the dummy fill at a greater distance from the signal line) rather than one long strip oriented parallel to the signal line.

60. The result of using a constant (often very small) lateral fill dimension was that substantial dishing would occur during CMP due to variation in interconnect density in the lateral dimension, resulting in an unacceptably high rate of chip defects and unacceptably low yield. Since fixing fill dimension manually was a time-consuming process, with limited time available, the result would typically be that the interconnect density requirements could not be met, and a waiver would be requested before fabrication would begin, with any resulting yield degradation being accepted by the customer.

61. By minimizing the lateral dimension of dummy fill, its parasitic capacitance can be bounded below a particular value and its effect on circuit timing can be minimized. However, hard-coding a small dimension will create discontinuities in the dielectric that will only be exacerbated (rather than resolved) by CMP, thus limiting chip yield.

62. In other words, when using a one-size hard-coded dummy fill solution, the higher the required yield, the more constant the overall interconnect density must be within various portions of the layer, with increasingly higher parasitic capacitance and negative impact on timing and circuit performance because that interconnect will comprise dummy fill having a substantial

lateral dimension paralleling signal lines. Conversely, the more sensitive the timing requirements for the circuit, the less the parasitic capacitance can be tolerated near crucial signal nets and the lower the lateral dimension of the dummy fill can be for tiles that include such signal nets, resulting in a lower overall interconnect density, and greater variation across the layer, resulting in defects and lower yield. This tradeoff between performance and yield is further complicated when multiple metal layers are involved, which can be ten or even more.

63. The traditional solution to minimizing the parasitic capacitance effect of dummy fill near signal nets was the "simplistic approach" of hardcoding a large "stay-away" distance from crucial signal nets, essentially establishing a defined "exclusion zone" (or "keep-out area"), essentially a "moat" around those circuit elements that would be designated categorically unsuitable to receive dummy fill when the dummy fill software tool was utilized and the device fabricated. The distance was typically derived empirically for each design by studying the effect on timing from dummy fill inserted at various distances from clock nets in sample designs and was then manually hardcoded in the dummy fill libraries for each type of process technology.

64. The result of using these keep-out zones was that potentially the chip would have poor yield. Since this was a manual time-consuming process, with limited time available, the result would typically be that the fill requirements could possibly not be met, and a waiver would be requested before fabrication would begin, with any resulting yield degradation being accepted by the customer.

65. By excluding dummy fill from being placed within a certain distance of crucial signal nets, its parasitic capacitance can be bounded below a particular value and its effect on circuit timing can be minimized. However, hard-coding a large "stay-away" distance between dummy fill and signal nets, creating a region in which dummy fill cannot be placed, will also

reduce the space available for dummy fill insertion and thus limit the overall interconnect density that can be achieved.

66. In other words, the higher the required interconnect density, the closer it must be placed to signal nets, with increasingly higher parasitic capacitance and negative impact on timing and circuit performance. Conversely, the more sensitive the timing requirements for the circuit, the less the parasitic capacitance can be tolerated near crucial signal nets and the lower the interconnect density can be for tiles that include such signal nets. This tradeoff is further complicated when multiple metal layers are involved, which can be ten or even more.

67. It may be that the timing requirements cannot be met without a revision to the fill placement, density, and sizing, and re-extraction of the layout parasitics to determine if the timing requirements are met. If they are not, then a decision would have to be made to continue the iteration process or apply for a waiver and bear the risk of lower yield, or accept decreased performance.

68. Balancing these tradeoffs started to become particularly problematic by the early 2000s, as new processing technologies with smaller and smaller features demanded increasingly higher minimum interconnect density values at the same time that chip designs became much more aggressive in the circuit timing requirements. In such cases, it was often impossible to insert sufficient dummy fill into a tile such that the higher minimum density requirements could be met without also reducing the large "stay-away" distance, and thereby raising the timing impact of the dummy fill to levels that affected the performance of the chip. One potential solution was for the chip designer to waive the minimum interconnect density specified by a particular fabrication process. However, because invoking this waiver would not comply with the fabrication process requirements, the yield of the produced devices would not be guaranteed in such cases, which rendered this alternative not viable in practice.

69. Traditional dummy fill software tools of that time often completed their run through the tiles of each layer without reaching minimum interconnect density in some cases. In such cases, it would be necessary to re-run the dummy fill tool for those problematic tiles with a lowered "stay-away" distance and/or after adding, removing, or manually revising the size and positioning of portions of the fill. If, as frequently occurred, more than one such tile lacked sufficient interconnect density and required (at least) a second run of the dummy fill tool with the revised "stay-away" distance parameters and/or dummy fill size and positioning, multiple runs could be needed if, as was typical, the dummy fill tool could only handle one tile at a time.

70. This iterative process, with manual adjustments of the "stay-away" distance, dummy fill size, and dummy fill positioning often required multiple runs for each such affected tile; it was an involved, time-consuming process that can and did significantly impact design schedules.

71. Prior to Lakshmanan '803, every layout change or other ECO required re-running the dummy fill tool, at a cost of approximately 30 hours per ECO on cutting-edge circuit designs at that time. (Lakshmanan '803 at 1:47–50.) The only way to guarantee that dummy fill would not intersect any design objects throughout the circuit design would be to re-run the dummy fill tool after each and every change. However, removing all of the original dummy metal fill geometries, doing the ECO, and then inserting new dummy metal fill could lead to different timing characteristics in areas of the device that were not affected by the original ECO itself, which cause additional iterations in the ECO process. Manual examination and alteration and/or removal of dummy fill intersecting design objects would be so time-consuming as to be commercially impractical even if it would not affect timing closure and interconnect density requirements (which it would). Even leaving dummy fill for the last possible moment could not be sure to avoid any

subsequent ECOs, and there would also be no guarantee that sufficient interconnect density requirements and timing closure would be met on a single run of the dummy fill tool.

Explanation of Lakshmanan '803

72. Likewise, even when dummy fill could be placed in such a fashion that it would simultaneously satisfy interconnect density requirements for each tile and minimize any impact on critical nets, prior to Lakshmanan '803, any change to layout or ECO would practically require rerunning the dummy fill tool for the entire layer, at a substantial time cost. That is because an ECO typically results in design objects (such as wires) being added and/or their locations being changed. (Lakshmanan '803 at 1:51–59.) In other words, while the routing has changed as a result of implementing the ECO, dummy fill insertion is typically not part of the routing portion of the process flow, but rather a separate step that is only done after the routing and timing closure stages of the design flow. (*See* 1:33–36; 2:62–65.) And that step must be redone for the entire layer to ensure that no dummy metal intersects with any of the design objects. (1:55–59.)

73. In place of having to deal with dummy fill in a batch process for the entire layer at a time whenever the layout changed, Lakshmanan '803 teaches a technique that permits layout changes without requiring that the entire dummy fill process be redone. Specifically, Lakshmanan '803 teaches that, following an ECO, the dummy fill tool performs a check to determine whether any dummy metal objects (which were inserted prior to the ECO) intersect with any other objects (such as signal nets) in the design data. (3:21–24.) Any such intersecting dummy metal objects are then deleted from the design database, which obviates the need to rerun the dummy fill tool after the ECO. (*Id.* at 3:24–27, 3:44–46.)

74. Because most ECO make only small incremental changes, most of the dummy fill is likely to be unaffected by the ECO. (*See* 1:55–57.) Accordingly, it is highly likely that even after deleting any dummy fill that intersects other design objects, the layout will still meet

minimum density requirements for interconnect. If certain tiles fail to meet the minimum density requirement, the dummy fill tool may be used to add additional dummy metal at legal locations until the minimum interconnect density requirement is met, but it is not required to do so. (*See* 4:13–17.)

75. The significant efficiency gains from the ability to implement ECOs without having to rerun the dummy fill tool are repeatedly described within Lakshmanan '803. (*E.g.*, 1:46–50, 1:60–65, 2:20–22, 3:12–17.) This helps IC manufacturers "meet aggressive design schedules even though run-times for inserting dummy metal in large designs can be significant, and therefore saves time on overall design execution." (*Id.* at 4:52–57.) Based on my experience in semiconductor layout and design I agree that this new and improved process flow results in substantial efficiency gains in the design process for modern semiconductor devices. These gains are so substantial, and these incremental methods of dummy fill are so widely used today that it is hard to quantify just how important the inventions claimed by Lakshmanan '803 are to achieving current time-to-market for modern chip designs.

76. Based on my experience in semiconductor layout and design, it was not well-understood, routine, or conventional at the time of Lakshmanan '803 to perform dummy fill in an incremental fashion. In particular, it was not well-understood, routine, or conventional to identify dummy metal objects that, following an ECO, intersected other design objects and then delete such intersecting dummy metal objects from the design database. This feature, central to Lakshmanan '803, is required by every claim in the patent and recited explicitly in both independent claims. This is not only true in considering that element by itself, but also in an ordered combination with the other recited claim elements in creating a novel process flow that did not require a full-layer dummy metal fill simply to account for the relatively few objects that would intersect other design objects after an ECO.

77. Lakshmanan '803 explains, "A conventional design flow using a conventional dummy fill tool would require that the dummy fill tool be rerun after each change order was implemented to recompute the dummy metal 18 required for the design, severely impacting aggressive timing schedules." (3:12–17.) Rather, as I have explained, the typical process flows and all the dummy fill tools of which I was aware lacked the capability to accommodate ECOs without a full-layer re-run of the dummy fill tool. Nor am I aware of any "unconventional" tools or process flows dating to the time of Lakshmanan '803 that had such capabilities.

78. During prosecution of the application that matured into Lakshmanan '803, the patent examiner expressly agreed in the Notice of Allowance that the claims as issued satisfied the requirements of 35 U.S.C. § 101. The examiner specifically agreed with Applicant's arguments that the practical benefits of the claimed invention, which resulted in substantial time-savings by avoiding having to re-run the design tool after a portion of the design data changed provided sufficient basis for patent eligibility. I agree with the examiner and the applicant.

Claim Charts

79. I have reviewed the Complaint supported by this Declaration, along with the Claim Charts showing infringement of Hoff '626. For at least the reasons set forth below, I agree that the Claim Charts establish use of at least one of the methods recited by the respective claims of Hoff '626.

80. I have used design tools from different vendors in my career. As a consultant, I use the tools to review schematics and layouts, which has included industry-standard tools for detection of texted metal shorts. Based on the requirements for the latest process technology nodes, and the yield requirements for these technologies, the latest fill tools that are used by designers use timing-aware fill routines with minimum fill dimensions to meet timing as well as yield requirements simultaneously. These tools typically operate on an incremental basis; although

they can and do perform routing and insert dummy fill on a layer-by-layer basis, they typically operate in incremental fashion thereafter so that the impact of layout changes and ECOs to the overall design schedule is minimal and does not require rerunning the routing and dummy fill tool for the entire layer for each and every change. As I have done as a consultant, I can review either layouts post-fill or reverse engineering ("RE") of semiconductor die to confirm that these tools have been used to construct the layout or the die.

81. Given the aggressive schedules for bringing modern semiconductor devices to market, and the availability of incremental dummy fill in common design tools like Cadence's Innovus product, it is unlikely (if not implausible) that most chip designers would not have access to design tools that practice the inventions claimed in Hoff '626 and Lakshmanan '803. I am aware that at least Cadence provides this functionality. It is even less likely that such designers would not use the incremental dummy fill features that allow ECO without a time-consuming (and design-freezing) repeat of the dummy fill insertion process for the entire layer whenever the layout changes or another ECO is implemented. Especially because these typically happen late in the design process, and often happen more than once, any entity who declined to use these features would be at a substantial competitive disadvantage in bringing its products to market in a timely fashion. As such, based on my experience in semiconductor layout and design, and my review of designs and supervision of designers that used such tools, I believe that it is highly unlikely that such functionality was not used in creating most modern semiconductor devices.

82. Even when the full history of the GDSII database for a particular integrated circuit is not available, my experience in semiconductor design and layout gives me sufficient basis to opine whether one or more of the methods claimed in Hoff '626 have likely been used in creating integrated circuits.

83. Given the multiple dependencies in the semiconductor processing design flow and the reality of ECO after layout has been completed, I believe that it is highly unlikely that anyone using the Cadence Innovus tool (or another design tool with similar functionality for incremental routing and dummy metal fill) to create a modern IC would not have used at least one of the inventions recited in Hoff '626 to minimize the delay from having to re-route every net following an ECO, and then re-do the dummy fill. Likewise, I believe that it is similarly unlikely that anyone using the Cadence Innovus tool or another tool with similar functionality would not have used at least one of the inventions recited in Lakshmanan '803 to minimize the delay from a post-routing ECO. The delays from having to manually re-run the routing and the dummy fill tool after each ECO or layout change is so impactful that failure to use these now-commonly available tools would result in a severe competitive disadvantage and substantial delays in bringing products to market.

84. By contrast, based on my experience in semiconductor layout and design, I would only assume that relatively simple IC designs would have been made in recent years without employing at least one of the methods claimed in Hoff '626 and Lakshmanan '803.

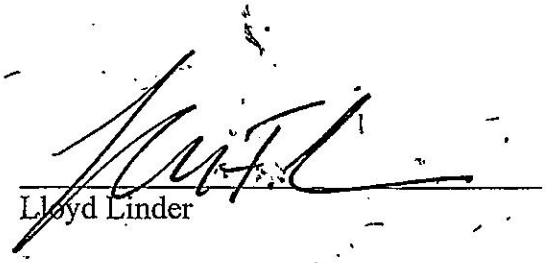
85. In addition, based on my experience, it can be assumed with a high degree of confidence that modern components in the same family or product line made by the same producer and used by the same customer in the same product line share similar features and were designed and laid out in similar fashion. For example, I would expect with a high degree of confidence that two RYZEN processors made by AMD (such as the Ryzen 7 1700 and 5 5500U processors) or two Qualcomm Snapdragon transceivers (such as the Snapdragon 865 and 665 transceivers) would have similar performance specifications, be used for similar (if not identical) purposes by similar clients, be built on the same knowledge base and design history of prior generation devices, and thus share substantially similar design philosophies. Given that these are cutting-edge, modern

devices, I expect that their production similarly involved incremental layout and routing methodologies following at least one of the methods claimed in each of Hoff '626 and Lakshmanan '803.

86. The Cadence paper "New Metal Fill Considerations for Nanometer Technologies" demonstrates several things. First, the use of the word "new" is justified in that it is a new approach, as documented here. Secondly, it reinforces the importance of formulating "a comprehensive methodology surrounding metal fill . . . in order to minimize impact on design timing as well as to cut down on design iterations." The paper explains that "sometimes the dummy metal fill geometries that were added to the original design must be deleted to make room for the ECO process to succeed," before identifying the solution as ignoring the effect of ECO on dummy fill in the first instance. The paper elaborates that allowing ECO "to cause shorts and/or DRC violations" from existing dummy fill following an ECO, and then repairing any violations will reduce the overall time to complete the ECO, including handling of the metal fill and its effects. Overall, this evidences that the Cadence tool suite is used for incremental dummy metal fill modification following ECO as claimed in Lakshmanan '803.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Dated: October 12, 2022



Lloyd Linder

EXHIBIT 1

cell 818.632.9660
lflinder@yahoo.com
09/22/2021

Lloyd F. Linder

Skills summary

Extensive experience in high performance / high dynamic range analog mixed signal, custom digital, and RF integrated circuit design, layout, and test, from concept to production for commercial, military, and space IC products. Have knowledge of IC process development, characterization, and modeling. Have significant amount of experience in obtaining new military, space, and commercial IC business, as well as obtaining funding for start-up activities. Technical oversight for large IC design teams (20-40 people). Have ability to contribute creatively to the solution of difficult technical problems. Have 99 U.S. patents issued with twenty U.S. patents pending. Have 200-300 issued international patents. Have experience at the discrete analog / RF / mixed signal board level design and layout, system analysis, link budget analysis.

Specialties:

IP analysis / technical due diligence for M&A

IP portfolio management and creative contribution to new IP generation

Prior art searches and technical support for patent office action amendments

Perform simulations, review IP, and provide expertise in support of patent litigation

System Design/Architecture/Analysis/Block Specifications

New business development/capture

Winning proposals for small (SBIR Phase I and II) and large businesses

Product road maps

VC funding pursuits

Technical due diligence for VCs, angel investors, and M&A

IP creation and protection

Client deposition

Technical lead for IC design groups and product development

AMS/RFIC Design Chip/Circuit/System Architect

High speed, high performance ADC, Sample/Hold, ADC drvier amplifier, and DAC architectures

RF/AMS/SOC BIST/DFT architectures and methodologies

PLL and DDS

Digitally programmable RF transceivers/SDR/GPS/cellular/wireless transceiver architectures

RF TxRx, optical TxRx, modulator driver, LDD, TIA

Flash Ladar, active/passive imaging ROIC

regulators, high voltage/high current switches, ATE electronics

SiGe BiCMOS, CMOS, SOI, bipolar, Complementary bipolar, GaAs, InP

Digital beamforming

Cadence tools - schematic capture, SPECTRE, layout review

Solutions to production problems
Secret clearance

Objective

Looking for consulting opportunities to utilize my experience and provide technical leadership in all aspects of analog / mixed signal / RF integrated circuit and discrete circuit design: architectural conception, design, simulation, layout, test, and measurement / simulation correlation.

Experience

April 2006 – Present
Lloyd Linder Consulting
Consultant
Black Forest Engineering / Luminar Colorado Springs, CO.

- Architecture development for next generation automotive lidar ROIC

Strategic IP Initiatives Inc. Morgan Hill, CA.

- Review of patent portfolio for PIC applications in SFP optical modules

GreyB Service Pte Ltd Shaw Centre, Singapore.

- Provide expertise for many different invalidity cases for many different clients

Upwork Santa Clara, CA.

- Technical writer for application notes and VNA user's guide

Syrnatec Inc. Newington, CT.

- Consult on ROICs for SBIR proposals

Kenney&Sams, P.C. Boston, MA.

- Expert witness in software defined radio development case

Microchip Technology Inc. Burnaby, Canada

- Participated in ADC architecture study for 28 and 56 GBps SERDES products.
- Did webinar for world-wide IC design staff on ADC design issues.

ElevATE Semiconductor Carlsbad, CA.

- Write white paper on ATE products.

GoodIP GmbH Munich, Germany

- Review and analysis of GaN and LED patent portfolio for potential acquisition.
- Spoke as the GaN / LED IP expert at webinar to discuss IP auction.

Nevada Nanosystems Inc. Reno, NV.

- Review and analysis of ASIC architecture and requirements in support of MEMS control circuitry. Evaluate IC design houses in the down-select process.

Axzon Inc. Austin, TX.

- Contribute to the analysis and review of CMOS transceiver architecture for UHF RFID reader.

Microcosm Inc. Torrance, CA.

- Architect the discrete RF transceiver and analog base band signal processing solution for digital beamformer. Develop packaging concepts for the beamfomer and interface to the antenna elements.

Otava Inc. Moorestown, NJ.

- Contribute to the definition of overall transceiver and circuit architectures for 5G beam formimg solution for 28-40 GHz 5G applications.

Analog Circuit Works Boston, Mass.

- Review of specification for fiber optic SOC application. Contribute to system level analysis and architecture.

Second Sight Medical Sylmar, CA.

- Debug of current eyewear for blind people. Contribute to reduction of noise and coherent spurs in current product.

Linear Microsystems Irvine, CA.

- Architect for high volume SOC for VR headset application. System analysis for SOC proposal for fiber optic communications applications.

Teqnovations Colorado Springs, CO.

- System level architect for receiver for phased array radar applications.

Analog Devices Inc. Colorado Springs, CO.

- Work with design team on a DAC buffer IC to improve performance in the lab and remove oscillation. Review existing architecture for redesign and developed new architecture.

Facebook Woodland Hills, CA.

- Schematic and board layout reviews of electronics for flight system

GHB Intellect San Diego, CA.

- Review of Patent claims for client for multiple issued patents in the wireless communications area.

BINJ Labs Scituate, MA.

- Definition of top level Software Defined Radio architecture for wide band operation. Work with board development effort and SDR development company.

Sentinel Monitoring Systems Inc. Tucson, AZ.

- Schematic review of high speed data converter and timing board schematic.

FlexPowerControl Woodland Hills, CA.

- Consultation on system level requirements document in-home energy control product development. Develop IP for the company.

SpectraResearch Dayton, OH.

- Consultation on integration considerations for discrete X-band and Ka / Ku-band transponder architecture for SWAP-C improvements.

McKool Smith Dallas, TX.

- Perform simulations of IP for RFIC receiver, and provide expert opinion for patent litigation in a report for case :2:15-cv-00011-JRGRSP in the United States District Court for the Eastern District of Texas.

Quantum Semiconductor LLC San Jose, CA.

- Consultation on architecture and simulations for proprietary ADC architecture.

Maven Research San Francisco, CA.

- Consultation on use of design house by third party for products.

Faraday Technology Corporations Santa Clara, CA.

- Review of third party transceiver RFIC schematic design, layout, and testability.

Irunway Dallas, TX.

- Review of IP for legal firm in patent litigation. Simulation of IP for transceiver RFIC. Simulation results included in expert report.

Alphacore Inc. Phoenix, AZ.

- Architecture review and enhancements of high speed CMOS ADC and visible monolithic imaging chips. Develop DROIC architectures for SBIR proposal pursuits.

Brady Worldwide Inc. Milwaukee, WI.

- IP review of start-up for potential investment / acquisition. Develop sensitivity analysis for present products and future CMOS technology scaling.

InPhi Corporation Westlake Village, CA.

- Review and contribute to architecture refinements for single channel and multi-channel EAM drivers for 2 level and 4 level PAM. Perform architecture study for low power EAM driver.

DRS RSTA Inc. Cypress, CA.

- Help with EDA methodology for AMS design for ROICs.

Ridgetop Group Tuscon, AZ

- Architected wide band RF front end for multiple current SBIR proposals.

Space Micro San Diego, CA

- Review of 0.18 μm CMOS quadrature DAC design and layout.

Teradyne Agoura Hills, CA

- Analog DFT / BIST / testability architect for 40 nm CMOS SOC for next generation Teradyne tester. Architect transistor level circuit solutions for power supply IC for DUT testing. Investigate high voltage CMOS and complementary bipolar process technologies for internal design development with unique current clamping architecture. Define baseline circuit topology and perform simulations.

Lockheed Martin Moorestown, New Jersey
Littleton, Colorado
Deer Creek, Colorado

- Involved in high voltage driver IC development for GaN PA.
- Involved in architecture development and review of wide band band receiver integrated circuits from DC to Ka / Ku in SiGe.
- Involved in overall ADC architecture development and definition, and transistor level circuit architectures, for next generation RFIC transceivers and data converters. Architect of next generation transceiver architectures for SOC / heterogeneous applications. Involved in study for government customer of data converter architectures for next generation digital beam forming applications. Architecture review and development for high voltage analog driver array. Involved in architecture for multiple receiver RFIC developments for S, C, and Ka bands.

HRL Malibu, CA

- Perform market survey of component technologies for multi-mode, multi-mode commercial software defined radio applications. Summarize capability for data converters, front end modules, antennas, transceivers, and base band processors. Compare the available technology to an architecture based on custom chip development for the solution.

Micrel San Jose, CA

- Involved in the testing, debug, and redesign of a 65 nm CMOS 2.4 G / 5 G WiFi transceiver product. Provide technical guidance for redesign of RF front end and the 2.4 G / 5 G LO clock distribution.

Key2Mobile Westlake Village, CA

- Developed RF transceiver concepts for multi-band, multi-mode remote radio head system. This is included transceiver architectures based on digital beam-forming and direct RF sampling and direct RF synthesis data converters.

Hittite Microwave Colorado Springs, CO

- Consultant on the architecture for the high dynamic range, high speed IBM SiGe 8HP BiCMOS DAC and complementary bipolar ADC driver amplifier products for the cellular base station market.

Semtech Redondo Beach, CA

- Technical consultant on IBM SiGe 8HP BiCMOS interleaver IC and IBM 32 nm SOI monolithic coherent detection transceiver SOC for 100G coherent optical detection systems. Involved at the architectural level for the SOI interleaver, 8

bit, 64 GSPS ADC, and 8 bit 64 GSPS DAC circuits, and overall system calibration.

- Developed concepts for 10-12 bit, 4-8 GSPS ADC architectures for digital array radar and digital beam-forming applications, as well as high performance sample and hold architecture for military applications.

FBI Westwood, CA

- Technical consultant on matters of national security. Awarded medal for service to the country.

Nu-Trek Inc. San Diego, CA

- Developed an RF BIST architecture for characterization of a RF transceiver. Helped the company win Air Force Phase I and Phase II awards.
- Involved with test evaluation of pipeline ADC for cryogenic applications, L1 / L2 band GPS receiver, and Universal Reliability SOC development for lifetime testing of X-Band and L-Band transceivers.
- Responsible for the development of the company's product roadmaps.
- Contributed to SBIR and STTR proposals on nonlinear coupled oscillators for active array applications, active sonar signal processing, high dynamic range ADC, GPS, RFIC transceivers, RIICs, and ROICs. Involved in testing of ADCs for ROICs, and architecture development for RF BIST.

FLIR Electro-Optical Components Ventura, CA

- Technical lead for the development on ROIC architectures for NASA, Navy, Air Force, MDA, and Army SBIR Phase I and Phase II programs. Development of novel active and passive unit cell architectures.

SYS Technologies / Kratos Defense San Diego, CA

- Review of SiGe BiCMOS class E power amplifier design to improve reliability of operation. Reviewed circuit, simulation results, test results (dynamic and DC), and performed thermal analysis based on self-heating.
- Review of schematic and layout for small form factor PCB that contains GPS transceiver RFIC and companion digital ASIC. Review of schematic and layout for PLL, IF / baseband test chip evaluation boards. Suggestions for characterization / test debug.
- Review Transmitter and Receiver schematics and block layouts of GPS transceiver IC in IBM 7HP 0.18 μm SiGe BiCMOS for redesign effort. Review of improved receiver IC design.
- Review of test results for the evaluation board and suggestions for characterization and debug. Review of board design and layout revisions for improved electrical and thermal drift performance for successful demo. Help with board yield and manufacturing issues.

Aerius Photonics LLC Ventura, CA

- Technical lead for STTR Phase I ROIC circuit design partner.
- Developed ROIC architectures for laser vibrometer SBIR Phase I proposal.

LinearChip Inc. Aliso Viejo, CA

- Developed complete single chip CMOS 802.11 a/b/g/n/ac transceiver architecture, with on-chip T/R switch, for proposal to commercial test equipment house.
- Developed CMOS MSK transmitter for patient temperature monitor and medical equipment tracking ASIC. Developed overall quadrature transmitter architecture, circuit topologies for the DAC, active filter, quadrature mixer, power amplifier, and temperature stabilized reference oscillator. Performed noise / distortion budgets, duty-cycled power calculations for extended battery life, determined PLL phase noise requirements, and defined the circuit block specifications.

Technical lead for the circuit simulations in XFAB XH018 0.18µm CMOS RF process.

- Participating in pursuit of new IC design business. Development of PHEMT TIA gain block concept, satellite receiver / de-multiplexer architecture, CMOS and SiGe RF receiver architectures, and CMOS analog AFE for hand-held controller for telescope, including 16 bit audio DAC architecture. Involved with multiple RFIC proposals for military and commercial applications. Developed multi-channel AM/FM receiver for location positioning application.
- Developed unique TIA / AGC / output amp circuit concept for cable TV over fiber market based on JAZZ 0.18µm SBCH18XL SiGe BiCMOS process.
- Review of battery charger circuit architectures for XFAB XC06 0.6 µm CMOS IC. Architecture suggestions for capacitor charging loop and low battery indicator circuit.

Wistron Corporation Taipei, Taiwan

- Contributed to discrete quadrature receiver architecture for a new module business proposal to DirectTV.
- Involved with review of existing ODU L-Band module specifications, and application to new digital L-Band module. Contribute to the definition of ASIC requirements and discrete component requirements for new ODU architecture.

Arete Associates Sherman Oaks, CA

- Phase I and internal IRAD programs for advanced TIA architecture development for high speed laser pulse return processing.
- Review of schematics, simulation results, and layout floor plan, and layout for a 64 channel TIA / OTA wavelength converter in IBM 5HPE 0.5µm SiGe BiCMOS. Function is to receive 1 ns laser pulse and provide linear gain for retransmission. Made suggestions for additional simulations for design robustness and concerns, as well as improved performance based on layout changes. Also made layout suggestions for improved isolation and performance.
- Developing unique 3D FPA and digitally programmable ROIC pixel unit cell architectures for inclusion in STTR proposal.
- Review of 2 TIA input / 128 channel output VCSEL driver, 2 GHz pulsed sampling IC in IBM 7WL 0.18 µm SiGe BiCMOS.

Raytheon Corp. Dallas, Tx. / El Segundo, CA

- Involved in the development of 40 GSPS ADC architecture in 32 nm IBM SOI.
- Involved in development of on-chip mechanical stress measurement circuit for thermal imaging sensor IC in IBM 9SF 90 nm CMOS process. Submitted patent disclosure on stress sensor circuit. Reviewed the pixel circuit design and the overall ROIC circuitry and timing.
- Participated in winning MDREX proposal effort to AFRL to develop high performance 10 bit, 2.2 GSPS ADC, 14 bit, 3 GSPS DDS, and 1:4 DMUX ICs in IBM 8HP 0.12µm SiGe BiCMOS, and integrate these functions with 8HP receiver and transmitter circuits developed by AFRL, as well as 8HP bias and control circuits developed by Raytheon. Involved with Phase I kick-off meeting.
- Participate in SBIR proposals development with partners Nu-Trek and Crossfield. Developed design methodology for CMOS GPS SOC integration. Developed sub-threshold CMOS RF circuits for low power GPS receiver concept. Generated phase adjust circuit for RF clock distribution for antenna array electronics, and submitted patent disclosure. Contributed write-up on high speed, high performance DAC topologies for DDS proposals. 1 Phase I SBIR proposal awarded.

- Schematic and layout review of IBM 7HP 0.18µm SiGe BiCMOS digital control and bias regulation circuits for MMIC common leg circuit. Reviewed regulator loading problems, solutions, and simulation results. Made simulation recommendations for verification of design robustness. Reviewed metal mask fixes.
- Review of test data, process parameters, and circuit design for production HRL G1.5 2µm InP band-pass Σ-Δ IC for yield enhancement. Developed vendor RFQ for multi-phase IC redesign effort.
- Involved in metal mask effort for 14 bit, 3 GSPS DDS / DAC IC in IBM 7HP 0.18µm SiGe BiCMOS through the Trusted Foundry program. Contributed to design, layout changes in the high speed digital DLL section to improve performance for higher clock applications. Documented circuit design limitations for future redesign for clock rate enhancement.
- Analyzing test data, PCM data for the metal mask DDS chip. Correlate sensitivity of test results to process parameters, and simulation results, to improve yield on future fabrications. Investigate design improvements for possible new mask set. Provide suggestions for performance improvements at the board level. Involved in improvements of the DLL section for next all-layer mask release.
- Member of team analyzing radiation induced latch-up effects in commercially available data converter for space application. Involved in focused laser beam testing to create single events in the converter. Analyzing radiation data, reliability data, and design guides for end-of-life DC power estimates for ICs designed in NS 0.8µm ABIC-IV BiCMOS, MAXIM GST-1 bipolar, IBM 5SF CMOS, and Honeywell HX3000 SOI.
- Review of link budget and block performance for IF and base-band ICs implementing high dynamic range receiver, including IF amp, mixer, VGA / attenuator, and ADC driver amp in IBM 5HPE 0.5µm SiGe BiCMOS. Made architectural suggestions for improved performance. Reviewed test results, and made suggestions for debug.
- Design review of IBM 5HPE 0.5µm SiGe BiCMOS IF receiver ASIC including mixer, gain control amp, and ADC buffer amplifier. Review of measurements for test circuits.
- Jitter analysis for ADC module clock path using divider circuits.
- Design reviews of IBM 5DM 0.5µm SiGe BiCMOS L1 / L2 GPS dual channel receiver IC: LNA1, LNA2, RF amp, RF mixer, IF mixer / AGC, gain calibration loop, baseband amp, PLL, and ADC. Defined layout floor plan, channel layout isolation techniques, and package requirements to meet isolation requirements. Reviewed final GPS receiver layout and developed plan for simulation of layout, package, and external component parasitics. Contributed to correlation of test results. Review of socketed test board layout.
- Review of quad channel IQ detector hybrid design and layout. Made suggestions for debugging of existing hybrid oscillation and improved performance. Review of TI BiCOM-2 0.7µm CBiCMOS IQ IC performance and correlation to hybrid measurement.
- Review of simulations and test results for IBM 8HP 0.12µm SiGe BiCMOS millimeter wave transceiver chipset module performance from outside vendor.
- Review of M/N PLL hybrid design. Review of TI BiCOM-2 0.7 µm CBiCMOS M/N PLL IC performance and correlation to hybrid measurement.
- Performed BOL and EOL noise analysis to estimate the jitter of on-chip clock receiver circuits for the SPT7760 ADC IC based on the MAXIM GST-1 process parameters, and off-chip COTS components for satellite application.

Menara Networks Irvine, CA

- Reviewed schematics and simulation results for high frequency, multi-GHz active RF low pass filter in JAZZ SBC18HXL 0.18µm SiGe BiCMOS. Involved in top level layout review of first generation EDC IC.
- Contributing to the development of Nyquist 10 GSPS sample / hold circuit, for hold mode feed-through reduction, low distortion, and low power. Contributed to the DC AGC circuit to generate coefficients for Gilbert multiplier as well as developed a new summing circuit for the sampled signals in the analog sampled FIR filter. Involved in solving layout-induced performance problems.
- Involved in the clock distribution architecture and feedback loop to reduce DC offset effects on zero crossing. Review of regulator circuit power-up issues. Created new ADC-based residue architecture to generate the appropriate transfer function for a phase detector circuit for consideration on a higher performance, lower power version of the existing Fiber Optic Receiver IC in JAZZ SBC18HXL 0.18µm SiGe BiCMOS.
- Preliminary review of third party design of 10 Gb/sec CDR PLL schematic blocks for SOC application in STM 0.13µm SiGe BiCMOS. Reviewed metal mask circuit design changes.

MOSIS / ISI Marina del Rey, CA

- Review of MOSIS website. Provide report consisting of ways to improve technical and business information on the website, as well as customer support. Used client questionnaire to provide additional insight into website, technical information, customer service and support.

Tangea Semiconductor Manhattan Beach, CA

- Participated in business plan development, facility requirements, engineering manpower requirements, technical concepts, and potential investor meetings.

Technoconcepts Inc. / Terocelo Van Nuys, CA

- Involved in the design, development, and review of RF receiver and transmitter ICs for multi-band, multi-mode applications using JAZZ SBC18HXL 0.18 µm SiGe BiCMOS. Versions of the Receiver IC include RF VGA, mixer, RZ (Return-to-Zero) and NRZ (non-Return-to-Zero) 6 GSPS 1 bit Σ-Δ ADC, with 2 feedback DAC and 3 feedback DAC versions, PLL, 1:16 DMUX, and base band decimation and filtering. Activities include circuit-level architectures to improve existing performance, schematic and simulation reviews, top level layout floor-planning, layout review, and evaluation board review.
- Involved in testing and correlation of packaged part performance, to simulation, for noise density, harmonic distortion, and intermodulation distortion products. Involved in architecture improvements and enhancements, based on test results, for a metal mask effort. Improvements include extension of VGA architecture to extend the input 1 dB compression point, IIP3, and bandwidth. Added provision to sample very low input frequencies. Improved the dynamic range of the transconductance amplifiers in the modulator. Added dither DAC at the comparator input to improve idle tone performance. Extended the dynamic range of the present RZ Σ-Δ design. Improved the DAC settling and noise response. Added an LNA, and a single-ended to differential converter to interface to the existing VGA.
- Development and layout of test chips for the TSMC 90nm CRN90LP CMOS RF process. Designs include single-ended, wideband and tuned versions of high IIP3 LNA architectures using novel distortion cancellation techniques for operation in the 1- 6 GHz frequency bands. Also developing versions of a 1.8V bidirectional, tri-stated CMOS / LVDS I/O driver with resistive and active back terminations,

and a single input, multi-band, multiple output, switched / tuned RF front end. Involved with CASCADE probing, and correlation to simulation results.

- Development of a wide-band, software defined, multi-band, multi-mode, receiver chip for the TSMC 65nm CRN65GP mixed signal / RF process. Architected the circuits for the wideband LNA with novel AGC and attenuator, the RF DMUX / on-chip RF filter bank, the RF MUX / single-ended-to-differential converter, the quadrature mixer with AGC, RSSI log amp, and the programmable base-band filters. All the RF blocks utilize IM3 cancellation. Target services include AM, FM, DTR, DTV, WiFi, and WiMAX for automotive application for Japanese customer. Involved in the link budget analysis, block specifications, and the requirements for the associated base band ADC and PLLs for the high band LO, low band LO, and ADC LO ICs. Also proposed this architecture for NSF proposal in order to obtain additional development funding.
- Involved in the design, layout, and review of customer demonstration board, based on existing transceiver chipset, for WiMAX applications, using Picochip base-band processor.
- Developing transceiver architecture concepts for multi-service / simultaneous /switched reception off of single multi-band antenna, diversity, and MIMO with self-calibration. Developed low power architecture for multi-service receiver summing into single ADC. Developed transmit / receive architecture for multi-band, multi-mode military radio. Architectures are baseline for new business opportunities.
- Developed IBM 0.12µm 8HP SiGe BiCMOS low power LNA topologies for 10-20 GHz for SBIR proposal. Developed RF interference cancellation architecture for SBIR proposal.

Red Dot Wireless Milpitas, CA

- Performed transceiver architecture study for TD-SCDMA / EVDO / WiFi / MIMO WiMAX application. Involved in presentations to investors.

Ubidyne Ulm, Germany

- Schematic, simulation, and layout review of IHP SG25H1 SiGe BiCMOS S1.0 Receiver RFIC. Review of characterization test results.
- Schematic, simulation, and layout review of JAZZ SBCH18XL SiGe BiCMOS S2.0 receiver, transmitter, and PA driver IC designs. Schematic and layout review of Toshiba 90nm CMOS high speed custom digital IC design.
- Review of test data and circuit design for S2.0 receiver to determine yield issues.

Dynamic Research Corporation San Diego, CA

- Review of existing top level IC issues and proposed packaging approach for GPS transceiver in IBM 7HP 0.18 µm SiGe BiCMOS.

Q3Web Wideband Wireless Inc. Harbor City, CA

- Constructed white paper on the development of IP libraries in the IBM CMOS and SiGe BiCMOS technologies for use by military contractors. Being submitted to government for funding consideration.

August 2009 – May 2011 Aerius Photonics Ventura, CA.

Senior Systems Engineer

- Directly responsible for winning new SBIR business for ROIC development. Captured $2.6M of ROIC development money. Have written multiple winning proposals for Army, Navy, MDA, NASA, Air Force, and NSF SBIR Phase I efforts. Have won Navy and ARMY Phase II efforts. Additionally, supported other proposal wins for other technology developments.

- Responsible for the development of new and novel circuit concepts for CMOS and SiGe BiCMOS passive and active imaging ROICs. Have found and engaged ROIC design partnerships. Involved in new business development.
- Have defined ROIC specifications and system requirements in conjunction with BALL Aerospace, Sensor Creations, Raytheon, BAE Systems, Arete and Associates, Tetravue, IDEO, Microvision, Velodyne, and other military and commercial contract partners.
- Technical lead for the conceptual phases of the following ROIC developments: JAZZ SBC35 ROIC for laser vibrometry, ON Semiconductor C5 0.5µm ROIC for 3-D FLASH LADAR for beach zone / surf zone applications, ON Semiconductor C5 0.5µm CMOS ROIC for dual well application (patent pending), JAZZ SBC18 CMOS monolithic imaging ROIC with integrated SiGe APD, and ON Semiconductor 0.18µm CMOS 1920 X 1080 SWIR ROIC.
- Contributed to the development of new laser range finder receiver architecture with unique time programmable gain.
- Developed digitally programmable pixel architecture and specifications for linear direct / coherent detect ROIC for STTR Phase I effort.
- Technical lead in development of single pixel discrete board level customer demo for STTR Phase I LADAR application, and board developments for: 10 Gb/second hexagonal InGaAs detector array, custom ROSA and CDR, 4 X 4 array with fan-out electronics in support of sub-ns laser returns, and new laser range finder receiver.

April 2008- January 2009 Menara Networks Irvine, CA

Director of ASIC Development

- Involved in simulations of existing Electronic Dispersion Compensation (EDC) IC to correlate to measured performance to define metal mask effort for JAZZ SBC18HXL 0.18µm SiGe BiCMOS IC. Helped define testing for chip characterization.
- Patent application on interleaved FIR with unique sample / hold for extended high dynamic range over previous implementations.
- Contributed to architectural improvements for low power version of EDC IC in IBM 8HP 0.13 µm SiGe BiCMOS.
- Performed simulation trade-off study to compare circuit performance for transmitter application in TSMC CMN65LP 65 nm CMOS, IBM 10LPE 65 nm CMOS, and IBM 8HP 0.12µm SiGe BiCMOS.
- Simulation and design of transmitter pre-driver and output driver for quad 10 Gb/s transceiver with integrated EFEC in IBM 10LPE 65 nm CMOS.
- Simulated low power EML driver concept in IBM 8HP 0.12µm SiGe BiCMOS.
- Involved in the investigation and development of new architectures in support of 100 Gbit/s optical links.
- Review of board schematics and layouts for EDC IC evaluation board, OTN XFP module, and OTN 300 pin module.

February 2002- April 2006 TelASIC Communications El Segundo, CA

Director of Technology / Founder

- Technical lead for next generation single supply (+5V) data converter ICs in IBM 0.5 µm 5AM SiGe BiCMOS: RF sampling 10 bit, 1 GSPS ADC, on-chip sample / hold, and up-converter IC with integrated 14 bit, 1 GSPS DAC, IF amplifier / mixer. Developed self-heating error correction for quantizer preamp.

- Technical lead for new business pursuits in military and commercial integrated circuits. These included RF handset transceivers, spot BTS, fiber optics, analog transmit cancellation receiver for Gigabit Ethernet, automotive radar, data converters, sample / hold, FPA imaging sensor readout, and arbitrary waveform generators. Technical lead in new business pursuits in board-level DPD-based transceivers based on COTS components. Involved in proposals with Raytheon for DARPA programs, including RHBD (Rad Hard by Design) and Team Phase II.
- Technical advisor for the conception, development, and commercial production of the TC2412 14 bit, 737 MSPS DAC IC and TC1412 14 bit, 250 MSPS ADC IC in IBM 5AM (data sheets available at www.telasic.com/website/products). Architectural contributor to base station transceiver chipset concept. Data converter IC products are being sold to PMC for the NTT DoCoMo base station market. Involved in development of IBIS models of DAC and ADC IC for customer board level simulations.
- Technical contributions to various IC designs including IBM 5AM ADC driver amps, Re-sampler, IBM 7HP test chips, including sample / hold, amplifier, mixer, ring oscillator, and 14 bit, 3 GSPS DDS. IBM 8T chips including re-sampler and 3 bit / 40 GSPS sample / hold / Quantizer / DAC.
- First version of the ADC IC developed, TC1411, received analogZone 2003 Product of the Year Award.
- Involved in business plan development, process to obtain first round of funding.
- Performed technical due diligence on potential new investments for venture fund.

1999– February 2002 Raytheon Advanced Products El Segundo, CA

Engineering Fellow

- Technical lead for new business pursuits in military / commercial ICs, working with organizations across the company. Programs won include: SIMBAW, TEAM, ADRT, ULTRACOMM, ACN, 3D Flash Ladar image sensor, and APLA.
- Involved in FPA multi-sampling ROIC developments in AMI 0.5µm CMOS: 10 X 10, 64 X 48 arrays. Unit cell development in IBM 0.13 µm CMOS for 256 X 256 array. Developed fan-out concept to maintain small cell pitch while allowing for multi-sampling analog architecture. Evolved multi-sampling concepts for programmable sample time stamp and number of samples.
- Technical advisor for integrated circuit development across Raytheon. This includes design review / debug of existing IC developments.
- Involved in the design and development of data converters, IBM 5HP IF sampling Band-pass Σ-Δ, compact DDS, and RF transceivers for the military and commercial markets. Circuit concepts include fast frequency hopping PLLs, active biquad filters, and a sine weighted DAC.
- Developed Tondelayo 802.11a half duplex transceiver chipset in IBM 5HP for start-up (Systemonic) acquired by Philips. The transceiver demonstrated 802.11a frequency bands in the 5- 6 GHz frequency range using a PCMCIA format.
- Technical contributor to conversion of 0.6µm to 0.5µm NS CMOS for 14 bit, 10 MSPS radiation hard, algorithmic ADC. Involved in design and review process.
- Cooperative effort with LUCENT for next generation design improvements and completed plastic / ceramic package performance evaluation trade-off of CSP1152A CMOS 14 bit, 65 MSPS ADC for Sirius radio application.
- Technical evaluator for BOEING 0.35µm CMOS 1.0625 Gbit/sec Multi-channel Fibre Channel Transceiver for Raytheon AESA application. Contributed to

design reviews, layout reviews, design changes / iterations, suggested simulations to run, and evaluated test results.

- Developed concepts for the integration and packaging of RF MEMS devices with integrated circuits. Circuit architectures included RF front ends with tunable capacitors, tunable RF band-pass and notch filters, as well as active MUX circuits for frequency hopping between filters.

1993–1999 Hughes Communications Products El Segundo, CA

Senior Staff Engineer / Senior Scientist

- Technical lead of the development ICs for the Digital Receiver Program. This included NS ABIC-IV 0.8µm BiCMOS ICs with the following functions: LNA, mixer, LO driver, DAGC, fractional frequency hopping low phase noise PLL, IF amplifier, video amplifier, serial interface, log detection / blanking, and control logic, and a LUCENT CBIC-V2 summing amplifier IC. Involved in the packaging and test of plastic packaged parts. Digital Receiver board contained 2 chip UHF receiver, single chip GPS receiver IC, and master PLL IC.
- Technical lead for research and development of RF and analog ICs in CMOS, Hughes NB SOS / SOI, silicon (NS ABIC-IV, V, MAXIM SHPi), and IBM SiGe bipolar / BiCMOS process technologies. Functions included LNAs, RF LNA, mixer, VCO, ring oscillator, video amplifier, IF amplifier, sample / hold, high speed 10 bit ECL-to-CMOS translator / latch, 12 bit DAC, and LP Σ-Δ.
- Development of AM / FM LNAs in IC Delco 1.2µm CMOS for automotive radio.
- Involved in the chipset development for NS for the 1.0625 Gbit/sec ANSI X3T11 8B/10B standard using ABIC-IV process. Involved in laser diode driver, TZA, SIPO, PISO, Transceiver ICs.
- Involved with process development / modeling for CMOS, SOS, and silicon / SiGe BiCMOS process technologies.
- Team member of the NS ABIC-IV ADC chip development based on requirements for the ICO satellite system
- Involved in the debug, characterization, and production of hybrids and modules for airborne radar and AMRAAM missile applications.

1991–1993 Radar Systems Group, Hughes Aircraft El Segundo, CA

Staff Engineer

- Lead the IC development of high performance data converter components including sample / hold, summing amplifier, timing generator, band-gap, ADC reference amplifier, video amplifier, DAC, flash quantizers, and buffer amplifier in LUCENT CBIC-U / U2 and MAXIM SHPi and CPi processes.
- Involved in the development of mixer ICs for high dynamic range radar using HRL InP, AlGaAs, and Litton and Hughes D-MESFET technologies.

Fall Semester 1990 Electrophysics Department, USC Los Angeles, CA

Lecturer

- Taught EE448, Senior Electronics. Generated syllabus, created homework problems, tests, and solutions. Handed out final grades.

1986–1991 Radar Systems Group, Hughes Aircraft El Segundo, CA

Member of Technical Staff

- Involved in the design of components for high performance data converters.

- Contributed to the design of high dynamic range buffer amplifiers, sample / holds, integrators, and gain stages in Hughes 2 µm CBiCMOS, Fairchild 1.25 µm Fast-Z Fineline, and NS Aspect-II, Aspect-III, and ABIC-IV.
- Designed 2 bit adaptive threshold ADC IC in ORBIT 2µm CMOS for EPLRS radio.
- Contributed to architecture for Hughes NB 2 µm CMOS gate array ASIC.
- Involved with process development / modeling for bipolar, complementary bipolar, CMOS, BiCMOS, CBiCMOS.
- Generated analog tile array for the Hughes Carlsbad CBiCMOS process.

July 1985–1986 Radar Systems Group, Hughes Aircraft El Segundo, CA

Member of Technical Staff

- Involved in design of high speed digital ICs for the VHSIC (Very High Speed Integrated Circuit) program using Fairchild Fast-Z Fineline 1.25µm bipolar.
- Involved in design of high speed 64 X 16, 124 X 24, and 1K X 24 SRAM ICs.
- Contributed to the merged junction bipolar SPICE model.
- Designed current mode logic for UHSBL (Ultra High Speed Bipolar Logic) cell library in NS Aspect-III. Cells used in high speed MUX, DMUX, and DDS ICs.
- Developed digital IC architectures for high speed radar signal processing.

Education

1980-1985 UCLA Westwood, CA

- BS Electrical Engineering Summa Cum Laude, Phi Beta Kappa
- UCLA's Most Outstanding Senior Electrical Engineering Student

1985-1987 UCLA Westwood, CA

- MS Electrical Engineering

1987-1989 USC Los Angeles, CA

- Engineer's Degree Electrical Engineering

1990-Present USC Los Angeles, CA

- PHD Candidate under the advisement of Prof. John Choma Jr.
- Completed Thesis: "Nonlinear Error Correction for the Bipolar Canonic Cells."
- Designed, fabricated, and DC wafer probed amplifier circuits in MAXIM SHPi bipolar process to verify theory developed.

Publications

- M. Chambers and L. Linder, "A Precision Monolithic Sample- And-Hold for Video Analog-to-Digital Converters," ISSCC Feb. 1991.
- B. Felder, et al., "A Low Noise 13 Bit 10 MSPS ADC Hybrid with High Dynamic Range," GOMAC 1994.
- W. Cheng, et al., "A 3 Bit, 40GSPS ADC- DAC in 0.12µm SiGe," ISSCC Feb. 2004.
- O. Panfilov, et al., "Direct Conversion Transceivers as a Promising Solution for Building Future Ad-hoc Networks," International Conference on Next Generation Tele-traffic and Wired / Wireless Advanced Networking September 2007.
- O. Panfilov, et al., "Test Results of the Direct Conversion Transceiver Demo Board", November 2007 SDR Forum Technical Conference.

- O. Panfilov, et al., “Overcoming Challenges of Direct Conversion Software Radio,” IEEE International Design and Test Workshop December 2007.
- A. Varghese and L.F. Linder, “Software Defined Radios for Wireless Handsets,” April 2008 Wireless Design & Development Magazine.
- S. Elahmadi, et al., “A Monolithic One-Sample / Bit Partial-Response Maximum Likelihood SiGe Receiver for Electronic Dispersion Compensation of 10.7 GB / s Fiber Channels,” OFC / NFOEC March 2009.
- S. Elahmadi, et al., “A 50 dB Dynamic Range, 11.3 GSPS, Programmable Finite Impulse Response (FIR) Equalizer in 0.18µm SiGe BiCMOS Technology for High Speed Electronic Dispersion Compensation (EDC) Applications,” RFIC Symposium, June 2009.
- J. Edwards, et al., “A 12.5 Gbps Analog timing Recovery System for PRML Optical Receivers,” RFIC Symposium, June 2009.
- D. Baranauskas, et al., “A 6th Order 1.6 to 3.2 GHz Tunable Low-Pass Linear Phase gm-C Filter for Fiber Optic Adaptive EDC Receivers,” RFIC Symposium, June 2009.
- S. Elahmadi, et al., “An Analog PRML Receiver for up to 400km of Uncompensated OC-192 Fiber-Optic Channels,” ESSCIRC September 2009.
- S. Elahmadi, et al., "An 11.1 Gbps Analog PRML Receiver for Electronic Dispersion Compensation of Fiber Optic Communications," IEEE JSSC, vol.45, no. 7, July 2010.
- Montierth, D., Strans, T., Leatham, J., Linder, L., and Baker, R. J., "Performance and Characteristics of Silicon Avalanche Photo detectors in the C5 Process," 2012 IEEE Midwest Symposium on Circuits and Systems, Boise, Idaho.
- Rauch M. and Linder L., "Collaborating with Nu-Trek," 2012 HiRev Industry Day, December 2012, Los Angeles, California.

Awards / Achievements

- IEEE Senior Member
- Two-time Hughes Aircraft Division Patent Award winner
- 55 issued US patents, over 300 international patents, several US patents pending
- Numerous IC design team awards at Hughes and Raytheon
- Hughes Masters Fellow, Engineers Fellow, Doctoral Fellow
- 2008 IEEE San Fernando Valley Section Entrepreneurial Business Plan Competition Judge
- Menara Networks EDC IC Team Award – world’s first error free operation over 400 km of uncompensated fiber

IC Process Experience

- CMOS, silicon / SiGe bipolar, silicon / SiGe BiCMOS, complementary bipolar, CBiCMOS, SOI, SOS, GaAs D-mode / E-mode MESFET, AlGaAs / InP HBT

Skills

- CADENCE Analog Artist Schematic Composer, Spectre Simulator

Security Clearance

- Secret clearance is presently supported by Nu-Trek.
- US Citizen