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Attorneys for Plaintiff

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF OREGON

PORTLAND DIVISION

BELL SEMICONDUCTOR, LLC

Plaintiff,

v.

LATTICE SEMICONDUCTOR CORPORATION

Defendant.

Case No. 3:22-cv-1543

COMPLAINT FOR PATENT INFRINGMENT

JURY TRIAL DEMANDED

Plaintiff Bell Semiconductor, LLC ("Bell Semic" or "Plaintiff") brings this Complaint against Defendant Lattice Semiconductor Corporation ("Lattice") for infringement of U.S. Patent No. 7,396,760 ("the '760 patent"). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1. This is a patent infringement suit relating to Lattice's unauthorized and unlicensed use of the '760 patent. The circuit design methodologies claimed in the '760 patent are used by Lattice in the production of one or more of its semiconductor chips, including its LCMX02-7000HC.

2. Traditionally, the process flow for IC design is highly linear, with each phase of the design process depending on the previous steps. Accordingly, when revisions to portions of the physical design are made, as typically happens numerous times during the design process, all the subsequent steps typically need to be redone in their entirety for at least the layer, if not the entire device. This is because regardless of the size or extent of the revision to the physical design, the changes must be merged into a much larger integrated circuit design and then the remaining steps of the design process flow re-run.

3. Semiconductor devices include different kinds of materials to function as intended. For example, these devices typically include both metal (*i.e.*, conductor) and insulator materials, which are deposited or otherwise processed sequentially in layers to form the final device. These layers—and the interconnects and components formed within them—have gotten much smaller over time, increasing the performance of these devices dramatically. As a result, it has become even more important to keep the layers planar as the device is being built because defects and warpage can cause fabrication issues and malfunctioning of the device.

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4. Manufacturers use a process called Chemical Mechanical Planarization/Polishing ("CMP") to smooth out the surface of the device to prepare the device for further processing, such as deposition of another layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be "polished" away at different rates, leading to erosion or dishing on the surface.

5. To reduce this problem "dummy" material, also known as "dummy fill," is typically inserted into low-density regions of the device to increase the overall uniformity of the structures on the surface of the layer and reduce the density variability across the surface of the device. However, dummy fill can increase capacitance if it is placed too close to signal wires, which slows the transmission speed of signals and degrades the overall performance of the device.

6. Just as unwanted capacitance can result from the interaction of elements within the layer of an integrated circuit, it can also result from interaction of elements across adjacent layers. While certain elements (such as signal lines and power lines) cannot be easily moved without affecting circuit performance, there is substantially more flexibility regarding placement, positioning, and spacing of non-signal carrying features such as dummy fill, even when certain quantities of dummy fill are needed within layers and portions of layers to meet processing requirements.

7. Prior to development of the methodology described in the '760 patent, the placement of dummy fill in the open areas of the interconnect layer was performed based primarily upon meeting density requirements. To the extent that timing and capacitance effects were considered in dummy fill dimensions, orientation, positioning, or otherwise in dummy fill

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placement, the conventional dummy fill tools at the time only considered intralayer effects—i.e., interactions between dummy fill features and other elements (such as signal nets) on that same layer. However, use of dummy fill that overlapped on successive layers could and often did create a substantial interlayer bulk capacitive effect that had a negative impact on circuit timing and performance, and which was not considered by the conventional dummy fill tools at the time even when they considered certain intralayer timing effects. *See* Ex. A at 1:43–2:6, 4:11–16.

8. Recognizing these drawbacks, as well as the importance of having a flat or planarized surface on the devices, the inventors of the ’760 patent set out to develop a design process that would also consider the interlayer bulk capacitance created by overlapping dummy fill and consider those intralayer effects in arranging dummy fill in the chip layout so as to minimize the unwanted bulk capacitance created by overlapping dummy fill features.

9. The inventors of the ’760 patent ultimately conceived of a method for addressing the interlayer capacitive effects of dummy fill by treating each successive set of layers as a pair and then rearranging the dummy fill in one or both layers so as to minimize their overlap. This was particularly advantageous in “intelligent dummy fill placement,” i.e., when timing impact is considered when placing dummy fill. *See* Ex. A at 2:10–19.

10. The inventions disclosed in the ’760 patent provide many advantages over the prior art. In particular, rearranging the dummy fill features such that they do not align vertically in successive layers can reduce unwanted bulk capacitance introduced by dummy fill and thus minimize the interlayer capacitance. *See* Ex. A at 2:45–48, 2:47–59, 3:30–33, 5:19–39. This removed unwanted bulk capacitance that would otherwise slow down signals in the circuit and adversely affect timing in the IC, thus improving its speed and performance. *See* Ex. A at 2:3–6. These significant advantages are achieved through the use of the patented inventions and thus

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the ’760 patent presents significant commercial value for companies like Lattice.

11. Bell Semic brings this action to put a stop to Lattice’s unauthorized and unlicensed use of the inventions claimed in the ’760 patent.

THE PARTIES

12. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

13. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America’s greatest technology incubators. Bell Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

14. Bell Semic, a successor to Bell Labs’ pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor–related inventions was developed over many years by some of the world’s leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation (“LSI”). This portfolio reflects technology that underlies many important innovations in the development of semiconductors and integrated circuits for high–tech products, including smartphones,

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computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

15. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since those early days at Bell Labs. For example, Bell Semic's CTO was a LSI Fellow and Broadcom Fellow. He is known throughout the world as an innovator with more than 300 patents to his name, and he has a sterling reputation for helping semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from the semiconductor world to work with Nortel Networks in the telecom industry during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees and employees. In addition, several Bell Semic executives previously served as engineers at many of these companies and were personally involved in creating the ideas claimed throughout Bell Semic's extensive patent portfolio.

16. On information and belief, Lattice is an Oregon company with its principal place of business and headquarters at 5555 NE Moore Ct, Hillsboro, OR 97124.

17. On information and belief, Lattice develops, designs, and/or manufactures products in the United States, including in this District, according to the '760 patented processes/methodologies; and/or uses the '760 patented processes/methodologies in the United States, including in this District, to make products; and/or distributes, markets, sells, or offers to sell in the United States and/or imports products into the United States, including in this District, that were manufactured or otherwise produced using the patented process. Additionally, Lattice introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

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JURISDICTION AND VENUE

18. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

19. This Court has personal jurisdiction over Lattice under the laws of the State of Oregon, due at least to its substantial business in Oregon and in this District. Lattice has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of Oregon, and in this District by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of Oregon and in this District, Lattice, directly or through intermediaries: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the '760 patented process/methodology; (iii) distributes, markets, sells, or offers to sell products formed according to the '760 patented process/methodology; and/or (iv) imports products formed according to the '760 patented process/methodology.

20. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because Lattice has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, Lattice maintains a regular and established place of business at its corporate headquarters, which is located in the District at 5555 NE Moore Ct, Hillsboro, OR 97124. *See About Us*, Lattice Semiconductor (available at https://www.latticesemi.com/About) (last visited September 20, 2022).

21. On information and belief, Lattice employs more than 80 engineers in the State of

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Oregon. *See* Search Results for Current Lattice Employees, LinkedIn (available at https://www.linkedin.com/search/results/people/?currentCompany=%5B%226994%22%5D&geoUrn=%5B%22101685541%22%5D&keywords=engineer&origin=FACETED_SEARCH&sid=POi) (last visited October 13, 2022). In addition, Lattice is advertising 21 jobs in the Portland area, including product development and engineering positions. These positions include those that relate to the '760 patented technology, including Product Engineer, Product Test Engineering Manager, and Senior Reliability Engineer. *See Lattice Semiconductor Careers*, Lattice (https://recruiting2.ultipro.com/LAT1001LATT/JobBoard/e7f50c7c-43f9-46e9-86ed-b31eaa369842/?q=&o=postedDateDesc&f4=shWMTo1HzVuSJsTCE90ghw) (last visited October 12, 2022).

22. Venue is also convenient in this District. This is at least true because of this District's close ties to this case—including the technology, relevant witnesses, and sources of proof noted above—and its ability to quickly and efficiently move this case to resolution.

23. On information and belief, Bell Semic's causes of action arise directly from Lattice's circuit design work and other activities in this District. Moreover, on information and belief, Lattice has derived substantial revenues from its infringing acts occurring within the State of Oregon and within this District.

U.S. PATENT NO. 7,396,760

24. Bell Semic is the owner by assignment of the '760 patent. The '760 patent is titled "Method and System for Reducing Inter-Layer Capacitance in Integrated Circuits."

25. A true and correct copy of the '760 patent is attached as Exhibit A.

26. The inventors of the '760 patent are Kunal Taravade, Neal Callan, and Paul Filseth.

27. The '760 patent issued on July 8, 2008 from an application filed on November 17,

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2004.

28. The ’760 patent generally relates to “a method for reducing inter-layer capacitance” in integrated circuits “through dummy fill methodology.” Ex. A at 1:8–10.

29. The background section of the ’760 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior dummy fill methodologies were disadvantageous because they typically focused on achieving uniformity of feature density and failed to sufficiently address adverse effects of the dummy fill on electric field and unwanted bulk capacitance. *See* Ex. A at 1:62–66. In addition, these dummy fill methodologies only considered intralayer effects of dummy fill, to the extent that they considered timing impact at all. *See* Ex. A at 1:66–2:3. Thus, placement of dummy fill, even if advantageous on each individual layer, could create problems when it overlapped with dummy fill features on successive layers, introducing an additional bulk capacitance component that could be substantial. *See id.* at 4:11–17, 4:25–28. These methodologies failed to consider interlayer effects such as those caused by the overlap of dummy fill features in successive layers, which could have a substantial negative impact on timing. *See id.* at 2:3–6.

30. In light of the drawbacks of the prior art, the inventors of the ’760 patent recognized a need for “intelligent dummy fill placement to reduce interlayer capacitance caused by overlaps of dummy fill area on successive layers,” which would also “treat[] each consecutive pair of layers together when the intelligent dummy filling placement is performed.” Ex. A at 2:7–13. The inventions claimed in the ’760 patent address this need.

31. The ’760 patent contains two independent claims and 19 total claims. Claim 1 reads:

> 1. A method for placing dummy fill patterns in an integrated circuit fabrication process, comprising:

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> obtaining layout information of the integrated circuit, the integrated circuit including a plurality of layers;
>
> obtaining a first dummy fill space for a first layer based on the layout information;
>
> obtaining a second dummy fill space for a second layer, the second layer being placed successively to the first layer;
>
> determining an overlap between the first dummy fill space and the second dummy fill space; and
>
> minimizing the overlap by re-arranging a plurality of first dummy fill features and a plurality of second dummy fill features,
>
> wherein the first dummy fill space includes non-signal carrying lines on the first layer and the second dummy fill space includes non-signal carrying lines on the second layer.

32. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.,* minimizing interlayer bulk capacitance and thus improving the timing characteristics and performance of the IC while meeting interconnect density requirements during processing. *See, e.g.*, Ex. A at 1:37–55, 5:19–39.

33. The claims of the ’760 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to dummy filling. The claims of the ’760 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the ’760 patent specification, the claimed inventions improve upon the prior art processes by considering successive layers rather than each layer on its own, and then determining the overlap between dummy fill features on successive layers before rearranging them to minimize their overlap and thus reduce interlayer bulk capacitance. This has advantages such as minimizing the parasitic capacitance of the interconnect layers, especially the bulk capacitance contributed by the interlayer effects of overlapping dummy fill features, while maintaining necessary interconnect density to meet fabrication

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requirements.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,396,760

34. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

35. The ’760 patent is valid and enforceable under the United States Patent Laws.

36. Bell Semic owns, by assignment, all right, title, and interest in and to the ’760 patent, including the right to collect for past damages.

37. A copy of the ’760 patent is attached at Exhibit A.

38. On information and belief, Lattice has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’760 patent by using the patented methodology to design one or more semiconductor devices, including as one example the LCMX02-7000HC, in the United States.

39. On information and belief, Lattice employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to rearrange dummy fill to minimize its overlap in successive layers (the “Accused Processes”) as recited in the ’760 patent claims. As one example, Lattice’s Accused Processes allow arrangement and rearrangement of dummy fill in a timing aware fashion, including with the ability to stagger the dummy fill in successive layers so as to minimize the interlayer bulk capacitance after determining their overlap as required by claim 1 of the ’760 patent. Lattice does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, rearrange the dummy fill features in successive layers of its LCMX02-7000HC.

40. Lattice’s Accused Processes also form the dummy fill features in a grid within one or more of the successive layers, provide square-shaped dummy fill features in one or more of

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the successive layers, determine the dummy fill space based on a local pattern density in one or more of the successive layers, and minimize total bulk capacitance and/or certain of its components. Lattice does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to implement dummy fill functionality in a timing-aware fashion and with consideration of interlayer capacitive effects in creation and design of its LCMX02-7000HC.

41. An exemplary infringement analysis showing infringement of one or more claims of the ’760 patent is set forth in Exhibit B. The declaration of Dhaval Brahmbhatt, an expert in the field of semiconductor device design, is attached at Exhibit C and further describes Lattice’s infringement of the ’760 patent.

42. Lattice’s Accused Processes infringe and continue to infringe one or more claims of the ’760 patent during the pendency of the ’760 patent.

43. On information and belief, Lattice has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the ’760 patent. Lattice has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly or indirectly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the ’760 patent.

44. Lattice’s infringement of the ’760 patent is exceptional and entitles Bell Semic to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

45. Bell Semic has been damaged by Lattice’s infringement of the ’760 patent and will continue to be damaged unless Lattice is enjoined by this Court. Bell Semic has suffered and

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continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

46. Bell Semic is entitled to recover from Lattice all damages that Bell Semic has sustained as a result of Lattice's infringement of the '760 patent, including without limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

(a) a judgment declaring that Lattice has infringed one or more claims of the '760 patent in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;

(b) an award of damages adequate to compensate Bell Semic for infringement of the '760 patent by Lattice, in an amount to be proven at trial, including supplemental post-verdict damages until such time as Lattice ceases its infringing conduct;

(c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting Lattice and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with Lattice, from committing further acts of infringement;

(d) a judgment requiring Lattice to make an accounting of damages resulting from Lattice's infringement of the '760 patent;

(e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;

(f) pre-judgment and post-judgment interest at the maximum amount permitted by law;

(g) all other relief, in law or equity, to which Bell Semic is entitled.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

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Dated: October 13, 2022

/s/ Jeff S. Pitzer

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Attorneys for Plaintiff Bell Semiconductor, LLC

EXHIBIT A

US007396760B2

(12) **United States Patent**
Taravade et al.

(10) **Patent No.: US 7,396,760 B2**
(45) **Date of Patent: Jul. 8, 2008**

(54) **METHOD AND SYSTEM FOR REDUCING INTER-LAYER CAPACITANCE IN INTEGRATED CIRCUITS**

(75) Inventors: **Kunal N. Taravade**, Portland, OR (US); **Neal Callan**, Lake Oswego, OR (US); **Paul G. Filseth**, Los Gatos, CA (US)

(73) Assignee: **LSI Corporation**, Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 388 days.

(21) Appl. No.: **10/991,107**

(22) Filed: **Nov. 17, 2004**

(65) **Prior Publication Data**

US 2006/0105564 A1 May 18, 2006

(51) **Int. Cl.**
H01L 21/4763 (2006.01)

(52) **U.S. Cl.** **438/626**; 438/622; 438/12; 438/17

(58) **Field of Classification Search** 438/10, 438/12, 14, 17, 618, 622, 626, 631, 645
See application file for complete search history.

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Using Smart Dummy Fill and Selective Reverse Etchback for Pattern Density Equalization; Brian Lee, Duane S. Boning, Dale L. Hetherington and David J. Stein; Massachusetts Institute of Technology, Cambridge, MA, Sandia National Laboratories, Albuquerque, NM; Mar. 2000.

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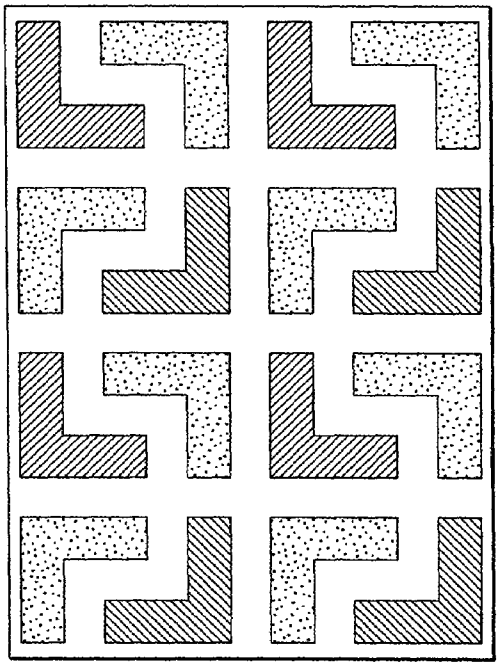
Primary Examiner—Kevin M Picardat
(74) *Attorney, Agent, or Firm*—Suiter Swantz PC LLO

(57) **ABSTRACT**

The present invention is directed to a method and system of intelligent dummy filling placement to reduce inter-layer capacitance caused by overlaps of dummy filling area on successive layers. The method and system treats each consecutive pair of layers together so as to minimize dummy filling overlaps between each layer. In particular, dummy fill features on each layer may be placed in a checkerboard pattern to avoid overlaps. As such, the present invention may eliminate large overlap area of the dummy patterns on consecutive layers by utilizing intelligent dummy filling placement.

19 Claims, 5 Drawing Sheets



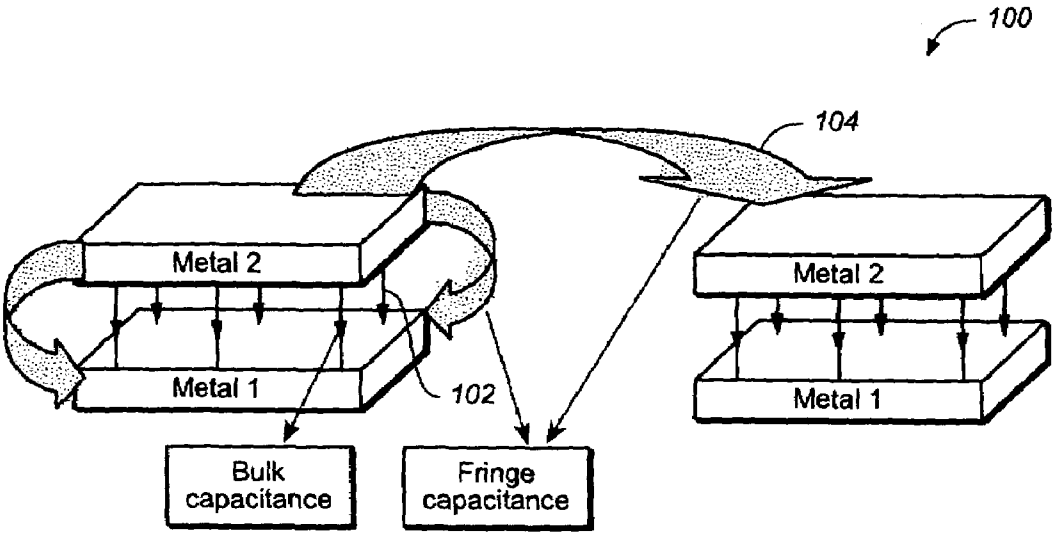

100
104
Metal 2
Metal 1
102
Metal 2
Metal 1
Bulk capacitance
Fringe capacitance

FIG._1

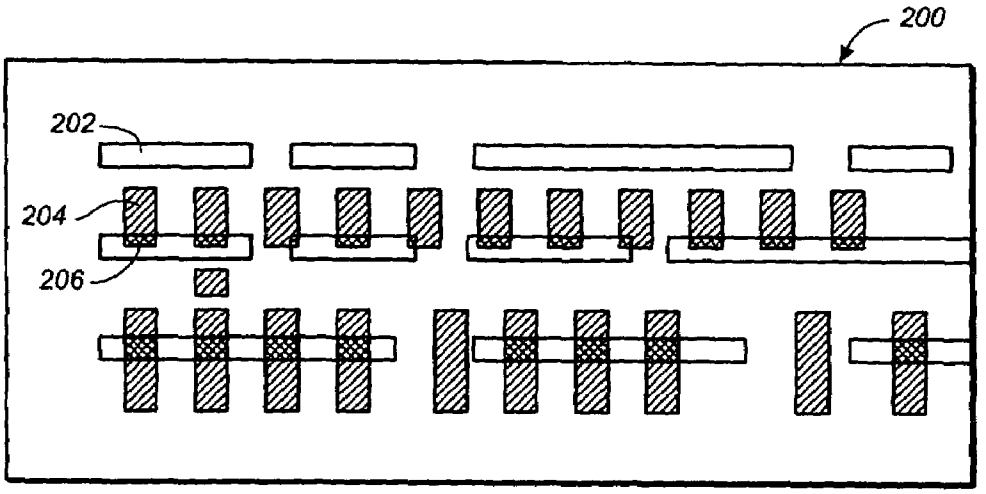

200
202
204
206

FIG._2

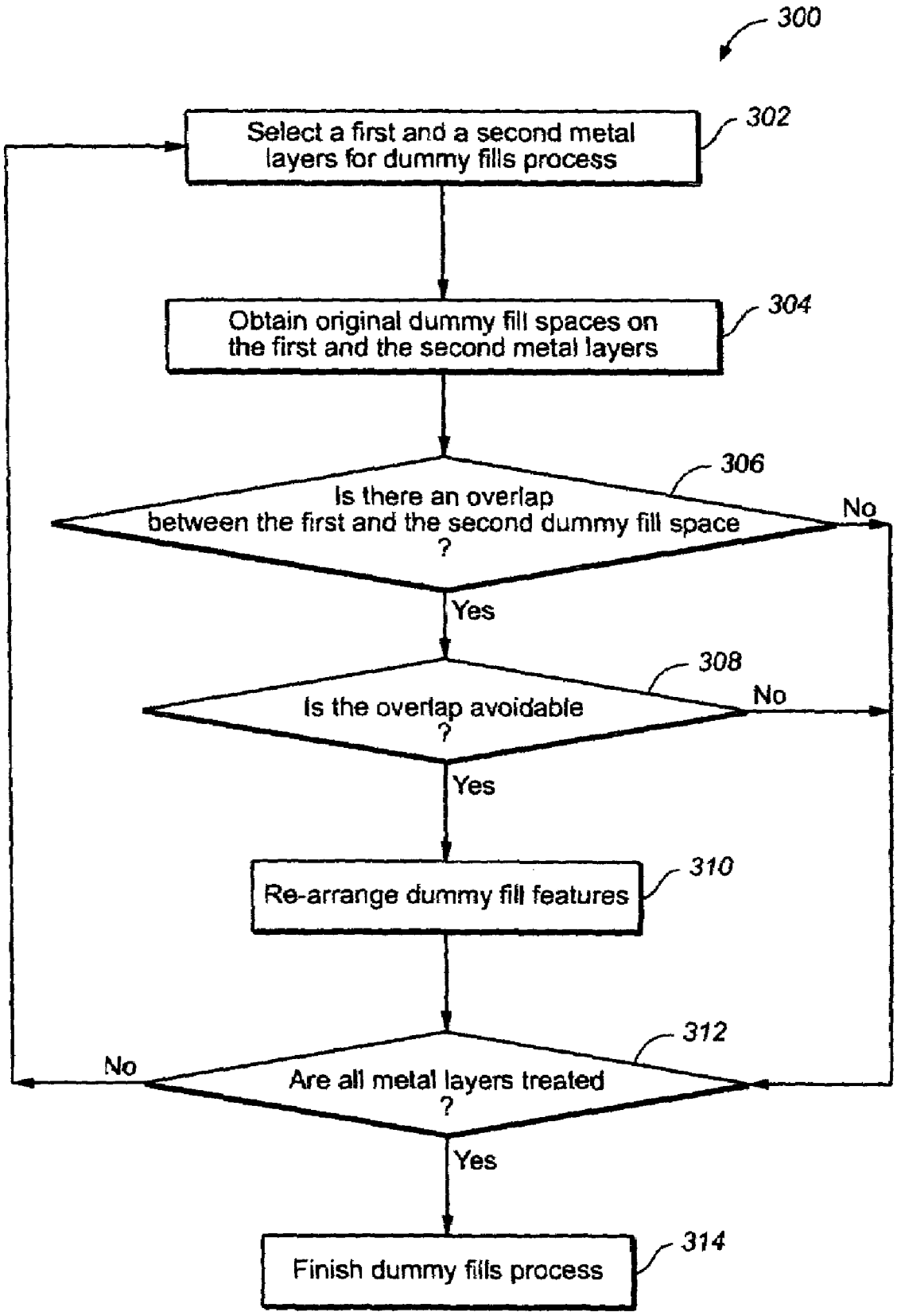

300
Select a first and a second metal layers for dummy fills process
302
Obtain original dummy fill spaces on the first and the second metal layers
304
Is there an overlap between the first and the second dummy fill space ?
306
No
Yes
Is the overlap avoidable ?
308
No
Yes
Re-arrange dummy fill features
310
Are all metal layers treated ?
312
No
Yes
Finish dummy fills process
314

FIG._3

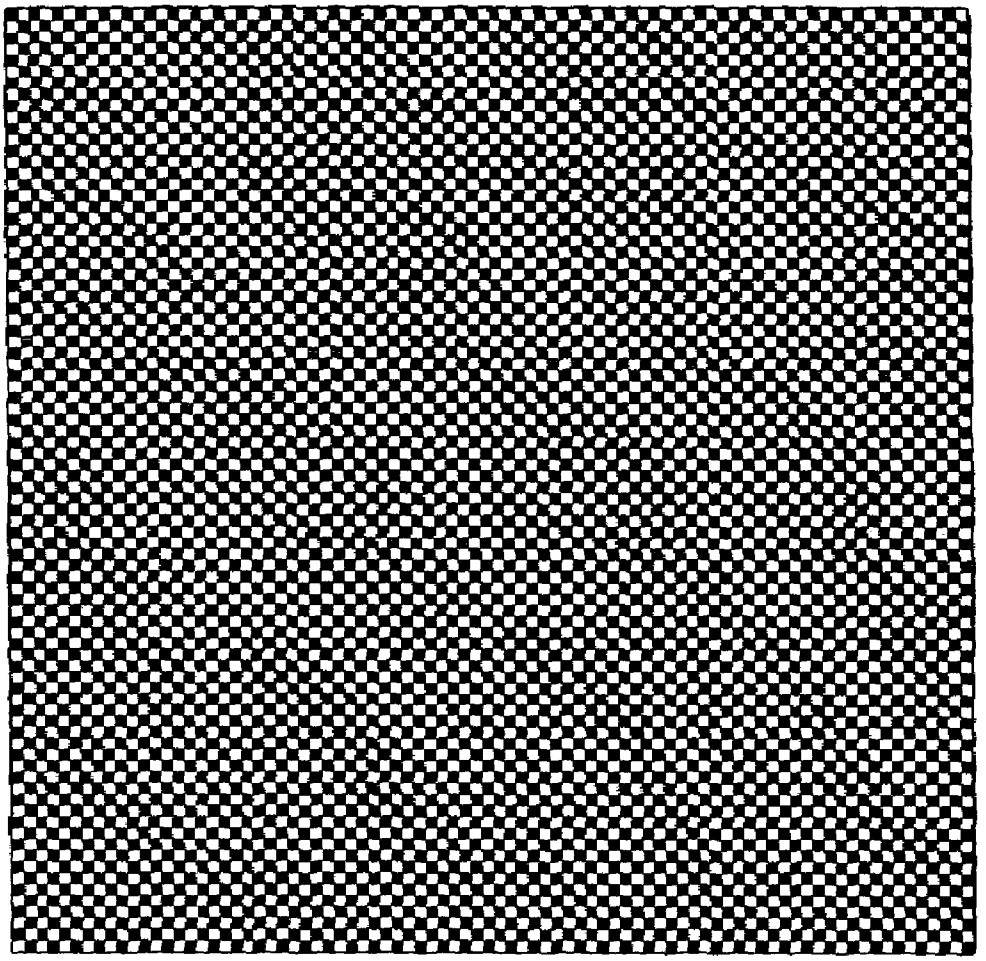


FIG._4

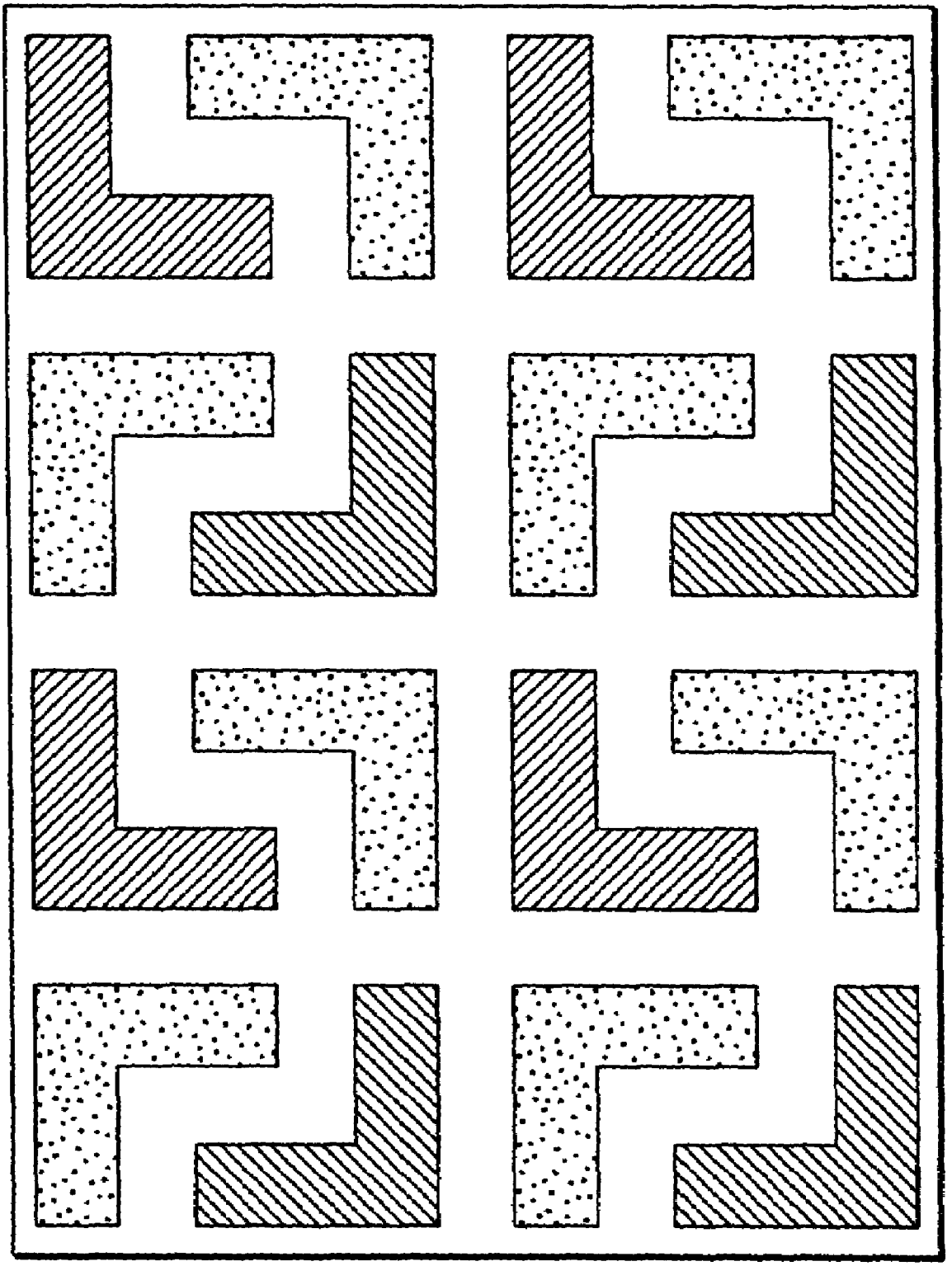


FIG._5

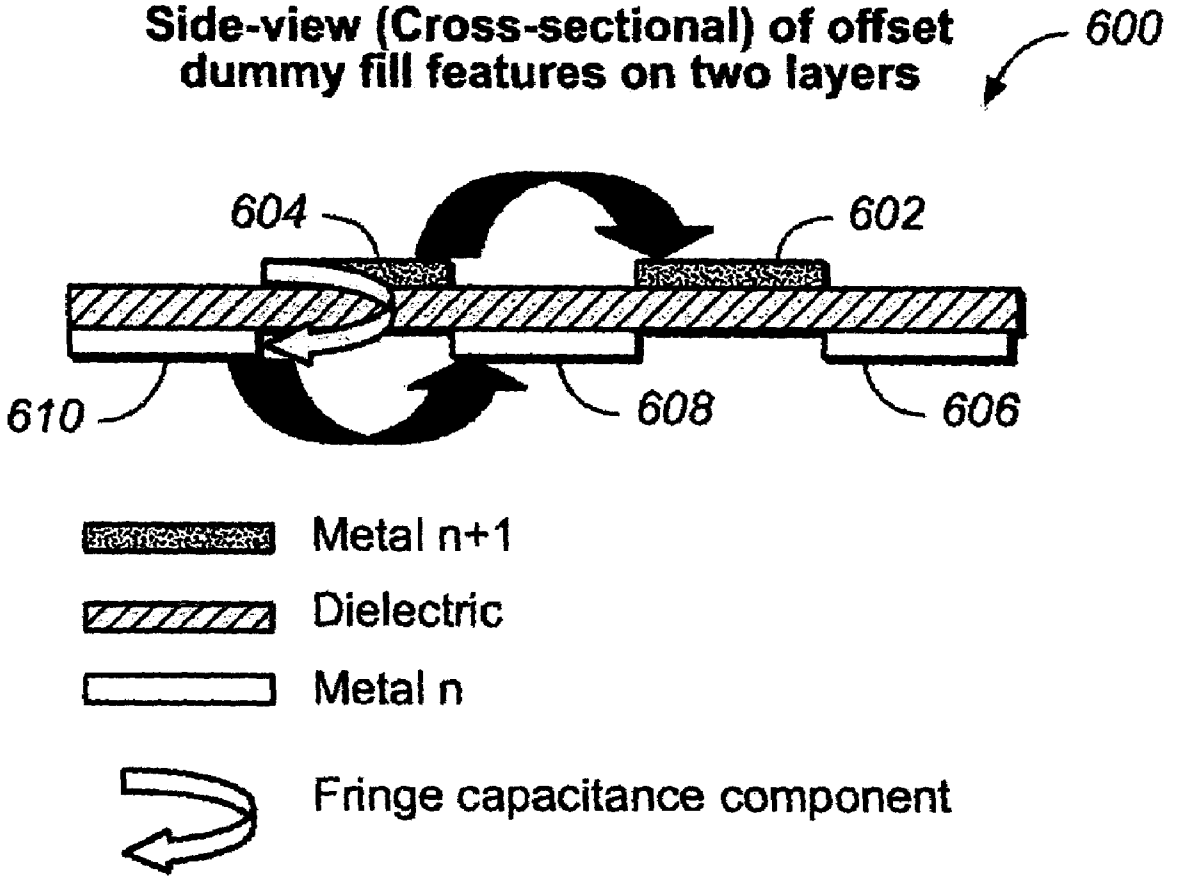

Side-view (Cross-sectional) of offset dummy fill features on two layers
600
604
602
610
608
606
Metal n+1
Dielectric
Metal n
Fringe capacitance component

FIG._6

METHOD AND SYSTEM FOR REDUCING INTER-LAYER CAPACITANCE IN INTEGRATED CIRCUITS

FIELD OF THE INVENTION

The present invention generally relates to the field of integrated circuit fabrication, and particularly to a method for reducing inter-layer capacitance through dummy fill methodology.

BACKGROUND OF THE INVENTION

In any integrated circuit, there is an inevitable capacitance that is introduced from electromagnetic interaction between electrical conductors, such as interconnect layers (metals). There are two components of such capacitance, a bulk (area) component and a fringe (peripheral) component. The bulk component is proportional to the overlap area of interconnect layers and the fringe component depends on the separation and the perimeter of adjacent interconnect layers. Referring now to FIG. **1**, the bulk capacitance **102** and the fringe capacitance **104** between Metal **1** and Metal **2** of an exemplary integrated circuit **100** are shown. The bulk capacitance generated due to the overlap of signal carrying lines on Metal **1** and Metal **2** may not be easily avoided since the placement of signal carrying lines is dictated by circuit functionality. However, the bulk capacitance introduced due to the overlap of non-signal carry lines may be reduced by changing the placement of non-signal carry lines.

An example of non-signal carry lines includes "dummy" fills which are utilized to even the topography and pattern density across the chip, prevent etch, or the like. "Dummy" fills refer to additional features to an integrated chip layout. In a typical integrated chip layout, there are unused areas on a layer after the signal, power and clock segments have been routed. These unused areas can be large enough such that additional features (metals) should be added to satisfy minimum metal coverage requirements for manufacturing. The "dummy" fills may be added to the unused areas such that subsequent layers on the integrated circuit are substantially planar.

For example, a dummy fills methodology is utilized in chemical mechanical polishing or planarization (CMP) process. Often, the planer profile resulting from the CMP process is dependent on the pattern density of the underlying layer. The density may vary and thus result in CMP planer profile variation. Such CMP planer profile variation may be reduced by employing the dummy fills methodology. In particular, dummy fills (dummy features) are inserted into a wafer prior to the CMP process so as to make the pattern density more uniform in IC chips. Uniform feature density improves wafer-processing uniformity for certain operations such as CMP. Dummy fills are typically placed according to conventional dummy fills methodologies that locate dummy fills where space is available. However, the conventional dummy fills methodologies allow a large planer profile variation. Some sophisticated dummy fills methodologies are utilized to reduce the large planer profile variation by selectively inserting dummy fills to achieve an effective density to within a predetermined range.

While most dummy fills methodologies have focused on uniform feature density, the problems created by the inserted dummy fills such as adverse effects on the electric field, unwanted bulk capacitance, and the like have not been addressed. Further, the existing dummy fill methodologies treat each layer independently which results in a large overlap over dummy fill areas on successive layers. Referring now to FIG. **2**, the overlaps **206** between Metal **1** dummy fill area **202** and Metal **2** dummy fill area **204** are shown. If the overlaps **206** are large, the unwanted bulk capacitance may be increased, thereby slowing down signals in the circuit and adversely affecting timing.

Therefore, it would be desirable to provide a method and system of intelligent dummy fill placement to reduce inter-layer capacitance caused by overlaps of dummy fill area on successive layers. It would be also desirable to provide a method and system for treating each consecutive pair of layers together when the intelligent dummy filling placement is performed.

SUMMARY OF THE INVENTION

Accordingly, the present invention provides a method and system for reducing inter-layer capacitance utilizing an intelligent dummy filling placement in integrated circuits.

In a first aspect of the present invention, a system for locating dummy fill features in an integrated circuit fabrication process is provided. The system may comprise an input for obtaining circuit layout information which provides initial signal lines on layers of the integrated circuit. The system may treat each successive pair of layers (a first layer and a second layer) together. The system may comprise a means for defining dummy fill features including small squares within the dummy fill space. The dummy fill spaces are suitable to have dummy fill features inserted. The dummy fill spaces may include areas where dummy patterns are intended to be placed on the first layer and the second layer. Then, the system may assign alternating dummy fill features to each layer in order to avoid overlaps between dummy fill features on each layer.

In a second aspect of the present invention, a method of placing dummy fill patterns to minimize inter-layer capacitance in an integrated circuit fabrication process is provided. The integrated circuit may include many interconnect layers (metals). The method may treat each consecutive pair of layers (a first layer and a second layer) together. Layout information of the integrated circuit may be obtained to determine an initial dummy fill space for a first layer and a second layer. Whether there are overlaps between the initial dummy fill space on the first layer and the initial dummy fill space on the second dummy fill space may be determined. If the overlaps are found and avoidable by re-arranging dummy fill patterns, a first dummy fill pattern and a second dummy fill pattern may be re-arranged to minimize the overlaps.

Additionally, the first dummy fill pattern may be placed to form a checkerboard pattern. If the first layer is already arranged in the form of a checkerboard pattern, the first dummy fill pattern may not be re-arranged. Then, the second dummy fill pattern may be placed to form a checkerboard pattern so as to be offset from the first dummy fill pattern. In this manner, each of the dummy fill features on the first layer may not be placed directly above dummy fill features on the second layer. Consequently, the unwanted bulk capacitance introduce by the dummy fill may be reduced and thus the inter-layer capacitance is minimized.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention as claimed. The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention and together with the general description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The numerous advantages of the present invention may be better understood by those skilled in the art by reference to the accompanying figures in which:

FIG. **1** is an illustration of fringe and bulk capacitance components in an exemplary integrated circuit having Metal **1** and Metal **2** layers;

FIG. **2** is an illustration of layout image showing overlaps of dummy fill areas of Metal **1** and Metal **2** layers in FIG. **1**;

FIG. **3** is a flow diagram illustrating a method implemented in accordance with an exemplary embodiment of the present invention wherein two consecutive layers are treated;

FIG. **4** is a top view of a layer showing a checkerboard pattern formed by the method described in FIG. **3**;

FIG. **5** is a top view of two layers showing an alternative pattern with which the present invention can be embodied; and

FIG. **6** is a cross-sectional view of two layers showing offset dummy fill features inserted by the method described in FIG. **3**.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the presently preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

Referring generally now to FIGS. **3** through **5**, exemplary embodiments of the present invention are shown.

The present invention is directed to a method and system of intelligent dummy filling placement to reduce inter-layer capacitance caused by overlaps of dummy fills on successive layers. Generally, dummy fill refers to the addition of features to a layout for the purpose of raising the density of specific regions on the layout of the integrated circuit. The method and system treats each consecutive pair of layers together so as to minimize the overlaps of dummy fills between each layer. In particular, dummy fill features on each layer may be placed in a checkerboard pattern to avoid overlaps. As such, the present invention may eliminate large overlap areas of the dummy fills on consecutive layers by utilizing intelligent dummy fill placement. In the following description, numerous specific descriptions are set forth in order to provide a thorough understanding of the present invention. It should be appreciated by those skilled in the art that the present invention may be practiced without some or all of these specific details. In some instances, well known process operations have not been described in detail in order to prevent obscurity of the present invention.

Referring now to FIG. **3**, a flow diagram **300** illustrating a method implemented in accordance with an exemplary embodiment of the present invention wherein a dummy fill process is performed on each layer of an integrated circuit is shown. Generally, an integrated circuit fabrication process involves a series of layering processes in which metallization, dielectrics, and other materials are applied to the surface of a semiconductor wafer to form a layered interconnected structure (an interconnect layer). The integrated circuits generally include inter-layered circuits comprising a plurality of metal lines across multiple layers that are interconnected by metal-filled vias. The method begins in step **302** in which a first layer and a second layer are selected for dummy fill process. The first layer and the second layer are a consecutive pair of layers of the IC.

Generally, dummy fills are utilized to improve planer profile uniformity by helping to level the feature density across the layout during an integrated circuit fabrication process. For example, dummy fills are utilized in chemical mechanical polishing or planarization (CMP) process. Often, the planer profile resulting from the CMP process is dependent on the pattern density of the underlying layer. The dependency may vary and thus offset the CMP planer profile variation. Such variation may be reduced by employing the dummy fills methodology. In particular, dummy fills (dummy features) are inserted into a wafer prior to the CMP process so as to make the pattern density more uniform in IC chips. Uniform feature density improves wafer-processing uniformity for certain operations such as CMP. Placement of the dummy fills is typically made according to conventional dummy fill methodologies that locate the uniform-densities dummy where space is available. However, the inserted dummy fills may create problems such as adverse effects on the electric field, unwanted bulk capacitance, and the like.

In Step **304**, the original (initial) dummy fill spaces of the first layer and the second layer may be obtained based on layout information. The layout information may be provided by a user, an IC fabrication process system, a CAD tool, or the like. The original dummy fill space may include areas where dummy fill patterns are intended to be placed on layers. Then, in Step **306**, whether there is any overlap between the original dummy fill space of the first layer and the original dummy fill space of the second layer may be determined. The overlaps of dummy fill areas between the first layer and the second layer are undesirable since the unwanted bulk capacitance may be introduced by the overlaps. Thus, in step **308**, whether the overlap can be avoided by re-arrangement of dummy features may be checked. Then, dummy fill patterns on the first layer and the second layer may be re-arranged to minimize the overlaps in Step **310**. In a particular embodiment of the present invention, a grid (composed of small squares) may be defined within the dummy fill spaces. The method may assign alternating squares (dummy fill features) in the grid to each layer. In this manner, dummy fill features on the first layer are not placed directly above the ones on the second layer but offset from each other. It is to be noted that the dummy fill features may be placed to form various predefined patterns designed to prevent overlaps on adjacent layers. Referring now to FIG. **4**, an exemplary top view of a layer showing a checkerboard pattern formed by the present invention is shown. As shown in FIG. **4**, dummy fill features placed in a checkerboard pattern may avoid overlap, thereby reducing the bulk capacitance component of the total capacitance. Preferably, the dummy fill features are placed to form a checkerboard pattern. Referring now to FIG. **5**, an exemplary top view of two layers showing a different pattern with which the present invention can be embodied is shown.

Referring back to FIG. **3**, if there is no overlap found, the method may proceed to check whether all interconnect layers in the IC have been treated in Step **312**. If all interconnect layers have been treated, the method may finish the dummy fill pattern placement in step **314**. If all interconnect layers have not been treated, the method may proceed to step **302** by selecting the next pair of consecutive layers.

Additionally, the method may check whether the first layer is already arranged in the form of a checkerboard. If the first layer includes dummy fill pattern in the form of a checkerboard, the dummy fill pattern on first layer may not be re-arranged. The dummy fill pattern on the second layer may be re-arranged to form a checked board pattern by offsetting against the dummy fill pattern on the first layer.

One of skill in the art will appreciate that there are various ways to check the form of the dummy fill pattern. In a particular embodiment, numbers may be assigned to dummy features in order to check whether the dummy fill pattern is

already in the form of a checkerboard pattern. For example, a dummy feature may have a row number, a column number, and a layer number. The dummy fill pattern may be checked by implementation of a simple Boolean check as follows: Pattern checking number=row number+column number+layer number. Each dummy feature may have a pattern checking number. The numbering scheme for the simple Boolean check may be assigned such that the pattern checking number is always odd for given row number, column number and layer number. As such, the dummy fill features on the first layer and the second layer are placed on alternating row and column combinations. Additionally, the simple Boolean check may be utilized to determine whether to re-arrange dummy features on the layer.

In FIG. **6**, a cross-sectional view **600** of two layers showing offset dummy fill features inserted by the present invention is shown. The first dummy features **602**, **604** is arranged to offset the second dummy features **606-610**. The checkerboard style layout of the dummy fill pattern prevents situations in which dummy patterns on successive layers overlap, thereby increasing parasitic capacitance of the circuit by adding bulk (area) capacitance of the chip in proportion to the overlap area of the dummy patterns on consecutive layers. By offsetting the dummy patterns in a checkerboard fashion, the large bulk capacitance component may be eliminated. As a result, the total capacitance for an integrated circuit may be reduced.

Generally, the total capacitance for an integrated circuit composed of interconnect layers (metals) may be given by:

$$C_{TOTAL}=C_{BULK}+C_{FRINGE}$$

where C_{BULK}=Bulk intra-layer capacitance (bulk capacitance of metal lines on the same layer)+Bulk inter-layer Capacitance (bulk capacitance of metal lines on adjacent layers) and C_{FRINGE}=Fringe intra-layer capacitance (fringe capacitance of metal lines on the same layer)+Fringe inter-layer Capacitance (fringe capacitance of metal lines on adjacent layers).

In a particular embodiment of the present invention, the above-described method and system may be implemented through various commercially available polygon manipulation languages. An example of the commercially available polygon manipulation languages may include, but are not limited to, Mentor Graphics® Calibre®, Synopsys® Hercules® or the like.

It should be noted that the method and system of the present invention may be utilized for wafer processing operations such as CMP. However, the method and the system of the present invention may be utilized for any suitable integrated circuit fabrication process.

In the exemplary embodiments, the methods disclosed may be implemented as sets of instructions or software readable by a device. Further, it is understood that the specific order or hierarchy of steps in the methods disclosed are examples of exemplary approaches. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the method can be rearranged while remaining within the scope and spirit of the present invention. The accompanying method claims present elements of the various steps in a sample order, and are not necessarily meant to be limited to the specific order or hierarchy presented.

It is believed that the method and system of the present invention and many of its attendant advantages will be understood by the forgoing description. It is also believed that it will be apparent that various changes may be made in the form, construction and arrangement of the components thereof without departing from the scope and spirit of the invention or without sacrificing all of its material advantages. The form herein before described being merely an explanatory embodiment thereof. It is the intention of the following claims to encompass and include such changes.

What is claimed is:

1. A method for placing dummy fill patterns in an integrated circuit fabrication process, comprising:

obtaining layout information of the integrated circuit, the integrated circuit including a plurality of layers;

obtaining a first dummy fill space for a first layer based on the layout information;

obtaining a second dummy fill space for a second layer, the second layer being placed successively to the first layer;

determining an overlap between the first dummy fill space and the second dummy fill space; and

minimizing the overlap by re-arranging a plurality of first dummy fill features and a plurality of second dummy fill features,

wherein the first dummy fill space includes non-signal carrying lines on the first layer and the second dummy fill space includes non-signal carrying lines on the second layer.

2. The method as described in claim **1**, wherein the plurality of first dummy fill features forms a grid within the first dummy fill space.

3. The method as described in claim **1**, wherein the plurality of second dummy fill features forms a grid within the second dummy fill space.

4. The method as described in claim **1**, wherein the first dummy fill space is determined based on a local pattern density for the first layer.

5. The method as described in claim **1**, wherein the second dummy fill space is determined based on a local pattern density for the second layer.

6. The method as described in claim **2**, wherein the grid includes a plurality of squares.

7. The method as described in claim **1**, the minimizing the overlap step further comprising:

determining whether the plurality of first dummy fill features form a predefined pattern; and

re-arranging the plurality of first dummy fill features to form the predefined pattern if the plurality of first dummy fill features are not arranged in the predefined pattern.

8. The method as described in claim **7**, further comprising:

re-arranging the plurality of second dummy fill features based on the plurality of first dummy features if the plurality of first dummy fill features are already arranged in the predefined pattern.

9. The method as described in claim **8**, wherein the plurality of second dummy fill features are re-arranged so as to be offset from the plurality of first dummy fill features.

10. The method as described in claim **7**, wherein the predefined pattern is a checkerboard pattern.

11. The method as described in claim **1**, wherein a total bulk capacitance is minimized.

12. The method as described in claim **11**, wherein the total bulk capacitance includes a bulk inter-layer capacitance.

13. The method as described in claim **11**, wherein the bulk inter-layer capacitance is a bulk capacitance created by overlaps between the first layer and the second layer.

14. A method of filling dummy patterns for pattern density equalization in an integrated circuit fabrication process, comprising:

obtaining a local density pattern of a first layer, the local density pattern obtained based on an initial layout design of the integrated circuit;

determining a second layer, the second layer being placed successively to the first layer;

obtaining a local density pattern of the second layer, the local density pattern obtained based on the initial layout design of the integrated circuit;

designing a plurality of dummy fill features on the first layer and the second layer, the plurality of dummy fill features being suitable for increasing pattern density in low density spaces on the first layer and the second layer;

determining whether there is an overlap between the plurality of dummy fill features on the first layer and the plurality of dummy fill features on the second layer; and

minimizing the overlap by re-arranging the plurality of dummy fill features on the first layer and the second layer,

wherein a total inter-layer capacitance of the integrated circuit is minimized.

15. The method as described in claim **14**, the minimizing the overlap step further comprising:

determining whether the plurality of first dummy fill feature form a checkerboard pattern; and

placing the plurality of first dummy fill features to form the checkerboard pattern base through a mathematical check if the plurality of first dummy fill features are not a form of the checkerboard pattern,

wherein the mathematical check is applied to numeric values of each of the plurality of first dummy fill features and the numeric values of each of the plurality of first dummy fill features are determined based on the location on the checkerboard pattern.

16. The method as described in claim **14**, further comprising:

placing the plurality of second dummy fill features based on an arrangement of the plurality of first dummy features if the plurality of first dummy fill features form a checkerboard pattern.

17. The method as described in claim **16**, wherein the plurality of second dummy fill features are placed so as to form an alternate checkerboard pattern against the checkerboard pattern of the plurality of first dummy fill features.

18. The method as described in claim **16**, wherein the plurality of second dummy fill features are placed so as to be offset from the plurality of first dummy fill features.

19. The method as described in claim **14**, further comprising:

placing the plurality of second dummy fill features to form the checkerboard pattern base through a mathematical check,

wherein the mathematical check is applied to numeric values of each of the plurality of second dummy fill features and the numeric values of each of the plurality of second dummy fill features are determined based on the location on the checkerboard pattern.

* * * * *

EXHIBIT B

BELL SEMICONDUCTOR LLC'S ANALYSIS OF INFRINGEMENT

U.S. Patent No. 7,396,760

Claims 1–6 & 11–13

Bell Semiconductor ("Bell Semic") provides evidence of infringement of exemplary claims 1–6 & 11–13 of U.S. Patent No. 7,396,760 ("the '760 patent") by the LCMX02-7000HC produced by Lattice Semiconductor Corporation ("Lattice"). In support thereof, Bell Semic provides the following claim charts.

"Accused Products" as used herein refers to the Lattice circuit designs and/or semiconductor products, including at least LCMX02-7000HC, that are made, produced, and/or processed by a design tool, such as a Cadence Design Systems, Inc. ("Cadence"), Synopsys, Inc. ("Synopsys"), and/or Siemens Digital Industries Software (formerly Mentor Graphics) ("Siemens") tool, by rearranging dummy fill features to minimize their overlap when viewed across adjacent layers. On information and belief, these design tools all function similarly with respect to the functionality described herein. For simplicity, the Cadence tool will be the primary tool cited herein to illustrate infringement of the claimed methods. These claim charts demonstrate infringement by comparing each element of the asserted claims to corresponding components, aspects, and/or features of the Accused Products. These claim charts are not intended to constitute an expert report on infringement. These claim charts include information provided by way of example, and not by way of limitation.

The analysis set forth below is based only upon information from publicly available resources regarding the Accused Products, as Lattice and relevant third parties have not yet provided any non-public information. An analysis of non-public technical documentation may assist in further identifying all infringing features and functionality. Accordingly, Bell Semic reserves the right to supplement this infringement analysis once such information is made available to Bell Semic. Furthermore, Bell Semic reserves the right to revise this infringement analysis, as appropriate, upon issuance of a court order construing any terms recited in the asserted claims or as other circumstances so merit.

Bell Semic contends that each element of each claim asserted herein is literally met, and would also be met under the doctrine of equivalents, as there are no substantial differences between the Accused Products and the elements of the patent claims in function, way, and result. Lattice directly infringes the asserted claims of the '760 patent by performing each of the limitations. If Lattice attempts to argue that there is no literal infringement and/or if Lattice attempts to draw any distinction between the claimed functionality and the Accused Products, then Bell Semic reserves the right to rebut the alleged distinction as a matter of literal infringement and/or as to whether any such distinction is substantial under the doctrine of equivalents.

Unless otherwise noted, the cited evidence applies across each of Lattice's products that were made, produced, or processed from a circuit design using windows, including but not limited to LCMX02-7000HC. Bell Semic reserves the right to amend this infringement analysis based on other products made, produced, or processed in the same or similar manner to that identified herein.

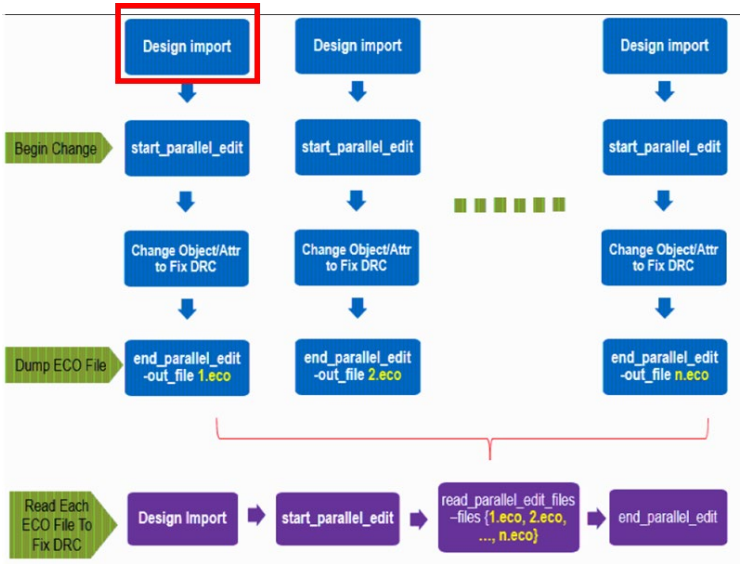
CLAIM CHARTS
Lattice Semiconductor Corporation

Claim 1	Accused Products
1. A method for placing dummy fill patterns in an integrated circuit fabrication process, comprising:	To the extent the preamble is limiting, the Accused Products are produced by performing a method for placing dummy fill patterns in an integrated circuit fabrication process: In layout design, the variation of wiring film thickness caused by the coarseness and denseness of the metal layer can be a bottleneck in the manufacturing process. It is time to consider a novel approach, to chip design that considers metal fill in-design. *See https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/pegasus-tb.pdf, page 1.* The dielectric layers in chip designs often vary in thickness due to the different patterns of metal on successive metal layers. These variations reduce yield and impact chip performance. To minimize these, you can add inactive metal segments, called metal fills, to the open areas of the design. The metal fill makes the topology of the metal layers more uniform, which reduces the variations in metal density. The additional metal increases cross-coupling capacitance, however, so it is important to balance the decrease in thickness variations with the increase in capacitance. • To simplify the estimation of cross-coupling capacitance added by the metal fill, the software adds the metal fill in a staggered pattern. For more information, see Metal Fill Features. • To minimize cross-coupling capacitance within layers, the software adds the metal fill in the timing-aware mode. For more information, see Recommendations for Adding Timing-Aware Metal Fill. *See Innovus User Guide product version 20.10, March 2020, page 705.* For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that places dummy fill patterns in an integrated circuit fabrication process.
obtaining layout information of the integrated circuit, the integrated circuit including a plurality of layers;	The Accused Products are made, produced, or processed from a circuit design that is created by obtaining layout information of the integrated circuit, the integrated circuit including a plurality of layers.

The Innovus® Implementation System (Innovus) software provides the following options for saving, restoring, importing, and exporting design data:

Starting (importing) designs	Allows you to specify data for starting or initializing a design.
Saving designs	Allows you to save the work you complete on designs during a design session for access at a later date.
Restoring designs	Allows you to load saved data from a previous design session.
Loading design data	Allows you to load design data saved in various stages of the design process, and to bring data from specific formats (DEF, PDEF, SPEF, SDF, and OA Cellview) into the Innovus environment.
Saving and exporting design data	Allows you to save design data in various stages of the design process, and to export data in specific formats (DEF, PDEF, GDS, and OASIS) from the Innovus environment.

See Innovus User Guide product version 20.10, March 2020, page 219.



See Innovus User Guide product version 20.10, March 2020, page 1583.

	For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created by loading design information of the integrated circuit. The integrated circuit includes multiple layers.

obtaining a first dummy fill space for a first layer based on the layout information;	The Accused Products are made, produced, or processed from a circuit design that is created by obtaining a first dummy fill space for a first layer based on the layout information.
	
	Achieving Gradient Density with Preferred Density Setting
	
	To prevent density in neighboring regions from varying too much, the `addMetalFill` targets a preferred density. This minimizes the variation in density from window to window. You can set the parameters as follows:
	
	`-minDensity 15 -maxDensity 85 -preferredDensity 35`
	
	`addMetalFill -layer {Metal1 Metal2 Metal3}`
	
	The metal fills are inserted into white space to meet the preferred density. When the metal density in a window is less than the minimum metal fill density value, `addMetalFill` adds metal fill to achieve a density slightly above the preferred density, if possible. If the density is larger than maximum density after it pre-calculates the window density, no metal fills are inserted into the design. The metal fills are inserted based on the preferred density in all windows. This way, the density variation from window to window is minimized.
	
	The `windowStep` parameter can be used to get further global uniformity. With this parameter, the metal densities in the window are calculated and changed by step as shown in the diagram.
	
	See Innovus User Guide product version 20.10, March 2020, page 719 .
	
	For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created by obtaining a metal fill space for a first layer based on the loaded design information.

obtaining a second dummy fill space for a second layer, the second layer being placed successively to the first layer;	The Accused Products are made, produced, or processed from a circuit design that is created by obtaining a second dummy fill space for a second layer placed successively to the first layer.

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Achieving Gradient Density with Preferred Density Setting

To prevent density in neighboring regions from varying too much, the `addMetalFill` targets a preferred density. This minimizes the variation in density from window to window. You can set the parameters as follows:

```
-minDensity 15 -maxDensity 85 -preferredDensity 35

addMetalFill -layer {Metal1 Metal2 Metal3}
```

The metal fills are inserted into white space to meet the preferred density. When the metal density in a window is less than the minimum metal fill density value, `addMetalFill` adds metal fill to achieve a density slightly above the preferred density, if possible. If the density is larger than maximum density after it pre-calculates the window density, no metal fills are inserted into the design. The metal fills are inserted based on the preferred density in all windows. This way, the density variation from window to window is minimized.

The `windowStep` parameter can be used to get further global uniformity. With this parameter, the metal densities in the window are calculated and changed by step as shown in the diagram.

See Innovus User Guide product version 20.10, March 2020, page 719 .

For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created by obtaining a metal fill space for a second layer, where the second layer is placed successively to the first layer.

</td></tr>
<tr><td>determining an overlap between the first dummy fill space and the second dummy fill space; and</td><td>

The Accused Products are made, produced, or processed from a circuit design that is created by determining an overlap between the first dummy fill space and the second dummy fill space.

Staggered Metal Fill Pattern

The staggered metal fill spreads out the effects of cross-coupling capacitance because the staggered pattern ensures that the metal fill does not line up on adjacent layers.This pattern is most effective on lightly congested layers. By default, the software adds a metal fill that is staggered in the preferred routing direction and not staggered in the non-preferred direction. The following figures show staggered and non-staggered patterns for both rectangular and square metal fills.

See Innovus User Guide product version 20.10, March 2020, page 706 .

For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that created by determining overlap between the first and second metal fill spaces. The only way to stagger metal fill is to first determine where there is overlap in metal fill and then to rearrange it to be staggered. *See* Brahmbhatt Decl. at ¶ 75.

</td></tr>
</table>

minimizing the overlap by re-arranging a plurality of first dummy fill features and a plurality of second dummy fill features,	The Accused Products are made, produced, or processed from a circuit design that is created by minimizing the overlap by re-arranging a plurality of first dummy fill features and a plurality of second dummy fill features. The additional metal increases cross-coupling capacitance, however, so it is important to balance the decrease in thickness variations with the increase in capacitance. • To simplify the estimation of cross-coupling capacitance added by the metal fill, the software adds the metal fill in a staggered pattern. For more information, see Metal Fill Features. • To minimize cross-coupling capacitance within layers, the software adds the metal fill in the timing-aware mode. For more information, see Recommendations for Adding Timing-Aware Metal Fill. *See Innovus User Guide product version 20.10, March 2020, page 705 .*

You can generate the metal density report file containing the metal density violation information and view it in the GUI. For this, you need to use the `-report` parameter of the `verifyMetalDensity` command. For example, the content of the metal density report file is:

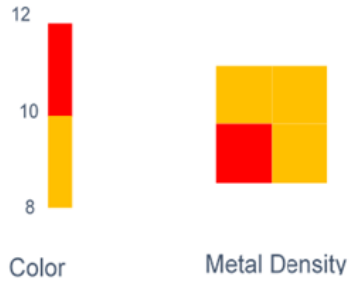
Metal	Density	Window Size
M1	11.14	(0 0) (10 10)
M1	8.96	(0 10) (10 20)
M1	8.96	(10 0) (20 10)
M1	8.96	(10 10) (20 20)

Run the following commands to check the metal density of all layers and view the metal density map in the GUI:

```
verifyMetalDensity -saveToDB
verifyMetalDensity -report reportName.rpt
```

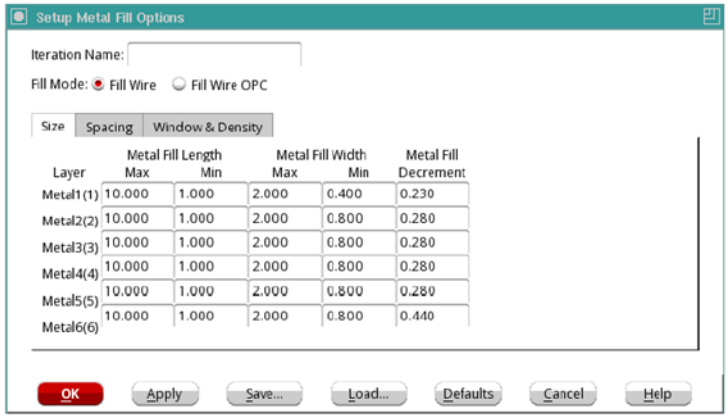
Note: Before running the above commands, you need to set the same values for `setMetalFill -windowSize` and `setMetalFill -windowStep`. Otherwise, the display of metal density is overlapped.

The output of the above commands is:



See Innovus User Guide product version 20.10, March 2020, page 728 .

For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created by minimizing the overlap by re-arranging a plurality of first and second metal fill features to be staggered. Given the near-certainty that ECOs are implemented during the design process, and the layout is altered (and thus, dummy metal fill is repositioned), it is necessary to minimize the resulting overlap between dummy fill features on successive layers. *See* Brahmbhatt Decl. at ¶¶ 71, 74–76.

wherein the first dummy fill space includes non-signal carrying lines on the first layer and the second dummy fill space includes non-signal carrying lines on the second layer.	The Accused Products are made, produced, or processed from a circuit design that is created such that the first dummy fill space includes non-signal carrying lines onf the first layer and the second dummy fill space includes non-signal carrying lines on the second layer. The dielectric layers in chip designs often vary in thickness due to the different patterns of metal on successive metal layers. These variations reduce yield and impact chip performance. To minimize these, you can add inactive metal segments, called metal fills, to the open areas of the design. The metal fill makes the topology of the metal layers more uniform, which reduces the variations in metal density. *See Innovus User Guide product version 20.10, March 2020, page 705 .* **Adding Metal Fill with Iteration** Metal fill can be added iteratively with different parameter settings. You can specify a name for a set of values for `setMetalFill` parameters. `setMetalFill -iterationName file_step1 -layer Metal1 -minDensity 15 -windowSize 100 100 -windowStep 50 50` You can also save the iteration file using GUI. To do so, open the *Setup Metal Fill Options* form, specify the parameters in the form, key in a file name, such as `file_step1` , in the *Iteration Name* text box, and click *OK*.  The window size and step must be the same for all iterations of a specific layer. For example, the following specifications are NOT allowed because the values are not consistent: *See Innovus User Guide product version 20.10, March 2020, page 726 .*

```
setMetalFill -iterationName file_step1 -layer Metal1 -minDensity 15 -windowSize 100 100 -windowStep 50 50
setMetalFill -iterationName file_step2 -layer Metal1 -minDensity 15 -windowSize 50 50 -windowStep 25 25
setMetalFill -iterationName file_step1 file_step2 -layer Metal1
```

If you want to specify different window size and step when adding metal fill, you need to run `addMetalFill` in separate steps. In the following example, the specified values for `-windowSize` and `-windowStep` in *step1*, *step2*, and *step3* are different:

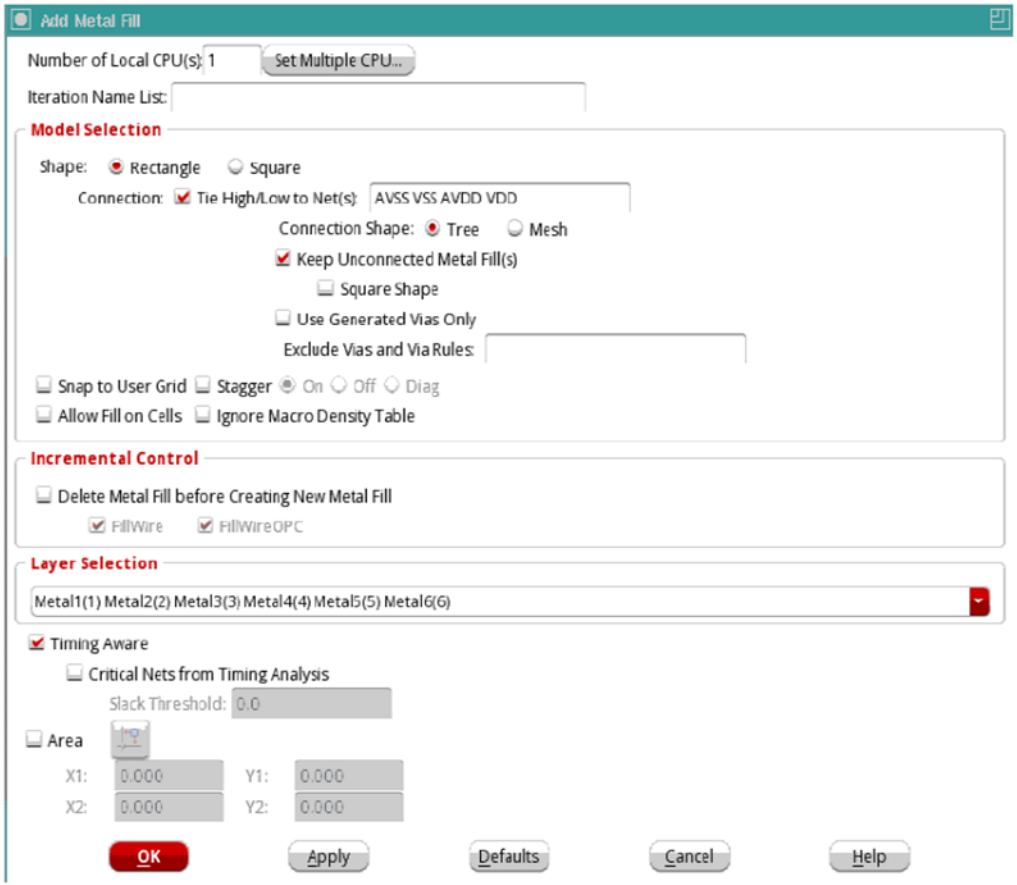
```
setMetalFill -iterationName step1 -layer -windowSize 100 100 -windowStep 50 50
setMetalFill -iterationName step2 -layer -windowSize 100 100 -windowStep 50 50
setMetalFill -iterationName step3 -layer -windowSize 50 50 -windowStep 25 25
```

Here, you can run `addMetalFill` for the first two steps in a single iteration. However, you must run *step3* in a separate iteration because its window size and step values are different from those of *step1* and *step2*. Use `addMetalFill -iterationNameList` to add the metal fill using the stored set of parameters:

```
addMetalFill -iterationNameList {step1 step2} ...
addMetalFill -iterationNameList step3 ...
addMetalFill -layer {Metal1 Metal2 Metal3} -area 0 0 100 100 -nets {VDD VSS} -iterationName step1 step2
```

See Innovus User Guide product version 20.10, March 2020, page 727 .

You can also do the same through the GUI by using the *Route - Metal Fill - Add* command.



Key in the existing file list in *Iteration Name List* text box in the *Add Metal Fill* form and then click *OK*.

The engine processes the iterations in the order listed and stops when the preferred density is reached in any iteration.

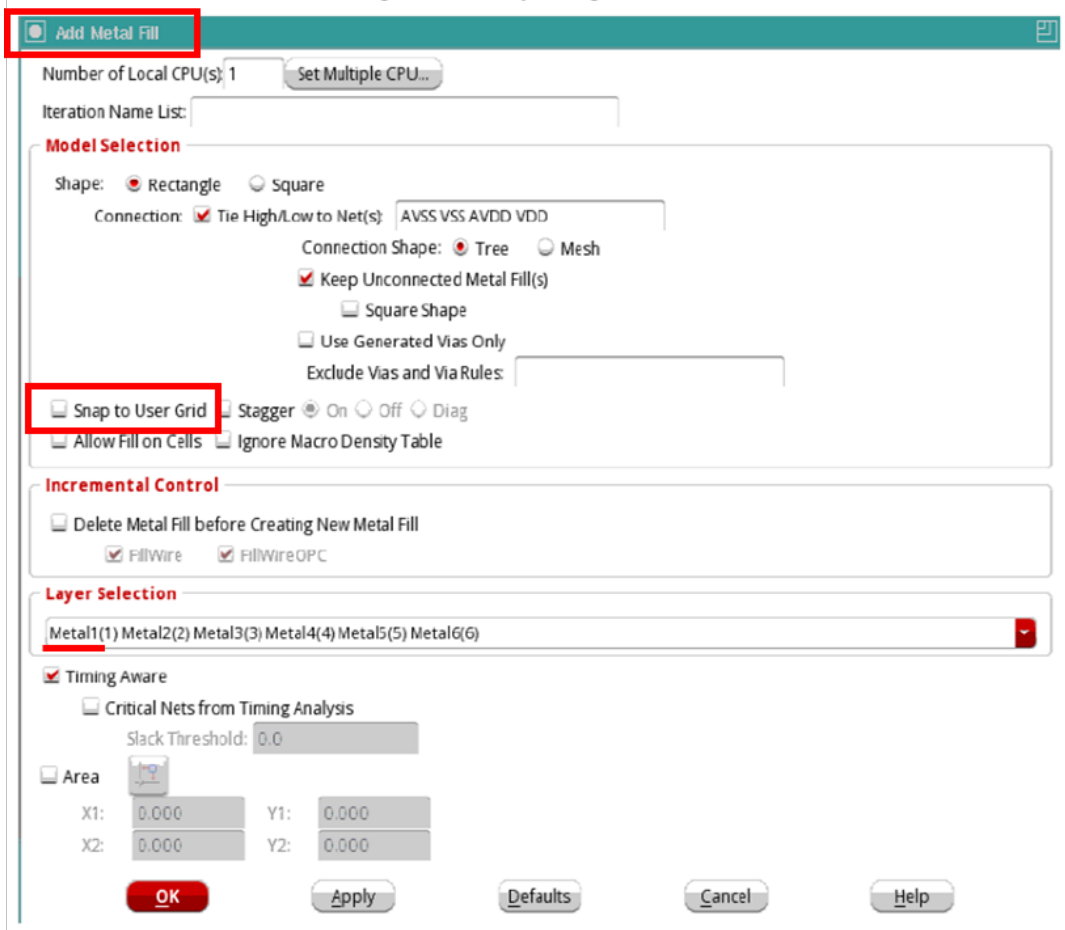
See Innovus User Guide product version 20.10, March 2020, page 727 .

For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created such that the first dummy fill space includes non-signal carrying lines on the first layer and the second dummy fill space includes non-signal carrying lines on the second layer.

CLAIM CHARTS
Lattice Semiconductor Corporation

Claim 2	Accused Products
2. The method as described in claim 1, wherein the plurality of first dummy fill features forms a grid within the first dummy fill space.	The Accused Products are further made, produced, or processed from a circuit design that is created such that the plurality of first dummy fill features forms a grid within the first dummy fill space.

You can also do the same through the GUI by using the *Route - Metal Fill - Add* command.



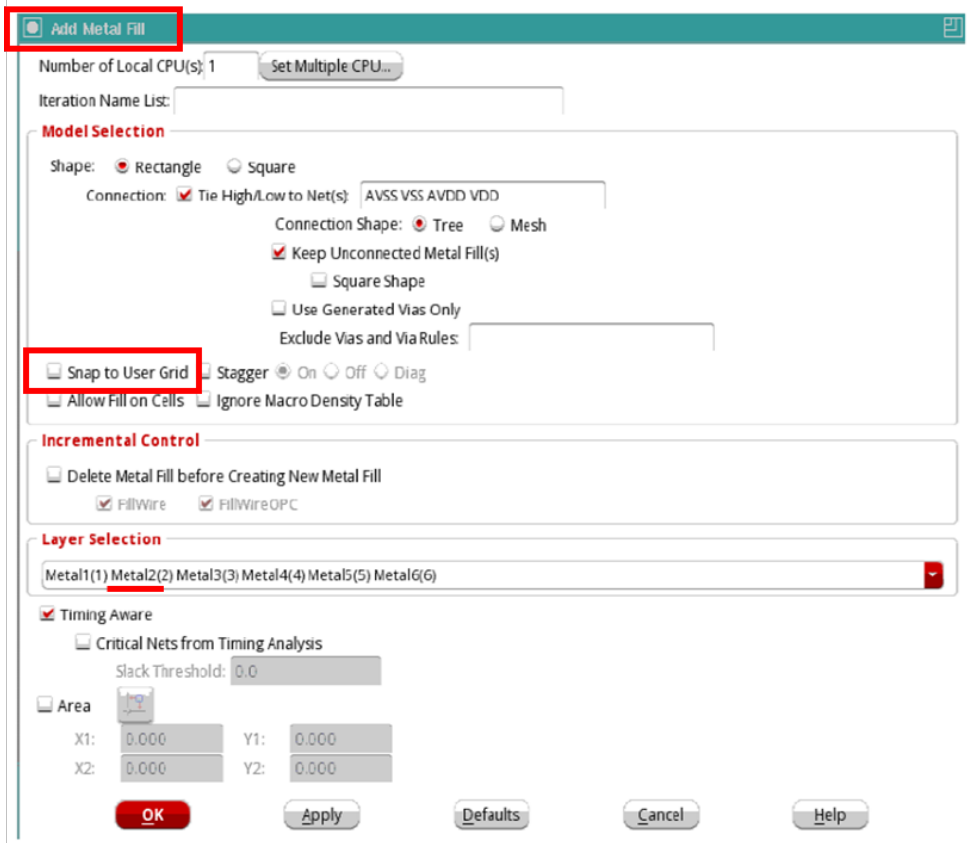
Key in the existing file list in *Iteration Name List* text box in the *Add Metal Fill* form and then click *OK*.

The engine processes the iterations in the order listed and stops when the preferred density is reached in any iteration.

See Innovus User Guide product version 20.10, March 2020, page 727 .

For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created such that the plurality of first dummy fill features forms a grid within the first dummy fill space

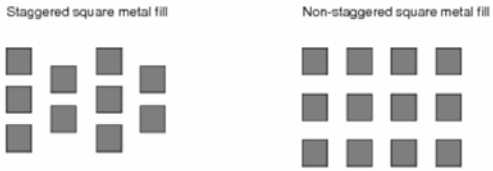
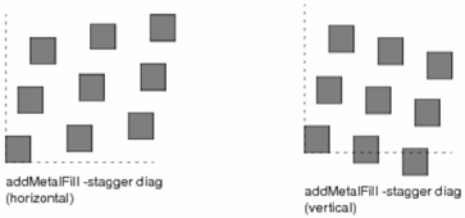
CLAIM CHARTS
Lattice Semiconductor Corporation

Claim 3	Accused Products
3. The method as described in claim 1, wherein the plurality of second dummy fill features forms a grid within the second dummy fill space.	The Accused Products are further made, produced, or processed from a circuit design that is created such that the plurality of second dummy fill features forms a grid within the second dummy fill space. You can also do the same through the GUI by using the *Route - Metal Fill - Add* command.  Key in the existing file list in *Iteration Name List* text box in the *Add Metal Fill* form and then click *OK*. The engine processes the iterations in the order listed and stops when the preferred density is reached in any iteration. *See Innovus User Guide product version 20.10, March 2020, page 727 .*

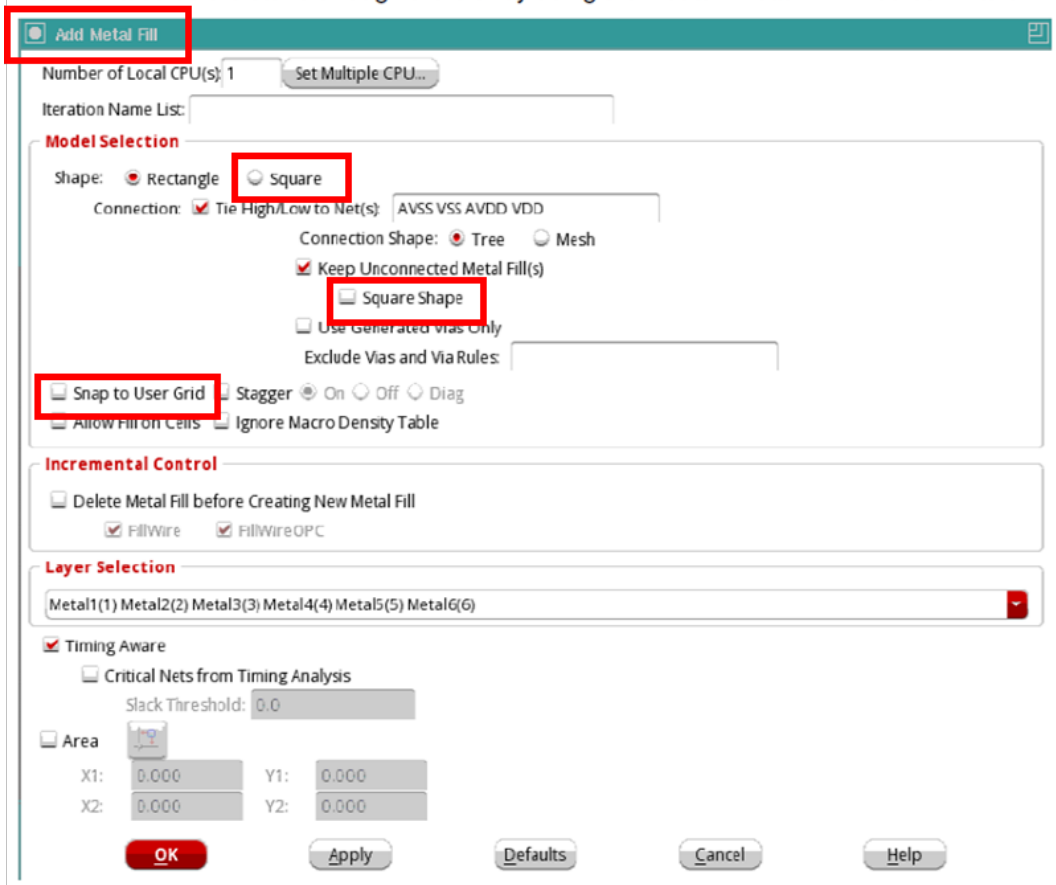
	For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created such that the plurality of second dummy fill features forms a grid within the second dummy fill space.
Claim 4	Accused Products
4. The method as described in claim 1, wherein the first dummy fill space is determined based on a local pattern density for the first layer.	The Accused Products are made, produced, or processed from a circuit design that is created such that the first dummy fill space is determined based on a local pattern density for the first layer. **Adding Metal Fill Using the GUI** 1. Determine the minimum and maximum size for metal fill shapes for each layer, then set these values on the *Size & Spacing* page of the Setup Metal Fill form. ◦ If you are using rectangular metal fill, use the *Rectangle Length* and *Metal Fill Width* values. ◦ If you are using square metal fill, use the *Metal Fill Width* and *Square Decrement* values. 2. Determine the spacing around metal fill shapes for each layer, then set the value on the *Size & Spacing* page of the Setup Metal Fill form. You must set two types of spacing values: ◦ Spacing between a metal fill shape and an active metal shape. An active metal shape can be a signal wire, a power wire, a cell, a pin, or any other structure that is not classified as a fillwire. ◦ Spacing between a metal fill shape and another metal fill shape. 3. Determine the minimum, maximum, preferred, and external metal density for each layer, then set these values on the *Window & Density* page of the Setup Metal Fill form. 4. Use the Verify Metal Density form to create a `Verify Density` report. 5. Locate an area in the design for which metal density is too low, then select that area on the Add Metal Fill form. 6. Determine whether you want metal fill to be square or rectangular, then choose the appropriate value on the Add Metal Fill form. 7. Click *OK* or *Apply* on the Add Metal Fill form to add metal fill shapes to the area that you specified. *See Innovus User Guide product version 20.10, March 2020, page 726 .* For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created such that the first dummy fill space is determined based on a local pattern density for the first layer.

Claim 5	Accused Products
5. The method as described in claim 1, wherein the second dummy fill space is determined based on a local pattern density for the second layer.	The Accused Products are made, produced, or processed from a circuit design that is created such that the second dummy fill space is determined based on a local pattern density for the second layer. **Adding Metal Fill Using the GUI** 1. Determine the minimum and maximum size for metal fill shapes for each layer, then set these values on the *Size & Spacing* page of the Setup Metal Fill form. ◦ If you are using rectangular metal fill, use the *Rectangle Length* and *Metal Fill Width* values. ◦ If you are using square metal fill, use the *Metal Fill Width* and *Square Decrement* values. 2. Determine the spacing around metal fill shapes for each layer, then set the value on the *Size & Spacing* page of the Setup Metal Fill form. You must set two types of spacing values: ◦ Spacing between a metal fill shape and an active metal shape. An active metal shape can be a signal wire, a power wire, a cell, a pin, or any other structure that is not classified as a fillwire. ◦ Spacing between a metal fill shape and another metal fill shape. 3. Determine the minimum, maximum, preferred, and external metal density for each layer, then set these values on the *Window & Density* page of the Setup Metal Fill form. 4. Use the Verify Metal Density form to create a `Verify Density` report. 5. Locate an area in the design for which metal density is too low, then select that area on the Add Metal Fill form. 6. Determine whether you want metal fill to be square or rectangular, then choose the appropriate value on the Add Metal Fill form. 7. Click *OK* or *Apply* on the Add Metal Fill form to add metal fill shapes to the area that you specified. *See Innovus User Guide product version 20.10, March 2020, page 726 .* For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created such that the second dummy fill space is determined based on a local pattern density for the second layer.

CLAIM CHARTS
Lattice Semiconductor Corporation

Claim 6	Accused Products
6. The method as described in claim 2, wherein the grid includes a plurality of squares.	The Accused Products are made, produced, or processed from a circuit design that is created such that the grid includes a plurality of squares. The software uses parameters specified in the LEF file or the fill commands to analyze the density and determine the size and position of the fill. It divides the design into windows and adds metal or cuts to the open areas in each window until the metal and cut densities meet the density requirements.  A metal fill that is staggered in both directions can also be added. This type of metal fill has a diagonal pattern. It is most apparent when it is added to the upper layers where there is not a lot of routing. The following figures show a metal fill that is staggered diagonally:  *See Innovus User Guide product version 20.10, March 2020, pages 705-6.*

You can also do the same through the GUI by using the *Route - Metal Fill - Add* command.



Key in the existing file list in *Iteration Name List* text box in the *Add Metal Fill* form and then click *OK*.

The engine processes the iterations in the order listed and stops when the preferred density is reached in any iteration.

See Innovus User Guide product version 20.10, March 2020, page 727 .

For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that is created such that the grid includes a plurality of squares.

CLAIM CHARTS
Lattice Semiconductor Corporation

Claim 11	Accused Products
11. The method as described in claim 1, wherein a total bulk capacitance is minimized.	The Accused Products are further made, produced, or processed from a circuit design that is created such that a total bulk capacitance is minimized. Bulk capacitance is the area capacitance between the two adjacent metal layers. The dielectric layers in chip designs often vary in thickness due to the different patterns of metal on successive metal layers. These variations reduce yield and impact chip performance. To minimize these, you can add inactive metal segments, called metal fills, to the open areas of the design. The metal fill makes the topology of the metal layers more uniform, which reduces the variations in metal density. The additional metal increases cross-coupling capacitance, however, so it is important to balance the decrease in thickness variations with the increase in capacitance. • To simplify the estimation of cross-coupling capacitance added by the metal fill, the software adds the metal fill in a staggered pattern. For more information, see Metal Fill Features. • To minimize cross-coupling capacitance within layers, the software adds the metal fill in the timing-aware mode. For more information, see Recommendations for Adding Timing-Aware Metal Fill. *See Innovus User Guide product version 20.10, March 2020, page 705.* **Staggered Metal Fill Pattern** The staggered metal fill spreads out the effects of cross-coupling capacitance because the staggered pattern ensures that the metal fill does not line up on adjacent layers.This pattern is most effective on lightly congested layers. By default, the software adds a metal fill that is staggered in the preferred routing direction and not staggered in the non-preferred direction. The following figures show staggered and non-staggered patterns for both rectangular and square metal fills. *See Innovus User Guide product version 20.10, March 2020, page 706 .* Definition of Bulk capacitance from Column 5 of Taravade $C_{TOTAL}=C_{BULK}+C_{FRINGE}$ where C_{BULK}=Bulk intra-layer capacitance (bulk capacitance of metal lines on the same layer)+Bulk inter-layer Capacitance (bulk capacitance of metal lines on adjacent layers) and For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design that minimized total bulk capacitance.

CLAIM CHARTS
Lattice Semiconductor Corporation

Claim 12	Accused Products
12. The method as described in claim 11, wherein the total bulk capacitance includes a bulk inter-layer capacitance.	The Accused Products are further made, produced, or processed from a circuit design that is created such that the total bulk capacitance includes a bulk inter-layer capacitance. Coupling capacitance between signals and dummies of multiple layers The dielectric layers in chip designs often vary in thickness due to the different patterns of metal on successive metal layers. These variations reduce yield and impact chip performance. To minimize these, you can add inactive metal segments, called metal fills, to the open areas of the design. The metal fill makes the topology of the metal layers more uniform, which reduces the variations in metal density. The additional metal increases cross-coupling capacitance, however, so it is important to balance the decrease in thickness variations with the increase in capacitance. • To simplify the estimation of cross-coupling capacitance added by the metal fill, the software adds the metal fill in a staggered pattern. For more information, see Metal Fill Features. • To minimize cross-coupling capacitance within layers, the software adds the metal fill in the timing-aware mode. For more information, see Recommendations for Adding Timing-Aware Metal Fill. *See Innovus User Guide product version 20.10, March 2020, page 705.* Bulk inter-layer capacitance is the bulk capacitance of metal lines on adjacent layers (5:34) For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design in which the minimized total bulk capacitance included a bulk inter-layer capacitance.

CLAIM CHARTS
Lattice Semiconductor Corporation

Claim 13	Accused Products
13. The method as described in claim 11, wherein the bulk inter-layer capacitance is a bulk capacitance created by overlaps between the first layer and the second layer.	The Accused Products are further made, produced, or processed from a circuit design that is created such that the bulk inter-layer capacitance is a bulk capacitance created by overlaps between the first layer and the second layer. **Staggered Metal Fill Pattern** The staggered metal fill spreads out the effects of cross-coupling capacitance because the staggered pattern ensures that the metal fill does not line up on adjacent layers.This pattern is most effective on lightly congested layers. By default, the software adds a metal fill that is staggered in the preferred routing direction and not staggered in the non-preferred direction. The following figures show staggered and non-staggered patterns for both rectangular and square metal fills. *See Innovus User Guide product version 20.10, March 2020, page 706 .* For example, Lattice creates a circuit design for the LCMX02-7000HC, which was made, produced, or processed from a circuit design in which the bulk inter-layer capacitance is created by overlaps between the first layer and the second layer.

Caveat: The notes and/or cited excerpts utilized herein are set forth for illustrative purposes only and are not meant to be limiting in any manner. For example, the notes and/or cited excerpts, may or may not be supplemented or substituted with different excerpt(s) of the relevant reference(s), as appropriate. Further, to the extent any error(s) and/or omission(s) exist herein, all rights are reserved to correct the same.

EXHIBIT C

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF OREGON

BELL SEMICONDUCTOR, LLC Plaintiff, v. LATTICE SEMICONDUCTOR CORPORATION Defendant.	**Case No.** **JURY TRIAL DEMANDED**

DECLARATION OF DHAVAL BRAHMBHATT

1. I make this declaration on behalf of Bell Semiconductor, LLC ("Bell Semic"). I understand that Bell Semic will offer my declaration as evidence in support of its contemporaneously-filed complaint for patent infringement in the above-captioned case.

2. My qualifications to testify concerning the relevant technology are set forth in my curriculum vitae, attached hereto as **Exhibit 1**.

3. I hold a Master of Science (M.Sc.) in Physics, with a specialization in Solid State Electronics, from Gujarat University in India, which I received in 1977. I also hold a Master of Science in Electrical Engineering (M.S.E.E.) from University of Cincinnati in the United States, which I received in 1978. My continuing education included a certificate in Executive Program for Small Companies in summer of 1993 and a certificate in Marketing Management in summer of 1994, both from Stanford University. I received additional certifications in International Marketing at the University of London in 1995 and certification as a Trained Nanotechnologist in 2007.

4. I have over 30 years of experience with integrated circuit design, semiconductor processing, semiconductor manufacturing, and product quality and reliability. Since 2002, I have served as the Founder, President, and CEO of PHYchip Corporation, a company focused on

memory and physical layer (PHY) chips as well as modules and sub-systems. I also occasionally serve as a technical expert in a variety of patent litigation lawsuits involving IC memory, CMOS Analog IC, I/O interface, SIMM/DIMM memory modules, and high-speed physical layer chips.

5. From 1978 to 1980, I served as a Senior Design Engineer at Fairchild Semiconductor Corporation where I was responsible for the memory design, debug, and production of the 32K bit EPROM memory and placing this non-volatile memory on a micro-processor in collaboration with the microprocessor design team. After my time at Fairchild, I moved to Synertek Inc. where I served as a Design Project Manager from 1980 to 1982. At Synertek, I was responsible for the design and development of an industry first 256-bit single power supply, 5V ONLY NMOS EEPROM with on-chip high-voltage generation. I received multiple technology pioneering patents for this invention.

6. In 1982, I decided to join National Semiconductor as a Design Manager. There, I was in charge of high-density single power supply 64 k-bit EEPROM memory. I left National Semiconductor in 1983 to start my own company, ICT, Inc., a semiconductor startup company in the area of high-speed programmable logic and programmable memory integrated circuits ("IC"). As Vice President of ICT, I personally designed leading nonvolatile memory and logic IC chips for the company, supervised engineering, and managed all design and product development in the company. As a Founder and Vice-President, I managed collaboration between ICT and its Japanese collaboration partner Asahi-Kasei Corporation, its Korean technology partner Hyundai Electronics, and its U.S. collaboration partners American Microsystems and Advanced Micro Devices. ICT, Inc. eventually went public and was thereafter acquired.

7. In 1989, I left ICT to join National Semiconductor again as a Product Line Director. I was in charge of the business unit in the memory IC product line where I supervised close to 100 employees and oversaw product development and P&L, amongst other responsibilities. As a

Senior Product Line Director, I managed collaborations between National Semiconductor and several partners, including the Japanese company Toshiba, and visited Japan frequently to both help develop new technologies with our collaborators and address suspected defects in products manufactured by National Semiconductor and incorporated into the products of Japanese customers and other customers worldwide.

8. In early 1996, I decided to leave National Semiconductor to join Smart Modular Corporation, a recognized leader in SIMM/DIMM memory modules, as a Vice President of Technology & Business Development. As Vice President, I developed and managed product development in IC memory based sub-systems such as PCMCIA, CompactFlash, and other memory cards/modules. This company also went public and was later acquired by a major worldwide manufacturer of electronic products named Solectron Inc.

9. In late 1997, I ventured to start yet another business, Modern Media Memory, Inc., where I served as the CEO until 1998. There, I designed and consulted on PCMCIA flash memory cards using NAND/NOR flash memory IC and CompactFlash cards using NAND flash IC.

10. Following Modern Media Memory, and around 1999, I joined MARS Technologies as Chief Operating Officer. This company designed and developed advanced network communications IC components focused on physical layer chips. MARS had a close technology collaboration relationship with Panasonic. MARS was acquired and the combined company eventually became a part of Broadcom.

11. Around 2000, I founded Modern Telecom that focused on advanced compound semiconductor (InP, GaAs) based technologies for telecommunications systems.

12. As an Adjunct Professor, I have taught graduate and undergraduate courses in Nanotechnology at Santa Clara University Graduate School of Engineering and at The Ohlone

College. I also taught full day courses on Nanotechnology at the Society of Photo-Optical Instrumentation Engineers (SPIE).

13. From 2006 to 2017, I was invited to serve on SBIR/STTR panels by NIH and NSF where I worked with other industry and academia experts to help the U.S. Government agencies decide on technology development funding awards for small companies in excess of tens of millions of dollars annually.

14. Over the years, I have received 11 U.S. patents in design and development of semiconductor devices. In ten of these eleven patents I was named as a sole inventor and as the lead inventor of each of the aforementioned patents. Four of these patents went on to have international counterparts.

15. I was named a Fellow under the National Scholarship Scheme by the Government of India and as a Fellow by Rotary International.

16. Currently I serve as the Co-Chairman of IEEE Region 6, Central Area. I am also the founder of the IEEE San Francisco Bay Area Nanotechnology Council and the former Chairman of the IEEE San Francisco Bay Area Vehicle Technology Society. I have received numerous awards by IEEE in 2007, 2008, 2012, and 2020. IEEE (Institute of Electrical and Electronics Engineers) is over 100 years old, and the biggest and most recognized worldwide organization of its kind.

17. Around 2007, I was appointed by then-Congressman Mike Honda and State Controller of California Steve Westly on the Blue Ribbon Task Force on Nanotechnology. Around that same time, I also made a presentation to the science sub-committee of the United States Congress.

18. I have reviewed U.S. Patent No. 7,396,760 to Taravade et al. ("Taravade '760"), which is asserted in the Complaint, and its file history. In addition, I have reviewed the claim charts accompanying the Complaint supported by this Declaration.

19. I have also reviewed various declarations of Lloyd Linder in support of other complaints filed by Bell Semic on patents relating to various aspects of dummy metal fill.[1] I agree with the substance of those declarations, and have reused their accurate descriptions of the background technology in this Declaration to help contextualize the innovations captured by Taravade '760. The portions incorporated from the Linder Declaration are identified by italicized text.

20. My college education over 7 years and 30-plus years of knowledge and experience in integrated circuit design, layout, and fabrication provides the necessary experience to support my stated conclusions set forth below.

Background on Integrated Circuit Manufacture, Including the Layout Process Flow Segment of the Manufacturing Process

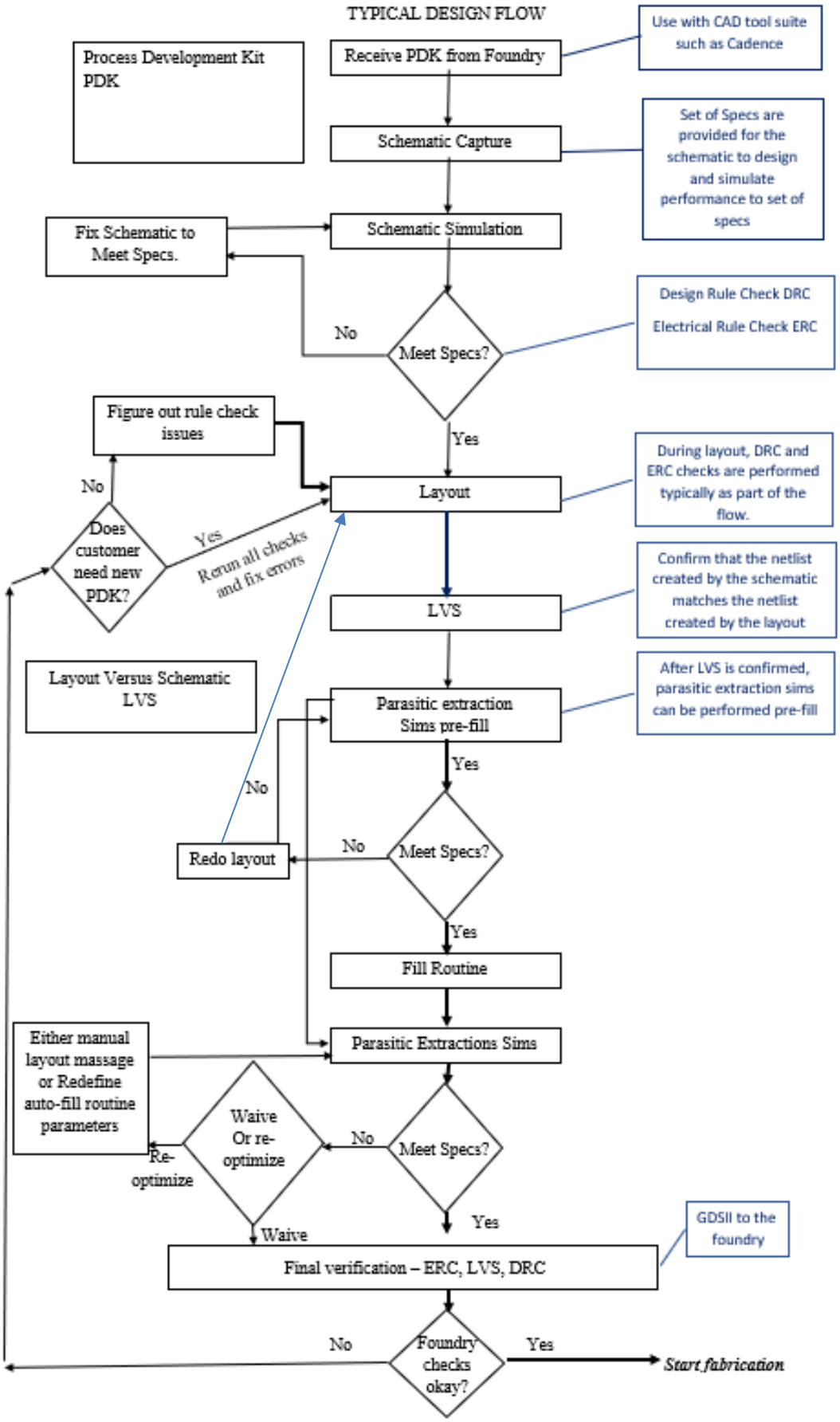
21. Semiconductor manufacture begins with the creation of a set of specialized electronic files that dictate the three-dimensional structure and features of the semiconductor device. These files, which are normally referred to as Graphic Design System (GDSII) files, are specifically formatted for and serve as necessary inputs for the devices that build the semiconductor device layer-by-layer according to the instructions contained in the GDSII files. Any changes to the structures in the GDSII files will result in changes to the structures in the fully

[1] These Declarations relate to the Shrowty '259, Cwynar '807, Lakshmanan '803, and Hoff '626 patents.

fabricated device.[2] *The manufacturing process ends with the wafer containing the individual semiconductor devices being fully fabricated and sawed into individual semiconductor dies.*

22. The image below (although not in italics, is borrowed from Linder Declaration) *provides a simplified schematic showing, at a high level, a commonly-used integrated circuit design flow process that is representative of many (if not most) process flows in current use for creation of circuit layouts:*

[2] *The physical design validation of an integrated circuit design ensures that all spatial constraints are satisfied for the traces and devices formed in various layers of an integrated circuit die. The structures formed in the several layers of an integrated circuit die are represented in a GDSII format file that contains the chip topological information for creating the masks used in manufacturing the integrated circuit dies. This is also called the "layout," and which patents in this area typically call a "design". The GDSII format is an industry standard used by commercially available physical verification tools to represent physical design data. All structures affecting the performance of the circuit die must and will be present in the layout.*


TYPICAL DESIGN FLOW
Process Development Kit PDK
Receive PDK from Foundry
Use with CAD tool suite such as Cadence
Schematic Capture
Set of Specs are provided for the schematic to design and simulate performance to set of specs
Fix Schematic to Meet Specs.
Schematic Simulation
No
Meet Specs?
Design Rule Check DRC
Electrical Rule Check ERC
Figure out rule check issues
Yes
No
Layout
During layout, DRC and ERC checks are performed typically as part of the flow.
Does customer need new PDK?
Yes
Rerun all checks and fix errors
LVS
Confirm that the netlist created by the schematic matches the netlist created by the layout
Layout Versus Schematic LVS
Parasitic extraction Sims pre-fill
After LVS is confirmed, parasitic extraction sims can be performed pre-fill
Yes
No
Redo layout
No
Meet Specs?
Yes
Fill Routine
Either manual layout massage or Redefine auto-fill routine parameters
Parasitic Extractions Sims
Waive Or re-optimize
No
Meet Specs?
Re-optimize
Yes
Waive
GDSII to the foundry
Final verification – ERC, LVS, DRC
No
Foundry checks okay?
Yes
Start fabrication

23. The integrated circuit design flow process includes a design engineer, using design tools, to create a design for an integrated circuit to be processed.

24. Design tools from vendors such as Cadence, Synopsys, or MentorGraphics (now Siemens) will then be used to design, simulate, and lay out integrated circuits. The typical design tool suite includes[3] schematic capture, simulation, layout, verification (layout versus schematic (LVS) and design rule check (DRC)), and fill generation routines. These fill routines can be automated or manual, and can be provided by the design tool company in whole or in part.

25. *To be sure, the precise capabilities of each design tool available to a particular design engineer may differ within a company (based on what options in the design suite are available to a particular user or on a particular device), and between different design tool suites. However, based on my experience, at a high level, the design tools used by design engineers in the semiconductor industry, all operate in substantially similar fashion for schematic capture, simulation, layout, verification, design rule check, and fill-generation.* In particular, based on my experience, I agree with Lloyd Linder that, the design tools commonly used in the industry to place dummy fill operate in substantially similar fashion in providing incremental and timing-aware fill generation for integrated circuit layouts, including the tools used for calculating the additional interlayer and intralayer capacitance in the placement or adjustment of dummy fill.

26. In the design process, the schematic is created first. The layout design tool is used to place and route all of the active (i.e., transistors) and passive components (i.e., resistors, capacitors, and inductors), and the interconnections between devices (represented as wires) in the schematic. It represents the circuit function that is to be physically implemented in the silicon. The schematic is created and simulated, using the CAD tools, to confirm that the circuit functions to a desired specification.

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[3] *Sometimes electrical rule check (ERC) is also included in design tool suite capabilities.*

27. Once that performance specification is confirmed from the schematic simulation, the layout of the circuit is performed to physically place each of the individual elements necessary to implement the circuit functions set forth in the schematic in the GDSII file. During layout, layout rules for active and passive devices must be followed, but conformance is not checked until a DRC is run (typically at least as part of the final verification, though it can be run at any point or points in the layout process).

28. Once the layout is completed, it is compared to the schematic of the circuit using layout-versus-schematic (LVS) tool to confirm that the two are identical. From the schematic, a netlist (a list of devices and the associated nodes) is generated. From the netlist, the schematic could be re-generated manually *by drawing the devices and connecting the device nodes. From the layout of devices and associated nodes, a corresponding netlist is generated, from which a similar schematic could be generated by hand by drawing the devices and connecting the device nodes from the layout netlist. Then the schematic netlist is compared to the layout netlist using the LVS tool. The LVS tool compares the schematic netlist to the layout netlist to see if they match—i.e., whether they contain the same devices connected in the same fashion. If they do not match, the discrepancies between the two must be found and corrected, and LVS re-run. Any violations of layout rules must be corrected and DRC re-run for the layout.*

29. After passing LVS, the process of performing parasitic extraction simulations before the fill has been placed (pre-fill) can be performed on an extracted netlist created from the layout. If parasitic simulations are performed prior to the fill placement, the designer can get an idea of the impact on circuit performance from the basic layout parasitics pre-fill. From the layout, a netlist is extracted that includes any of parasitic resistance (R), *parasitic inductance (L), parasitic capacitance (C), or any combination of the three. Additionally, the parasitic extraction can include what is termed "coupled" capacitance (parasitic capacitance between metal lines) as*

well as the parasitic capacitance to the substrate. For maximum accuracy, this should not only include intralayer effects (i.e., interactions between metal elements on the same layer, such as between dummy fill and signal lines) but also interlayer effects (i.e., interaction between parallel or overlapping metal features on adjacent layers), The extracted netlist, with the selected added parasitics, can be used to run simulations on the baseline layout to determine if there is any performance degradation due to the baseline layout routing.

30. The simulated performance of the layout, which includes the parasitics, needs to be as close as possible to the specification that was already satisfied by the schematic. That is why parasitic extraction is performed, and why it is iterated pre-fill and post-fill. So if there is performance degradation due to the baseline layout, the layout is redone until its performance is at acceptable parameters. Ideally, the extracted simulation results closely *match the schematic simulation results, which means that the layout parasitics had no* significant *impact on the circuit performance.*

31. Once the layout passes pre-fill, the design tool is used to insert dummy fill at appropriate locations in the layout that ideally *do not contain devices or other features. As is well-known in the industry, the purpose of adding dummy fill is to achieve a higher and more uniform density of interconnect across the surface of each layer of the chip, to improve the outcomes of the chemical-mechanical polishing/planarization (CMP) step during fabrication. If individual pieces of fill are below a certain minimum size, they may* give rise to planarization issues *during CMP, which will result in the dielectric material deposited on top of those too-small features not planarizing properly,*[4] *which will produce ~~in~~ dishing in the dielectric and result in a non-*

[4] *The effect on the dielectric from underlying interconnect is known as the deposition bias. A "positive bias" or "positive deposition" bias is when the width of the protrusion in the dielectric is greater than that of the underlying active interconnect feature. Conversely, a "negative bias" or "negative deposition bias" is when the width of the protrusion in the dielectric is less than that*

planarized surface. Thus, in practice, the fill pieces added cannot be below a certain minimum feature size. Adding dummy fill at or exceeding the minimum feature size and to achieve a higher and more uniform density of interconnect lowers the likelihood of defects caused by the CMP process step and thus improves the yield of modern integrated circuits.

32. Once all components of the integrated circuit design have been placed and routed, a physical design validation is typically performed at the very end of the design cycle. This ensures that all spatial constraints are satisfied for the traces and devices in each layer of an IC, that the die complies to all process rules, and that any additional required steps specific to manufacturability for a selected technology have been performed (e.g., metal utilization).

33. Even after a physical design validation, the physical design may change for any one of a number of reasons, including but not limited to timing delays, performance, or functionality. In such instances, the various steps in the process flow will have to be redone to accommodate the changes in the physical design. This includes placement of dummy fill as well.

34. *As the pre-fill step confirms that parasitics of the baseline layout, pre-fill, do not degrade the performance of the integrated circuit, it is desirable that the fill likewise does not degrade performance. However, depending on its placement, dummy fill can also degrade the performance of the integrated circuit, which is undesirable. To minimize this, the design suites include timing-aware fill tools that minimize, if not prevent, any degradation to circuit performance caused by dummy fill insertion. These tools also incorporate details on fill density, size, and position necessary to meet the requirements of the fabrication process and allow the user to specify the minimum and maximum dimensions of the dummy fill.*

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of the underlying active interconnect feature. In either case, large density variations of the active interconnect features will typically result in interconnect that is insufficiently planarized during CMP, and thus, overpolishing of the dielectric that produces significant dishing. This is particularly detrimental in fabrication of multi-layer chips and packages.

35. Based on my experience, I agree with Lloyd Linder that the use of such timing-aware fill tools has become standard practice in designing modern integrated circuits. *In fact, modern integrated circuit designs are required to have fill included as part of the database submitted for fabrication. Due to the complicated nature of these designs, such as SoCs and highly integrated circuits with many layers, the fill process cannot be manual at least for the practical reason of there being far too many locations and options for fill position and dimension to designate by hand for fill insertion. Moreover, the chip has many critical nets (i.e., important timing-sensitive signal lines), so there is a need for the fill-placement to be aware of any impact on the timing and resulting performance impact of the circuit. Timing-aware fill tools are used to attempt to simultaneously meet interconnect density (including feature size) and timing closure requirements, but they are not guaranteed to do so 100% of the time. When this occurs, a decision must be made to compromise performance at the expense of yield, or vice-versa.*

36. Once the fill routine is completed, the fill checks are done, and final verification is performed again (LVS, DRC). The fill checks are performed based on percentage requirement on a specified area in the layout.

37. Once the layout database has been verified, it is sent for fabrication in the form of a GDSII database, which is the industry standard format for delivery of the chip database. As previously mentioned, fill is required to be included as part of the GDSII database.

38. The design resource is provided with a process design kit (PDK), which includes all of the information necessary to capture a schematic, run a simulation, do a layout, and perform all of the checks on the layout to make sure that the final GDSII is in an acceptable form to be ready for fabrication. It is the design resource / customer's responsibility to make sure that the designed chip meets all of the expected requirements for fabrication and the design resource / customer *bears the risk of failing to follow any steps in the design flow. For example, if the circuit*

does not work, that is the customer's responsibility. If the layout does not match the schematic, that is the customer's responsibility. The GDSII does have to meet all of the DRCs in order to be fabricated.

39. In order to develop an integrated chip product, tools are needed to develop the schematic, the layout, verification of the layout, and the final GDSII database for fabrication. Many companies use different tools (from different vendors) to accomplish this process either typically due to cost or preference of internal proprietary tools. Regardless of the process and specific tools that are used, the GDSII database goes through an internal DRC after it is received and before fabrication of the integrated chip:

a. *The design resource receives a PDK that contains all of the information is included to create a GDS database to release for fabrication. This includes circuit symbols for the creation of the schematic, models for the circuit symbols to run simulation, and associated layout devices that have been created with all of the process layers needed.*

b. *Additionally, there are what are known as "rule decks" in the PDK that allow for LVS and DRC. A rule deck is typically a file that specifies all of the available rules (for example, minimum feature sizes such as line width*, line spacing, *and minimum fill dimensions), the layers to process on each rule, and the parameters of each rule. The LVS deck compares the schematic to the layout, and the DRC deck covers all of the design rules for placing and routing devices. For LVS, a netlist of the layout is created. This netlist is compared to a netlist created for the schematic. The LVS tool compares the two to determine if they match or not.*

c. *Additionally, there is a parasitic extraction deck that extracts all of the parasitics of the layout that is used to run simulations to close timing or to confirm that the layout still meets all of the chip requirements.*

d. *There can also be an electrical rule check (ERC) deck as well, depending on the fabrication involved.*

40. *If the DRC rules at pre-fabrication do not match those at the design resource, it is possible that there will be DRC errors. This could be due to a number of reasons, including the DRC in the provided process design kit (PDK) is not up to date, and so the PDK will be updated with the updated DRC and the design resource will have to redo* the necessary portions or even *everything and fix the DRC errors, providing a new GDSII database before fabrication can begin. These DRC checks at pre-fabrication will include checks for the fill on all layers to confirm that the fill requirement is met, on a granular level, for all tiles at the chip boundary level.*

Dummy Fill is Required in Design and Layout of Multi-Layer Semiconductor Chips

41. I agree with Lloyd Linder that, to the best of my knowledge, adding dummy fill is a requirement for every integrated circuit using the latest technology nodes. Certain older nodes still in fabrication (>350nm) may not require fill, but I believe that even some of these older technology nodes have incorporated fill requirement to enhance yield.

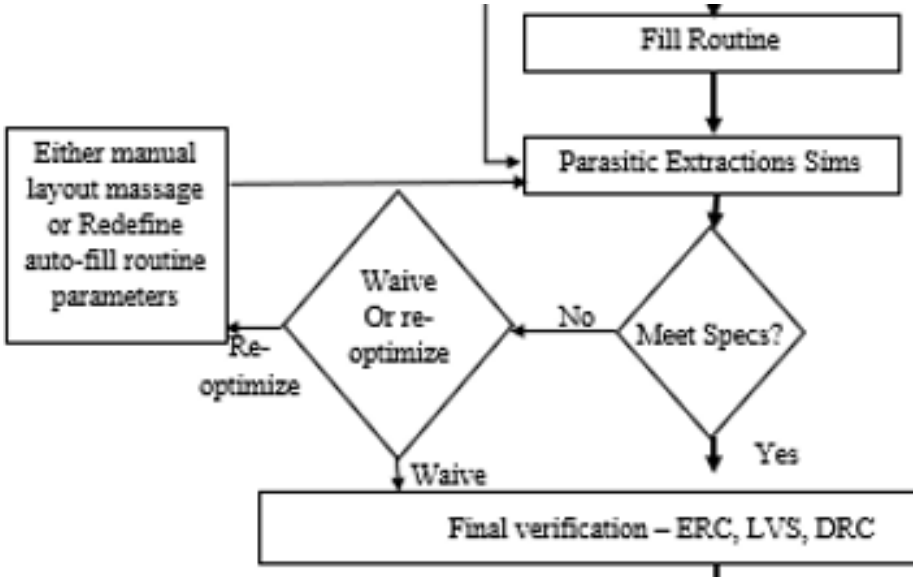
42. *As mentioned above, it is required that the GDS database include fill within the database submitted for fabrication. In particular, most fabrication processes used in modern semiconductor chip designs require both a minimum density and a minimum feature size for the interconnects (i.e., pieces of metal or semiconductor) placed on each layer of a multi-layer chip design. This is the case both for each of the layers as a whole and for individual subunits of each layer, and is fundamental to the creation of consistent fabrication of multi-layer devices with minimal defects.*

43. Fabrication processes typically partition each layer of the chip design into rectangular regions called tiles, each of which must also meet a minimum density requirement. For any given region of the chip, the interconnect density is the area of all of the interconnect in that region divided by the total area of that region.

44. Sufficient interconnect density and substantial uniformity of interconnect are required for the chemical mechanical polishing (CMP) portion of the chip fabrication process. CMP is crucial to achieve planarity, which allows for multi-layer chip designs and high yield of functional devices. Insufficient interconnect density and/or insufficient uniformity of interconnect between various regions will increase the likelihood of defects during the chip manufacturing process, which will resultantly degrade the yield.

45. Once the functional features of the chip design (such as power lines, signal nets, vias, and the like) have been laid out as needed in the first instance, there will usually be substantial portions of the chip design that have insufficient interconnect density to permit CMP without incurring substantial likelihood of defects.

46. To increase the interconnect density of the layer as a whole, and of regions within each layer, numerous individual pieces of interconnect are inserted into available space in low-density regions of the chip until the minimum interconnect density specified for the particular fabrication process is achieved for each tile. Because these pieces of interconnect are not intended to carry signal or power, but instead are added to provide structural stability to the chip during processing*, they are generally known as "dummy fill."*



47. Placement of dummy fill is typically performed by a dummy fill software tool, and is one of the last steps in the chip design flow, with its extent and placement typically occurring after routing and timing closure. The time it takes the dummy fill tool to complete its task depends on the complexity of the circuit layout, and correspondingly, the size of the design database. If dummy fill must be run (or re-run) for the entire layer, even small changes in layout can result in significant delays while the dummy fill tool runs each time the layout changes.

48. In operation, the dummy fill software tool typically partitions each layer of the design into rectangles called tiles, which it examines in each layer of the design. If the interconnect density in each tile does not meet (or exceed) the specified minimum interconnect density for the fabrication process, the dummy fill tool inserts dummy fill into free regions of that tile where no interconnect is present.

49. The dummy fill software tool typically allows the user to specify the shape (rectangular or square) and dimensions (maximum and minimum) for the dummy fill to be inserted into open areas of the layout. In addition or alternatively, fill dimensions, shape, and position can be (and typically are) supplied separately from the fabricator in a format such as a LEF file, which

the dummy fill software tool then incorporates and uses to place dummy fill in open areas of the layout

50. For large integrated circuits, commonly called system-on-a-chip (SoC) with either large analog content and small digital content ("big A, little D") or large digital content and small analog content ("big D, little A"), it is not practical to manually add dummy fill, so automated fill routines are almost always used. Because there are so many critical signals in a large SoC, the process cannot be done manually due to the time and trained human resources *it would require. Thus, the design timelines and practical realities require that the automated fill routines are used instead.*

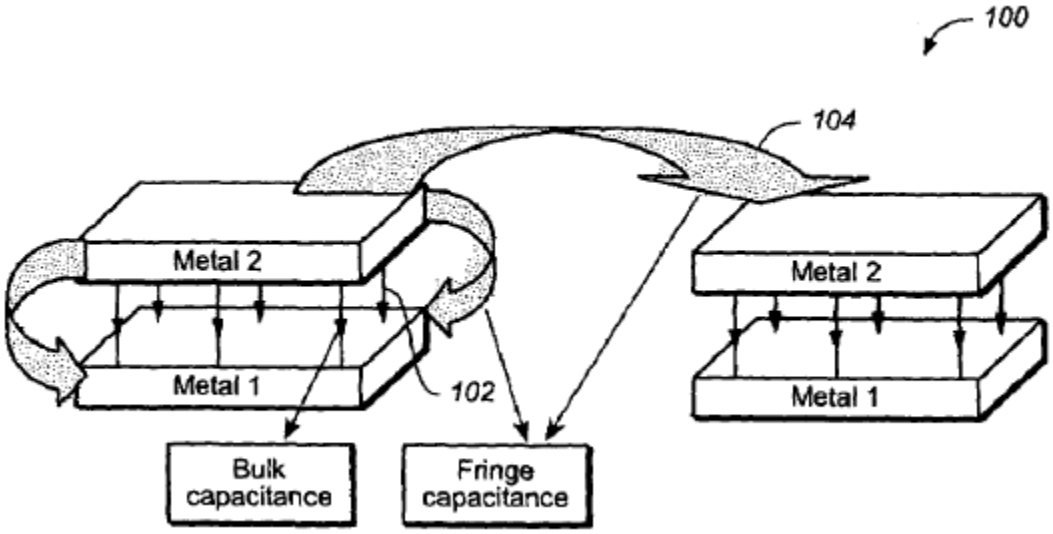
51. However, placing the dummy fill that is too large in size, too extensive, and/or too close to signal nets increases capacitance between the signal wires and the dummy fill in the physical device if fabricated without taking additional measures. That increase in capacitance in the fabricated physical device would in turn slow the transmission speed of signals and degrades the overall performance of the integrated circuit. This effect between the signal wires and the dummy fill (or dummy fill and other dummy fill) *is undesirable and is* caused by what is generally *known as "parasitic capacitance."*

52. The added parasitic capacitance will degrade parameters, such as operating frequency and rise/fall time, for a critical clock or signal, and this must be avoided in order for the circuitry to work properly. The manufacturers often would be required to sell units that are slow but fully functional otherwise at a significantly lower average selling price (ASP).

53. The parasitic capacitance within a layer is inversely proportional to the distance between the dummy fill and the signal wire. Thus, parasitic capacitance from dummy fill will be minimized if the dummy fill is placed far from signal nets.

54. *In other words, the higher the required interconnect density, the closer it must be placed to signal nets, with increasingly higher parasitic capacitance and negative impact on timing and circuit performance. Conversely, the more sensitive the timing requirements for the circuit, the less the parasitic capacitance can be tolerated near crucial signal nets and the lower the interconnect density can be for tiles that include such signal nets. This tradeoff is further complicated when multiple metal layers are involved, which can be ten or even more.*

55. However, parasitic capacitance also arises from interlayer effects, as shown in Figure 1 of Taravade '760, which depicts how overlapping metal elements (both signal-carrying and non-signal-carrying) on different layers can still produce unwanted and undesired capacitance:



56. Some portion of the bulk capacitance, such as that due to the overlap of signal lines, may not be easily addressed to a meaningful extent because the placement is dictated by circuit functionality and circuit layout realities. Accordingly, their overlap on adjacent layers (and thus, their contribution to unwanted bulk capacitance) may be difficult to reduce.

57. However, the interlayer bulk capacitive effects contributed by other features, such as that resulting from overlapping dummy fill features on adjacent layers, is more readily addressed. Especially compared to signal lines, the specific positioning of particular dummy fill

features (which do not carry signal) is not dictated nearly as strongly by circuit functionality demands. Rather, as discussed in greater detail above, the considerations for dummy fill placement primarily involve reaching sufficient density of interconnect for each tile on a layer and the layer as a whole, uniformity of interconnect density, and minimizing timing impact on crucial signal nets. Thus, it is possible to consider the capacitive interactions between dummy fill features on adjacent layers and to mitigate their negative effects by minimizing their overlap (thereby reducing the interlayer bulk capacitance) by repositioning the dummy fill features in one layer relative to the dummy fill features in an adjacent layer. Given the relatively small size of dummy fill features relative to signal nets (and especially crucial signal nets), and the typical spacing provided between individual features, this can readily be accomplished with no more than a miniscule impact on intralayer effects and without reducing interconnect density or uniformity on the tile or the layer.

58. It may be that the timing requirements cannot be met without a revision to the fill placement, density, positioning, and/or sizing, and re-extraction of the layout parasitics to determine if the timing requirements are met. If they are not, then a decision would have to be made to either (i) continue the iteration process, or (ii) apply for a waiver and bear the risk of lower yield or (ii) accept decreased performance that could significantly impact the ASP as was explained earlier.

59. Balancing these tradeoffs started to become particularly problematic by the early 2000s, as new processing technologies with smaller and smaller features demanded increasingly higher minimum interconnect density values at the same time that chip designs became much more aggressive in the circuit timing requirements. In such cases, it was often almost impossible to insert sufficient dummy fill into a tile such that the higher minimum density requirements could be met without also reducing the large “stay-away” distance, and thereby raising the timing impact of the dummy fill to levels that affected the performance of the chip. One potential solution was for the

chip designer to waive the minimum interconnect density specified by a particular fabrication process. However, because invoking this waiver would not comply with the fabrication process requirements, the yield of the produced devices would not be guaranteed in such cases, which rendered this alternative not viable in practice.

60. Even when dummy fill placement on an individual layer of the device was not problematic by itself, its interactions with overlapping dummy fill features on adjacent layers could and still did result in substantial undesired capacitance from interlayer effects. That is because even "timing-aware" or "smart" dummy fill tools conventional prior to the time of Taravade '760 focused primarily on solving the problems of feature density and uniformity *within a layer* or portions of a layer. *See* Taravade '760 at 1:62–67, 4:11–16. While they may have considered the timing impact of dummy fill, that impact was typically limited to *intra*layer effects, such as on adjacent signal nets.

61. Accordingly, these tools and methodologies for inserting dummy fill generally treated each layer independently. Because they did not typically consider *inter*layer capacitance even when applying timing-aware methodologies and techniques, they tended to produce substantial overlaps in dummy fill features between adjacent layers.

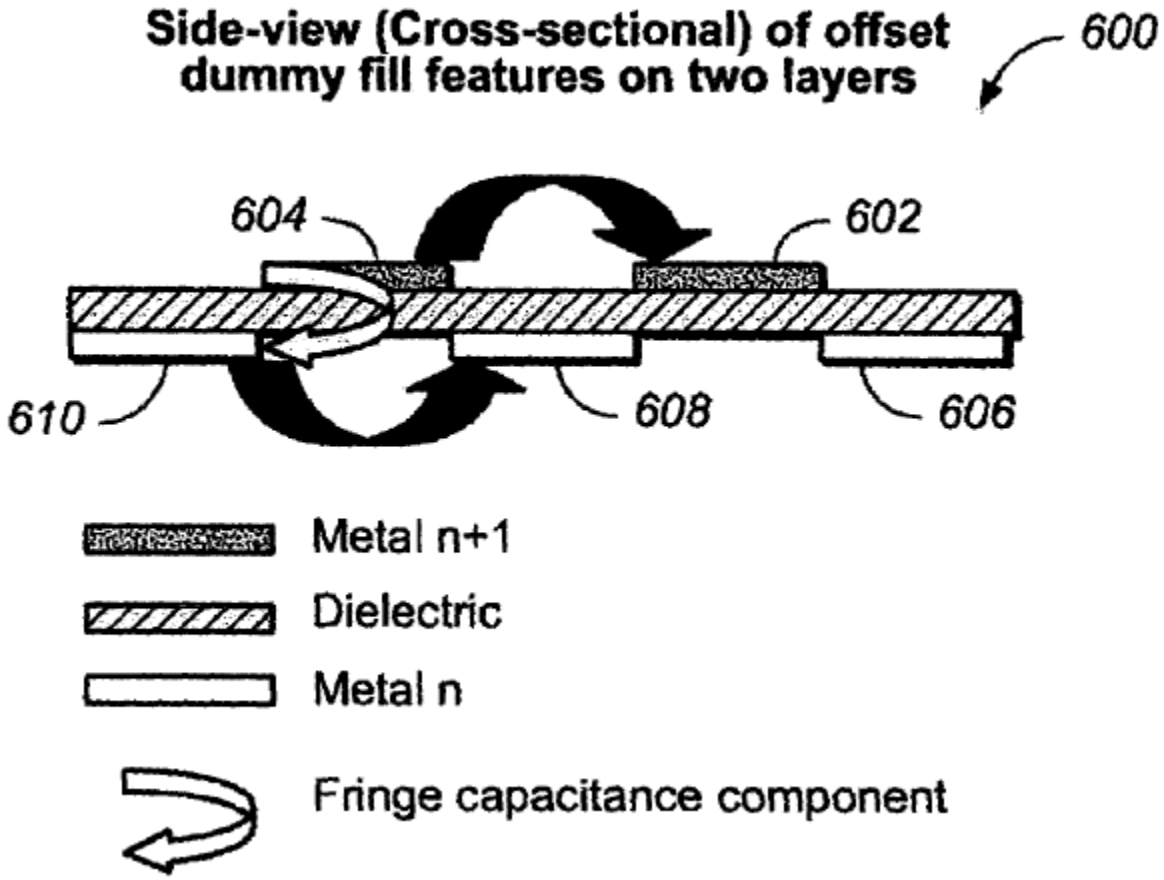
62. This unwanted bulk capacitance would tend to slow down signals in the IC and adversely affect its timing. *See* Taravade '760 at 2:1–6. Adjustment of layers individually and manually to reduce overlap in dummy fill features to mitigate interlayer capacitance was an involved and time-consuming iterative process that could produce substantial delays in meeting design schedules. Especially as features became smaller and performance demands increased, it became both increasingly important and increasingly difficult to remove additional sources of unwanted capacitance from the ICs.

Taravade '760

63. Even when dummy fill could be placed in such a fashion that it would simultaneously satisfy interconnect density requirements for each tile and minimize any impact on critical nets within a layer, prior to Taravade '760, the contribution of adjacent layers' overlapping dummy fill to interlayer capacitance could and did still have a substantial negative impact on timing . *See* Taravade '760 at 4:14–16.

64. Taravade '760 teaches a technique and a system for reducing the bulk capacitance caused by overlapping dummy fill in adjacent layers by repositioning the dummy fill features so as to minimize their overlap by not only considering each layer on its own, but also with respect to each of its adjacent/successive layers, by treating "each consecutive pair of layers together." Taravade '760 at Abst. Once the circuit layout is provided, suitable spaces for dummy fill insertion are identified. *See id.* at 2:28–31 & 2:41–43. Overlaps or potential overlaps are determined and then avoided. *See id.* at 2:31–34 & 2:40–48.

65. Dummy fill can be arranged initially to minimize overlaps and/or rearranged to minimize overlap in features once avoidable overlaps are discovered. *See* Taravade '760 at 2:28–34 & 2:43–48. Either way, in considering each individual pair of layers as a unit, the final placement of dummy fill features on the top layer will not be placed directly above dummy fill features on the lower layer; they will be offset in order to reduce the unwanted bulk capacitance and thus minimize the inter-layer capacitance. *See id.* at 2:49–59, 4:47–49. For square-shaped dummy fill features, this will typically result in a checkerboard-like pattern. *See id.* at 2:49–55.



66. The significant bulk capacitance reduction (and thus, increased ability to meet demanding performance requirements and operating speed) are repeatedly described within *See, e.g.*, Taravade '760 at 1:24–30, 2:3–6, 2:57–59, 3:30–33, 4:43–45, 4:47-49, 5:18–39. This helps IC manufacturers eliminate the large bulk capacitance component and reduce the total capacitance of an IC. *See id.* at 5:23–27.

67. Based on my experience in semiconductor layout and design, I agree that this new and improved technique of offsetting dummy fill features in adjacent layers results in substantial bulk capacitance reduction in an integrated circuit, and is crucial to meeting the aggressive performance demands of modern ICs. These gains are so substantial, and in my experience, the offsetting of dummy fill features in adjacent layers to prevent their overlapping is so widely used today that it is hard to quantify just how important the inventions claimed by Taravade '760 are to

achieving the market-demanded performance and the resulting financial gains from the marketing/sales of modern chip designs.

68. Based on my experience in semiconductor layout and design, it was not well-understood, routine, or conventional at the time of Taravade ’760 to identify overlap in dummy fill features in adjacent layers in multi-layer IC designs. Likewise, it was not well-understood, routine, or conventional to rearrange one or both sets of dummy fill features to minimize their overlap. These aspects of the technique, recited in claim 1 of Taravade ’760, are central to the invention and required by every claim of the patent. This is true not only considering each of these elements by themselves, but also in combination with each other and as an ordered combination with the other recited claim elements. As Taravade ’760 explains, “the problems created by the inserted dummy fills such as adverse effects on the electric field, unwanted bulk capacitance, and the like have not been addressed.” (1:63–65.)

Claim Charts

69. I have reviewed the Complaint supported by this Declaration, along with the Claim Charts showing infringement of Taravade ’760. For at least the reasons set forth below, I agree that the Claim Charts establish use of at least one of the methods recited by the claims of Taravade ’760.

70. I have used design tools from different vendors in my career. As a consultant, I use the tools to review schematics and layouts and design and simulate circuits. Based on the requirements for the latest process technology nodes,and the yield requirements for these technologies, the latest fill tools that are used by designers and/or foundries use timing-aware fill routines with minimum fill dimensions to meet timing as well as yield requirements simultaneously. These include rearranging dummy fill features to minimize overlap in adjacent layers and eliminating another source of unwanted capacitance from the IC.

71. In particular, these tools allow rearrangement of dummy fill features to minimize overlap that would otherwise occur as a result of the inevitable and frequent ECOs and/or other layout changes during the design process. In my experience, layout changes in at least one layer are a near certainty in all recent process nodes given the complexity of the chips, aggressive timing and performance requirements, and small feature sizes. As a result of these layout changes, existing dummy fill will need to be adjusted or repositioned not just to account for the new intralayer effects, but also to minimize any interlayer effects as a result of layout changes (and corresponding changes to dummy fill spacing, positioning, and dimensions) on adjacent layers as well.

72. Based on my work history in industry and as I have done as a consultant, I can review reverse engineering ("RE") of semiconductor die to confirm that at least one of these tools (or similar tools) have been used to construct the layout or the die.

73. Even when the full history of the GDSII database for a particular integrated circuit is not available, my experience in semiconductor design and layout gives me sufficient basis to opine whether one or more of the methods claimed in Taravade '760 have likely been used in creating integrated circuits.

74. Given the aggressive schedules for bringing modern semiconductor devices to market, and the availability of incremental dummy fill in common design tools like Cadence's Innovus product, it is unlikely (if not implausible) that most chip designers would not have access to design tools that practice the inventions claimed in Taravade '760. I am aware that at least Cadence provides this functionality.

75. Among other things, it is my understanding from the Cadence Innovus User Guide that when Cadence applies a staggered metal fill, it is by default only staggered in the preferred routing direction; it is not staggered (and thus overlaps) in the non-preferred direction. Thus, in order to minimize the overlap between the dummy fill features, it is necessary to assess the extent

of the overlap in the non-preferred dimension (where the fill is not staggered) and then further rearrange the default staggered metal fill applied by Cadence to create dummy metal fill that is fully offset in adjacent layers on both horizontal axes, rather than just one as is necessary to fully minimize interlayer bulk capacitance.

76. As such, based on my experience in semiconductor layout and design, and my review of designs, I believe that it is highly likely that such functionality was used in creating most modern semiconductor devices given the importance of reducing capacitance, including interlayer capacitances, in achieving timing closure and modern performance requirements.

77. By contrast, based on my experience in semiconductor layout and design, I would only assume that relatively simple IC designs would have been made in recent years without employing at least one of the methods claimed in Taravade '760. Simply put, there is no reason to accept substantial interlayer parasitic capacitance if it is relatively straightforward and easy to rearrange the dummy fill patterns between layers to minimize their overlap, and thus, their capacitance.

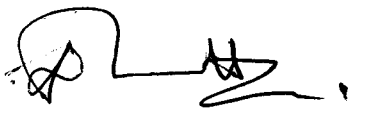
78. In addition, based on my experience, it can be assumed with a high degree of confidence that modern components in the same family or product line made by the same producer and used by the same customer in the same product line share similar features and were designed and laid out in similar fashion. This includes offsetting dummy fill features between adjacent layers.

79. *The Cadence paper "New Metal Fill Considerations for Nanometer Technologies" demonstrates several things. First, the use of the word "new" is justified in that it is a new approach, as documented here.* Secondly, it reinforces the importance of formulating "a comprehensive methodology surrounding metal fill . . . in order to minimize impact on design timing as well as to cut down on design iterations." The paper explains that "sometimes the dummy

metal fill geometries that were added to the original design must be deleted to make room for the ECO process to succeed." Overall, this indicates that, at least following ECO, the Cadence tool suite is used for offsetting dummy metal fill following ECO to minimize overlap of features (and thus, interlayer capacitance), as claimed in Taravade '760.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Dated: October 7, 2022



Dhaval Brahmbhatt

EXHIBIT 1

Dhaval J. Brahmbhatt ---- Confidential Resume ----

President & CEO, PHY*chip* Corporation

At a Glance:

- Expert witness in patent litigation nearly 20 years (ITC, PTAB, USDC, State Courts)
- Collaborated with JEDEC, CompactFlash Association, SEMI, etc.
- Experienced IC Product Development & Design Engineer, Modules/Sub-systems
- Awarded 11 US patents in IC device/devl., of these four became international patents
- Two graduate degrees (Physics, Electrical Engineering) & a number of certifications
- Entrepreneur - Started companies, went through IPO, acquisition, etc.
- Programmable memory IC and Modules/sub-systems (Flash, EEPROM, EPROM)
- Communications IC, DRAM/SRAM memory IC and SIMM/DIMM cards experience
- Device debug and product development experience
- Founder & Chairman Emeritus, IEEE S F Bay Area Nanotechnology Council *
- United States Citizen

IEEE – Institute of Electrical & Electronics Engineers – prestigious worldwide organization over 100 years old.

Professional Summary

Mr. Brahmbhatt has worked as Expert Witness with leading IP law firms, multi-national companies and patent holding firms for almost 20 years. Brings ITC, PTAB, US District Court experience. Over the past 20 years he has been involved in a variety of IC design, semiconductor manufacturing equipment and sub-systems IP matters. Additionally, has the rare experience of modifying claims at the USPTO of an existing US patent. He regularly visits events at the newly opened US PTO office in San Jose and has been trained in the proprietary prior art search tools offered by the US PTO.

Mr. Brahmbhatt is a creative engineer awarded 11 US patents (four became Int'l patents) and brings years of hands-on product design/development experience in IC memories (standard & custom), memory cards/modules (Flash Memory Modules, SIMM/DIMM), interface buses, logic circuits, driver circuits, micro-controllers, programmable logic, remote keyless entry for cars, tags for inventory control, etc. Mr. Brahmbhatt has participated in standardization committees for Flash Memory Cards. As Vice-President at the recognized memory module maker Smart Modular Technologies, he developed memory modules while at National Semiconductor, Mr. Brahmbhatt was in charge of managing Flash Memory IC alliance with Toshiba Corporation and National Semiconductor. As Sr. Product Line Director, he doubled the revenues and made his product line profitable by systematically addressing design, production and yield issues. He brings years of experience managing collaborations with international partners such as Asahi-Kasei (Japan), Hyundai (Korea), Toshiba (Japan), Intel, AMD, etc.

Mr. Brahmbhatt is a serial entrepreneur listed on the prestigious Silicon Valley Genealogy Tree for the 1983 IC Programmable Memory and Programmable Logic high-

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tech startup, ICT Inc., this company made IPO in 1989. He was Vice President responsible for memory sub-systems/modules/Flash memory cards employing a micro-controller at Smart Modular Technologies, this SIMM/DIMM company also made an IPO and later got acquired. Following Smart Modular, Mr. Brahmbhatt was COO at MARS technologies (worked on high-speed transceivers) that was acquired by Globespan-Virata, which itself got acquired by Broadcom. Mr. Brahmbhatt then developed ultra-high-speed transceivers (40 Gb/s) using compound semiconductors at Modern Telecom, Inc. Mr. Brahmbhatt's engineering experience spans from being an individual contributor to Engineering VP to "C" level executive in tech companies. He has worked in all aspects of IC starting from masks to fab to packaging and yields.

Mr. Brahmbhatt champions emerging transportation technologies at the San Francisco Bay Area unit of IEEE Vehicle Technologies Society of which he was the Chairman for 2013-2018. In addition to being the Co-Chairman of Region 6, Central Area of IEEE, he is also the Founder and Chairman Emeritus of the IEEE SF Bay Area Nanotechnology Council and was a member of the Blue-Ribbon Task Force on Nanotechnology for the State of California. He is a Senior Member of the IEEE and has been recognized numerous times by the IEEE with citations and awards. He is the past President of prestigious Silicon Valley Engineering Council which represents various engineering societies in the Silicon Valley. Mr. Brahmbhatt has participated as a Program Chair at the Flash Memory Summit held every year at Santa Clara Convention Center for the past several years. He was also a keynote speaker for the International Conference of the IEEE Vehicle Technology Society held at Santa Clara Convention Center in 2013.

Mr. Brahmbhatt has been an Adjunct Faculty at Santa Clara University Graduate School of Engineering and Ohlone College and has taught full day courses at Society of Photo-Optical Instrumentation Engineers (SPIE). Mr. Brahmbhatt holds an M. Sc. Physics from India and M. S. E. E. from Ohio (USA), he has received numerous scholarships & fellowships during his distinguished education career.

---------- **Current Employment & Other Information** ----------

Current Employment

From:	2002	PHY*chip* Corporation
To:	Present	Milpitas, CA
	Position:	Founder, President & CEO
		Design consultation, commercialization of research, and Intellectual Property support for IC & modules. Worked as a technical expert/expert witness in a variety of patent litigation involving IC fab equipment, semiconductor process/device & design, JEDEC standards, Non-Volatile & Volatile Memory, data communications, USB Flash, CMOS Analog IC, I/O interface & drivers, SIMM/DIMM memory modules, data security/integrity in Flash memory, etc. Appointed by US District Judge as his technical consultant on a DRAM patent litigation.

Mr. Brahmbhatt is sole inventor on 10 and the lead inventor on all 11 patents listed:

Patent #	Issued	Title
5,646,886	1997	Flash Memory Having Segmented Array for Improved Operation
5,583,808	1996	EPROM Array Segmented for High Performance and Method for Controlling Same
5,457,652	1995	Low Voltage EEPROM
5,341,342	1994	Flash Memory Cell Structure
5,016,217	1991	Logic Cell Array Using CMOS EPROM Cells Having Reduced Chip Surface Area
4,910,471	1990	CMOS Ring Oscillator Having Frequency Independent of Supply Voltage (this is the only patent involving a second inventor)
4,885,719	1989	Improved Logic Cell Array Using CMOS EEPROM Cells
4,831,589	1989	EEPROM Programming Switch Operable at Low VCC
4,823,317	1989	EEPROM Programming Switch
4,460,979	1984	Memory Cell
4,442,481	1984	Low Power Decoder Circuit

EDUCATION & CERTIFICATIONS:

Year	College/University	Degree
1978	University of Cincinnati, Ohio (USA)	M. S. Electrical Engineering
1977	Gujarat University, India	M. Sc. Physics, specialization in Solid State Physics & Electronics
1993	Small Company Management, Stanford Univ	Certificate
1994	Marketing Management, Stanford University	Certificate
1995	Marketing Excellence, Univ of London, Canada	Certificate
2007	Certified Trained Nanotechnologist California Institute of Nanotechnology	Certificate
2010	Certified Green Building Professional	Certificate
2010	Judicial Council State of California, Registered Language Interpreter – 5 languages.	Certificate & Registered with State
2011	Energy Efficiency Professional (CA Workforce Devl. & San Jose City College)	Certificate

Professional Associations and Achievements:

- Co-Chairman, IEEE Region 6, Central Area
- Current Vice-Chair & former Chair of IEEE SF Bay Area Vehicle Tech. Society
- Received Special IEEE Appreciation Award 2007 & IEEE Outstanding Leadership and Professional Service Award 2008, 2012 and 2020.
- Appointed on State of California's "Blue Ribbon Task Force on Nanotechnology"
- Former President, Silicon Valley Engineering Council
- Past Chairman Economic Development Commission, City of Milpitas
- Member of Consultant Network Silicon Valley (IEEE-CNSV)
- Rotary International Fellowship Award
- Government of India, National Fellowship Award
- Eta-Kappa-Nu (HKN) Member

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