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19 **Pro Hac Applications forthcoming*

20 Attorneys for Plaintiff

21 **IN THE UNITED STATES DISTRICT COURT**
22 **FOR THE SOUTHERN DISTRICT OF CALIFORNIA**

23 BELL SEMICONDUCTOR, LLC
24 Plaintiff,
25 v.
26 QUALCOMM TECHNOLOGIES,
27 INC.
28 Defendant.

Case No. '22CV1526 TWR RBB
ORIGINAL COMPLAINT
JURY TRIAL DEMANDED

1 Plaintiff Bell Semiconductor, LLC (“Bell Semic” or “Plaintiff”) brings this
2 Complaint against Defendant Qualcomm Technologies, Inc. (“Qualcomm”) for
3 infringement of U.S. Patent No. 7,231,626 (“the ’626 patent”). Plaintiff, on personal
4 knowledge of its own acts, and on information and belief as to all others based on
5 investigation, alleges as follows:

6 **SUMMARY OF THE ACTION**

7 1. This is a patent infringement suit relating to Qualcomm’s unauthorized
8 and unlicensed use of the ’626 patent. The circuit design methodologies claimed in the
9 ’626 patent are used by Qualcomm in the production of one or more of its
10 semiconductor chips, 5G RF Transceiver SDR865 device and Snapdragon 665 device
11 (“Qualcomm Accused Products”).

12 2. Traditionally, the process flow for IC design is highly linear, with each phase
13 of the design process depending on the previous steps. Accordingly, when revisions to
14 portions of the physical design are made, as typically happens numerous times during
15 the design process, all the subsequent steps typically need to be redone in their entirety
16 for at least the layer, if not the entire device. This is because regardless of the size or
17 extent of the revision to the physical design, the changes must be merged into a much
18 larger integrated circuit design and then the remaining steps of the design process flow
19 re-run.

20 3. Before the inventions claimed in the ’626 patent, the typical turnaround time
21 for implementing a change to the physical design for cutting edge devices was
22 approximately one week regardless of the size of the change. This is extremely
23 inefficient in most instances where the change relates to only a small fraction of the
24 overall design. See Ex. A at 3:16–18 & Fig. 1.

25 4. The ’626 patent’s inventors solved this problem by defining a window that
26 encloses a change specified by the revision to physical design. The window defines an
27 area that is less than the area of the entire circuit design. Only the nets within that
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1 window are routed pursuant to the revision, leaving the remaining nets in the design
2 unaffected. Then, the results of that incremental routing are inserted into a copy of the
3 original IC design to produce a revised IC design that effects the physical design change
4 without needing to redo the entire process flow.

5 5. Semiconductor devices include different kinds of materials to function as
6 intended. For example, these devices typically include both metal (*i.e.*, conductor) and
7 insulator materials, which are deposited or otherwise processed sequentially in layers
8 to form the final device. These layers—and the interconnects and components formed
9 within them—have gotten much smaller over time, increasing the performance of these
10 devices dramatically. As a result, it has become even more important to keep the layers
11 planar as the device is being built because defects and warpage can cause fabrication
12 issues and malfunctioning of the device. Manufacturers use a process called Chemical
13 Mechanical Planarization/Polishing (“CMP”) to smooth out the surface of the device to
14 prepare the device for further processing, such as deposition of another layer. This
15 allows subsequent layers to be built and connected more easily with fewer opportunities
16 for short circuits or other errors that render the device defective. CMP functions best
17 when there is a certain density and variance of the same material on the surface of the
18 chip. This is because different materials will be “polished” away at different rates,
19 leading to erosion or dishing on the surface. To reduce this problem “dummy” material,
20 also known as “dummy fill,” is typically inserted into low-density regions of the device
21 to increase the overall uniformity of the structures on the surface of the layer and reduce
22 the density variability across the surface of the device. However, dummy fill can
23 increase capacitance if it is placed too close to signal wires, which slows the
24 transmission speed of signals and degrades the overall performance of the device.

25 6. Bell Semic brings this action to put a stop to Qualcomm’s unauthorized and
26 unlicensed use of the inventions claimed in the ’626 patent.

THE PARTIES

1
2 7. Plaintiff Bell Semic is a limited liability company organized under the
3 laws of the State of Delaware with a place of business at One West Broad Street, Suite
4 901, Bethlehem, PA 18018.

5 8. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs
6 sprung out of the Bell System as a research and development laboratory, and eventually
7 became known as one of America’s greatest technology incubators. Bell Labs
8 employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely
9 considered one of the most important technological breakthroughs of the time, earning
10 the inventors the Nobel Prize in Physics. Bell Labs made the first commercial
11 transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its
12 transistor patents to companies throughout the world, creating a technological boom
13 that led to the use of transistors in the semiconductor devices prevalent in most
14 electronic devices today.

15 9. Bell Semic, a successor to Bell Labs’ pioneering efforts, owns over 1,900
16 worldwide patents and applications, approximately 1,500 of which are active United
17 States patents. This patent portfolio of semiconductor-related inventions was
18 developed over many years by some of the world’s leading semiconductor companies,
19 including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI
20 Corporation (“LSI”). This portfolio reflects technology that underlies many important
21 innovations in the development of semiconductors and integrated circuits for high-tech
22 products, including smartphones, computers, wearables, digital signal processors, IoT
23 devices, automobiles, broadband carrier access, switches, network processors, and
24 wireless connectors.

25 10. The principals of Bell Semic all worked at Bell Labs’ Allentown facility,
26 and have continued the rich tradition of innovating, licensing, and helping the industry
27 at large since those early days at Bell Labs. For example, Bell Semic’s CTO was a LSI
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1 Fellow and Broadcom Fellow. He is known throughout the world as an innovator with
2 more than 300 patents to his name, and he has a sterling reputation for helping
3 semiconductor fabs improve their efficiency. Bell Semic’s CEO took a brief hiatus from
4 the semiconductor world to work with Nortel Networks in the telecom industry during
5 its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees
6 and employees. In addition, several Bell Semic executives previously served as
7 engineers at many of these companies and were personally involved in creating the
8 ideas claimed throughout Bell Semic’s extensive patent portfolio.

9 11. On information and belief, Qualcomm has its principal place of business
10 and headquarters at 5775 Morehouse Drive, San Diego, CA 92121.

11 12. On information and belief, Qualcomm develops, designs, and/or
12 manufactures products in the United States, including in this District, according to the
13 ’626 patented processes/methodologies; and/or uses the ’626 patented
14 processes/methodologies in the United States, including in this District, to make
15 products; and/or distributes, markets, sells, or offers to sell in the United States and/or
16 imports products into the United States, including in this District, that were
17 manufactured or otherwise produced using the patented process. Additionally,
18 Qualcomm introduces those products into the stream of commerce knowing that they
19 will be sold and/or used in this District and elsewhere in the United States.

20 **JURISDICTION AND VENUE**

21 13. This is an action for patent infringement arising under the Patent Laws of
22 the United States, Title 35 of the United States Code. Accordingly, this Court has
23 subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

24 14. This Court has personal jurisdiction over Qualcomm under the laws of the
25 State of California, due at least to its substantial business in California and in this
26 District. Qualcomm has purposefully and voluntarily availed itself of the privileges of
27 conducting business in the United States, in the State of California, and in this District
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1 by continuously and systematically placing goods into the stream of commerce through
2 an established distribution channel with the expectation that they will be purchased by
3 consumers in this District. In the State of California and in this District, Qualcomm,
4 directly or through intermediaries: (i) performs at least a portion of the infringements
5 alleged herein; (ii) develops, designs, and/or manufactures products according to the
6 '626 patented process/methodology; (iii) distributes, markets, sells, or offers to sell
7 products formed according to the '626 patented process/methodology; and/or (iv)
8 imports products formed according to the '626 patented processes/methodologies.

9 15. On information and belief, venue is proper in this Court pursuant to 28
10 U.S.C. §§ 1391 and 1400 because Qualcomm has committed, and continues to commit,
11 acts of infringement in this District and has a regular and established place of business
12 in this District. For example, Qualcomm maintains a regular and established place of
13 business in the District at 5775 Morehouse Drive, San Diego, CA 92121.

14 16. On information and belief, Qualcomm maintains a campus located in San
15 Diego that consists of 36 buildings, 25,000 employees, and that spans hundreds of
16 acres of land. *See This Corporate Campus is Now a Mini Smart City*, Fast Company
17 (available at <https://www.fastcompany.com/90583927/this-corporate-campus-is-now-a-mini-smartcity#:~:text=With%2036%20buildings%2C%2025%2C000%20employees%2C%20and%20hundreds%20of,technologies%20aimed%20at%20making%20spaces%20and%20cities%20smarter>) (last visited August 18, 2022).

22 17. In addition to the foregoing, Qualcomm has numerous other regular and
23 established physical places of business in the District. More specifically, 32 of
24 Qualcomm's 70 United States offices are located in this District. *See 70 Offices in*
25 *USA*, Qualcomm (available at
26 <https://www.qualcomm.com/company/facilities/offices?country=USA&page=3>) (last
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1 visited October 4, 2022). For example, Qualcomm has offices at the following
2 locations, each of which are located within the District:

3	10555 Sorrento Valley Rd.	9685 Scranton Rd.
4	San Diego, CA 92121-1608	San Diego, CA 92121-1761
5	9950 Barnes Canyon Rd.	10145 Pacific Heights Blvd
6	San Diego, CA 92121-2720	San Diego, CA 92121
7	9393 Waples St.	5855 Pacific Center Blvd.
8	Ste. 150	San Diego, CA 92121
9	San Diego, CA 92121	
10	10160 Pacific Mesa Blvd.	10105 Pacific Heights Blvd.
11	San Diego, CA 92121	San Diego, CA 92121
12	10001 Pacific Heights Blvd.	10155 Pacific Heights Blvd.
13	San Diego, CA 92121	San Diego, CA 92121
14	4243 Campus Point Ct.	5770 Morehouse Dr.
15	San Diego, CA 92121-1513	San Diego, CA 92121
16	9325 Sky Park Court	9380 Waples St.
17	Ste. 360	Ste. 102-103
18	San Diego, CA 92123	San Diego, CA 92121-3905
19	5745 Pacific Center Blvd.	10445 Pacific Center Court
20	San Diego, CA 92121	San Diego, CA 92121
21	5525 Morehouse Dr.	5545 Morehouse Dr.
22	San Diego, CA 92121-1710	San Diego, CA 92121-1710
23	5555 Morehouse Dr.	6455 Lusk Blvd.
24	San Diego, CA 92121-1710	San Diego, CA 92121-2779
25	10190 McKellar Court	5665 Morehouse Dr.
26	San Diego, CA 92121	San Diego, CA 92121-1714
27	10185 McKellar Ct.	5535 Morehouse Dr.
28	San Diego, CA 92121-4233	San Diego, CA 92121-1710

1 5565 Morehouse Dr.
San Diego CA 92121-1710

5751 Pacific Center Blvd.
San Diego, CA 92121-4203

2
3 5788 Pacific Center Blvd.
San Diego, CA 92121-4202

5808 Pacific Center Blvd.
San Diego, CA 92121-4202

4
5 5828 Pacific Center Blvd.
San Diego, CA 92121-4202

5737 Pacific Center Blvd.
San Diego, CA 92121

6
7 18. Currently, Qualcomm is advertising 217 jobs in the San Diego-metro area.
8 These positions include those that relate to the '626 patented technologies, such as
9 positions for a Component Engineer and Design Verification Engineer. *See Transform*
10 *Your Future*, Qualcomm ([https://qualcomm.wd5.myworkdayjobs.com/en-](https://qualcomm.wd5.myworkdayjobs.com/en-US/External)
11 [US/External](https://qualcomm.wd5.myworkdayjobs.com/en-US/External)) (last visited October 4, 2022).

12 19. Venue is also convenient in this District. This is at least true because of
13 this District's close ties to this case—including the technology, relevant witnesses, and
14 sources of proof noted above—and its ability to quickly and efficiently move this case
15 to resolution.

16 20. On information and belief, Bell Semic's cause of action arises directly
17 from Qualcomm's circuit design work and other activities in this District. Moreover,
18 on information and belief, Qualcomm has derived substantial revenues from its
19 infringing acts occurring within the State of California and within this District.

20 **U.S. PATENT NO. 7,231,626**

21 21. Bell Semiconductor owns by assignment the entire right, title, and interest
22 in the '626 patent, entitled "Method Of Implementing An Engineering Change Order
23 In An Integrated Circuit Design By Windows."

24 22. A true and correct copy of the '626 patent is attached as Exhibit A.

25 23. The '626 patent issued to inventors Jason K. Hoff, Viswanathan
26 Lakshmanan, Michael Josephides, Daniel W. Prevedel, Richard D. Blinne, and
27 Johathan P. Kuppinger.

1 24. The application that resulted in issuance of the '626 patent, United States
2 Patent Application No. 11/015,123, was filed December 17, 2004. It issued on June 12,
3 2007 and expires on July 26, 2025.

4 25. The '626 patent generally relates to “methods of implementing an
5 engineering change order (ECO) in an integrated circuit design.” Ex. A at 1:1–13.

6 26. The background section of the '626 patent identifies the shortcomings of
7 the prior art. More specifically, the specification describes that the prior circuit design
8 methodology was disadvantageous because “[i]n previous methods for implementing
9 an engineering change order (ECO) request in an integrated circuit design, design tools
10 are run for the entire integrated circuit design, even though the engineering change
11 order typically is only a small fraction of the size of the integrated circuit design” Ex.
12 A at 2:15–19.

13 27. The '626 patent elaborates that because “cell placement, routing, design
14 rule check validation, and timing closure run times typically scale with the size of the
15 entire integrated circuit design,” Ex. A at 2:20–22, this produced a “typical turnaround
16 time” of “about one week regardless of the size of the engineering change order. . . .
17 because although the engineering change order may only have a size of a few cells, it
18 must be merged with an integrated circuit design that typically has a much greater size.”
19 *Id.* at 2:37–44. Certain of these steps “may be especially time consuming and resource
20 intensive.” *Id.* at 3:16–17.

21 28. The inventions disclosed in the '626 patent provide many advantages over
22 the prior art. In particular, they provide a simple and efficient method for ensuring that
23 revisions to the physical design of the IC do not unduly delay the completion of the
24 design process. As the '626 patent explains, “significant savings in the resources
25 required to perform routing, design rule check verification, net delay calculation, and
26 parasitic extraction may be realized by creating windows in the integrated circuit design
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1 that include only the incremental changes to the overall integrated circuit design.” Ex.
2 A at 3:19–23.

3 29. As mentioned above, this is very beneficial because it substantially
4 reduces the run time of the routing tools and related follow-on steps of the layout
5 portion of the design process flow (such as calculation of net delay, design rule check,
6 and parasitic extraction). Thus, it shortens the overall design timeline, and avoids cost
7 overruns and delays, making it less costly to make changes later in the design process
8 or more often. *See id.*

9 30. Given the aforementioned increased complexity of circuit designs and the
10 corresponding delays from design changes, these efficiency gains have become more
11 and more important in completing the design process without affecting time-to-market.
12 These significant advantages are achieved through the use of the patented inventions
13 and thus the ’626 patent presents significant commercial value for chip designers.

14 31. In light of the drawbacks of the prior art, the ’626 patent’s inventors
15 recognized the need for a circuit design methodology in which the time required to
16 implement an ECO “depend[s] on the number of net changes in the [ECO] rather than
17 on the total number of nets in the entire integrated circuit design.” Ex. A at 2:51–53.
18 The inventions claimed in the ’626 patent address this need.

19 32. The ’626 patent contains two independent claims and 8 total claims,
20 covering a method and computer readable medium for implementing a change order in
21 an integrated circuit design. Claim 1 reads:

22 1. A method comprising steps of:

23 (a) receiving as input an integrated circuit design;

24 (b) receiving as input an engineering change order to the integrated
25 circuit design;

26 (c) creating at least one window in the integrated circuit design that
27 encloses a change to the integrated circuit design introduced by the
28

1 engineering change order wherein the window is bounded by
2 coordinates that define an area that is less than an entire area of the
integrated circuit design;

3 (d) performing an incremental routing of the integrated circuit
4 design only for each net in the integrated circuit design that is
5 enclosed by the window;

6 (e) replacing an area in a copy of the integrated circuit design that
7 is bounded by the coordinates of the window with results of the
8 incremental routing to generate a revised integrated circuit design;
and

9 (f) generating as output the revised integrated circuit design.

10 33. This claim, as a whole, provides significant benefits and improvements to
11 the function of the semiconductor device design process, *e.g.*, providing a novel and
12 substantially more efficient process flow in which only the affected nets would be
13 considered in the incremental routing. This results in substantial reduction in the
14 expected time of the design portion of producing semiconductor devices.

15 34. The claims of the '626 patent also recite inventive concepts that improve
16 the functioning of the fabrication process, particularly as to post-ECO routing. The
17 claims of the '626 patent disclose a new and novel solution to specific problems related
18 to improving semiconductor fabrication. As explained in detail above and in the '626
19 patent specification, the claimed inventions improve upon the prior art processes by
20 ignoring nets that are unaffected by an ECO in performing routing following the ECO.
21 This has the advantage of substantially reducing the impact on design schedule of ECOs
22 and other layout changes, thus increasing the efficiency of the design process and
23 making it easier to improve the design and fix design errors without unduly delaying
24 time-to-market. By making it easier to fix errors as they are found, and causing
25 substantially less incremental delay upon finding and fixing errors, the claimed
26 inventive processes also increase the performance and reliability of the finished
27 product. Because of the claimed inventive processes, individual less impactful design
28

1 issues that still impact design performance (albeit not on a critical scale) can be caught
2 and fixed without costing the same delay as more substantial errors.

3 **COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,231,626**

4 35. Bell Semic re-alleges and incorporates by reference the allegations of the
5 foregoing paragraphs as if fully set forth herein.

6 36. The '626 patent is valid and enforceable under the United States Patent
7 Laws.

8 37. Bell Semic owns, by assignment, all right, title, and interest in and to the
9 '626 patent, including the right to collect for past damages.

10 38. A copy of the '626 patent is attached at Exhibit A.

11 39. On information and belief, Qualcomm has and continues to directly
12 infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the '626 patent by using
13 the patented methodology to design one or more semiconductor devices, including as
14 one example the Qualcomm Accused Products, in the United States.

15 40. On information and belief, Qualcomm employs a variety of design tools,
16 for example, Cadence, Synopsys, and/or Siemens tools, to perform incremental routing
17 in implementing an ECO (the "Accused Processes") as recited in the '626 patent claims.
18 As one example, Qualcomm's Accused Processes perform a method for only routing
19 the nets affected by the ECO and merging that changed area into the overall circuit
20 layout as required by claim 1 of the '626 patent. Qualcomm does so by employing a
21 design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to
22 perform incremental routing as part of implementing an ECO for the Qualcomm
23 Accused Products to generate a revised integrated circuit design.

24 41. Qualcomm's Accused Processes also calculate and perform a parasitic
25 extraction only for each net in the IC design enclosed by the window defining the ECO.
26 (This parasitic extraction is also how the Accused Processes further calculate a net delay
27 only for each net in the IC design enclosed by the window defining the ECO.)
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1 Qualcomm does so by employing a design tool, such as at least one of the Cadence,
2 Synopsys, and/or Siemens tools, to perform the incremental routing during
3 implementation of the ECO for the Qualcomm Accused Products' circuit designs.

4 42. Qualcomm's Accused Processes also perform a design rule check only for
5 each net in the IC design enclosed by the ECO window. Qualcomm does so by
6 employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens
7 tools, perform the incremental ECO and automatically perform a DRC for those nets to
8 ensure that the ECO did not violate any design rules when it fixed other issues.

9 43. An exemplary infringement analysis showing infringement of one or more
10 claims of the '626 patent is set forth in Exhibit B. The declaration of Lloyd Linder, an
11 expert in the field of semiconductor device design, is attached at Exhibit C and further
12 describes Qualcomm's infringement of the '626 patent.

13 44. Qualcomm's Accused Processes infringe and continue to infringe one or
14 more claims of the '626 patent during the pendency of the '626 patent.

15 45. On information and belief, Qualcomm has and continues to infringe
16 pursuant to 35 U.S.C. § 271, *et. seq.*, directly or indirectly, either literally or under the
17 doctrine of equivalents, by using the Accused Processes in violation of one or more
18 claims of the '626 patent. Qualcomm has and continues to infringe pursuant to 35
19 U.S.C. § 271, *et. seq.*, directly or indirectly, either literally or under the doctrine of
20 equivalents, by making, selling, or offering to sell in the United States, or importing
21 into the United States products manufactured or otherwise produced using the Accused
22 Processes in violation of one or more claims of the '626 patent.

23 46. Qualcomm's infringement of the '626 patent is exceptional and entitles
24 Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35
25 U.S.C. § 285.

26 47. Bell Semic has been damaged by Qualcomm's infringement of the '626
27 patent and will continue to be damaged unless Qualcomm is enjoined by this Court.

1 Bell Semic has suffered and continues to suffer irreparable injury for which there is no
2 adequate remedy at law. The balance of hardships favors Bell Semic, and public interest
3 is not disserved by an injunction.

4 48. Bell Semic is entitled to recover from Qualcomm all damages that Bell
5 Semic has sustained as a result of Qualcomm's infringement of the '626 patent,
6 including without limitation and/or not less than a reasonable royalty

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PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

- (a) a judgment declaring that Qualcomm has infringed one or more claims of the '626 patent in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;
- (b) an award of damages adequate to compensate Bell Semic for infringement of the '626 patent by Qualcomm, in an amount to be proven at trial, including supplemental post-verdict damages until such time as Qualcomm ceases its infringing conduct;
- (c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting Qualcomm and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with Qualcomm, from committing further acts of infringement;
- (d) a judgment requiring Qualcomm to make an accounting of damages resulting from Infineon's infringement of the '626 patent;
- (e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;
- (f) pre-judgment and post-judgment interest at the maximum amount permitted by law;
- (g) all other relief, in law or equity, to which Bell Semic is entitled.

1 Dated: October 6, 2022

/s/ James J. Yukevich, Esq.

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**Pro Hac Vice Applications forthcoming*

*Attorneys for Plaintiff Bell Semiconductor,
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DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: October 6, 2022

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