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14 **Pro Hac Vice application forthcoming*

15 Attorneys for Plaintiff

16
17 **IN THE UNITED STATES DISTRICT COURT**
18 **FOR THE SOUTHERN DISTRICT OF CALIFORNIA**
19

20 BELL SEMICONDUCTOR, LLC
21 Plaintiff,
22 v.
23 NXP USA, INC.
24 Defendant.

Case No. '22CV1794 BEN RBB
ORIGINAL COMPLAINT
JURY TRIAL DEMANDED

1 Plaintiff Bell Semiconductor, LLC (“Bell Semic” or “Plaintiff”) brings this
2 Complaint against Defendant NXP USA, Inc. (“NXP”) for infringement of U.S. Patent
3 No. 7,396,760 (“the ’760 patent”). Plaintiff, on personal knowledge of its own acts, and
4 on information and belief as to all others based on investigation, alleges as follows:

5 **SUMMARY OF THE ACTION**

6 1. This is a patent infringement suit relating to NXP’s unauthorized and
7 unlicensed use of the ’760 patent. The circuit design methodologies claimed in the ’760
8 patent are used by NXP in the production of one or more of its semiconductor chips,
9 including at least the NXP LS1043A Quad-Core Networking Processor devices (“NXP
10 Accused Product”).

11 2. Traditionally, the process flow for IC design is highly linear, with each
12 phase of the design process depending on the previous steps. Accordingly, when
13 revisions to portions of the physical design are made, as typically happens numerous
14 times during the design process, all the subsequent steps typically need to be redone in
15 their entirety for at least the layer, if not the entire device. This is because regardless of
16 the size or extent of the revision to the physical design, the changes must be merged
17 into a much larger integrated circuit design and then the remaining steps of the design
18 process flow re-run.

19 3. Semiconductor devices include different kinds of materials to function as
20 intended. For example, these devices typically include both metal (i.e., conductor) and
21 insulator materials, which are deposited or otherwise processed sequentially in layers
22 to form the final device. These layers—and the interconnects and components formed
23 within them—have gotten much smaller over time, increasing the performance of these
24 devices dramatically. As a result, it has become even more important to keep the layers
25 planar as the device is being built because defects and warpage can cause fabrication
26 issues and malfunctioning of the device.

1 4. Manufacturers use a process called Chemical Mechanical
2 Planarization/Polishing (“CMP”) to smooth out the surface of the device to prepare the
3 device for further processing, such as deposition of another layer. This allows
4 subsequent layers to be built and connected more easily with fewer opportunities for
5 short circuits or other errors that render the device defective. CMP functions best when
6 there is a certain density and variance of the same material on the surface of the chip.
7 This is because different materials will be “polished” away at different rates, leading to
8 erosion or dishing on the surface.

9 5. To reduce this problem “dummy” material, also known as “dummy fill,”
10 is typically inserted into low-density regions of the device to increase the overall
11 uniformity of the structures on the surface of the layer and reduce the density variability
12 across the surface of the device. However, dummy fill can increase capacitance if it is
13 placed too close to signal wires, which slows the transmission speed of signals and
14 degrades the overall performance of the device.

15 6. Just as unwanted capacitance can result from the interaction of elements
16 within the layer of an integrated circuit, it can also result from interaction of elements
17 across adjacent layers. While certain elements (such as signal lines and power lines)
18 cannot be easily moved without affecting circuit performance, there is substantially
19 more flexibility regarding placement, positioning, and spacing of non-signal carrying
20 features such as dummy fill, even when certain quantities of dummy fill are needed
21 within layers and portions of layers to meet processing requirements.

22 7. Prior to development of the methodology described in the ’760 patent, the
23 placement of dummy fill in the open areas of the interconnect layer was performed
24 based primarily upon meeting density requirements. To the extent that timing and
25 capacitance effects were considered in dummy fill dimensions, orientation, positioning,
26 or otherwise in dummy fill placement, the conventional dummy fill tools at the time
27 only considered intralayer effects—i.e., interactions between dummy fill features and
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1 other elements (such as signal nets) on that same layer. However, use of dummy fill
2 that overlapped on successive layers could and often did create a substantial interlayer
3 bulk capacitive effect that had a negative impact on circuit timing and performance,
4 and which was not considered by the conventional dummy fill tools at the time even
5 when they considered certain intralayer timing effects. *See* Ex. A at 1:43–2:6, 4:11–16.

6 8. Recognizing these drawbacks, as well as the importance of having a flat
7 or planarized surface on the devices, the inventors of the '760 patent set out to develop
8 a design process that would also consider the interlayer bulk capacitance created by
9 overlapping dummy fill and consider those intralayer effects in arranging dummy fill
10 in the chip layout so as to minimize the unwanted bulk capacitance created by
11 overlapping dummy fill features.

12 9. The inventors of the '760 patent ultimately conceived of a method for
13 addressing the interlayer capacitive effects of dummy fill by treating each successive
14 set of layers as a pair and then rearranging the dummy fill in one or both layers so as to
15 minimize their overlap. This was particularly advantageous in “intelligent dummy fill
16 placement,” i.e., when timing impact is considered when placing dummy fill. *See* Ex.
17 A at 2:10–19.

18 10. The inventions disclosed in the '760 patent provide many advantages over
19 the prior art. In particular, rearranging the dummy fill features such that they do not
20 align vertically in successive layers can reduce unwanted bulk capacitance introduced
21 by dummy fill and thus minimize the interlayer capacitance. *See* Ex. A at 2:45–48,
22 2:47–59, 3:30–33, 5:19–39. This removed unwanted bulk capacitance that would
23 otherwise slow down signals in the circuit and adversely affect timing in the IC, thus
24 improving its speed and performance. *See* Ex. A at 2:3–6. These significant advantages
25 are achieved through the use of the patented inventions and thus the '760 patent presents
26 significant commercial value for companies like NXP.

1 11. Bell Semic brings this action to put a stop to NXP’s unauthorized and
2 unlicensed use of the inventions claimed in the ’760 patent.

3 **THE PARTIES**

4 12. Plaintiff Bell Semic is a limited liability company organized under the
5 laws of the State of Delaware with a place of business at One West Broad Street, Suite
6 901, Bethlehem, PA 18018.

7 13. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs
8 sprung out of the Bell System as a research and development laboratory, and eventually
9 became known as one of America’s greatest technology incubators. Bell Labs
10 employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely
11 considered one of the most important technological breakthroughs of the time, earning
12 the inventors the Nobel Prize in Physics. Bell Labs made the first commercial
13 transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its
14 transistor patents to companies throughout the world, creating a technological boom
15 that led to the use of transistors in the semiconductor devices prevalent in most
16 electronic devices today.

17 14. Bell Semic, a successor to Bell Labs’ pioneering efforts, owns over 1,900
18 worldwide patents and applications, approximately 1,500 of which are active United
19 States patents. This patent portfolio of semiconductor-related inventions was
20 developed over many years by some of the world’s leading semiconductor companies,
21 including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI
22 Corporation (“LSI”). This portfolio reflects technology that underlies many important
23 innovations in the development of semiconductors and integrated circuits for high-tech
24 products, including smartphones, computers, wearables, digital signal processors, IoT
25 devices, automobiles, broadband carrier access, switches, network processors, and
26 wireless connectors.

1 19. This Court has personal jurisdiction over NXP under the laws of the State
2 of California, due at least to its substantial business in California and in this District.
3 NXP has purposefully and voluntarily availed itself of the privileges of conducting
4 business in the United States, in the State of California, and in this District by
5 continuously and systematically placing goods into the stream of commerce through an
6 established distribution channel with the expectation that they will be purchased by
7 consumers in this District. In the State of California and in this District, NXP, directly:
8 (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs,
9 and/or manufactures products according to the '760 patented process/methodology; (iii)
10 distributes, markets, sells, or offers to sell products formed according to the '760
11 patented process/methodology; and/or (iv) imports products formed according to the
12 '760 patented process/methodology.

13 20. On information and belief, venue is proper in this Court pursuant to 28
14 U.S.C. §§ 1391 and 1400 because NXP has committed, and continues to commit, acts
15 of infringement in this District and has a regular and established place of business in
16 this District. For example, NXP maintains a regular and established place of business
17 in the District at Innovation Drive, Suite 150, San Diego, CA 92128. On information
18 and belief, NXP current employs more than 75 engineers in the San Diego area. *See*
19 *Search Results for Current NXP Employees, LinkedIn* (available at
20 https://www.linkedin.com/search/results/people/?currentCompany=%5B%221088%22%5D&geoUrn=%5B%22103918656%22%2C%2290010472%22%5D&keywords=engineer&origin=FACETED_SEARCH&sid=or8) (last visited November 4, 2022).

23 21. Currently, on information and belief, NXP is advertising 20 jobs in the San
24 Diego area. These positions include those that relate to the '760 patented technologies,
25 such as positions for a Senior Principal Physical Design Engineer, SoC Hardware
26 Architect, and Entry Level Design, Verification, and Validation Engineer. *See NXP Job*
27 *Listings,* NXP

1 (https://nxp.wd3.myworkdayjobs.com/careers?Location_Country=bc33aa3152ec42d4
2 995f4791a106ed09&locations=98d67abaaa8a100fa6344859d7d49369) (last visited
3 November 4, 2022).

4 22. Venue is also convenient in this District. This is at least true because of
5 this District’s close ties to this case—including the technology, relevant witnesses, and
6 sources of proof noted above—and its ability to quickly and efficiently move this case
7 to resolution.

8 23. On information and belief, Bell Semic’s cause of action arises directly
9 from NXP’s circuit design work and other activities in this District. Moreover, on
10 information and belief, NXP has derived substantial revenues from its infringing acts
11 occurring within the State of California and within this District.

12 **U.S. PATENT NO. 7,396,760**

13 24. Bell Semic is the owner by assignment of the ’760 patent. The ’760 patent
14 is titled “Method and System for Reducing Inter-Layer Capacitance in Integrated
15 Circuits.”

16 25. A true and correct copy of the ’760 patent is attached as Exhibit A.

17 26. The inventors of the ’760 patent are Kunal Taravade, Neal Callan, and
18 Paul Filseth.

19 27. The ’760 patent issued on July 8, 2008 from an application filed on
20 November 17, 2004.

21 28. The ’760 patent generally relates to “a method for reducing inter-layer
22 capacitance” in integrated circuits “through dummy fill methodology.” Ex. A at 1:8–
23 10.

24 29. The background section of the ’760 patent identifies the shortcomings of
25 the prior art. More specifically, the specification describes that the prior dummy fill
26 methodologies were disadvantageous because they typically focused on achieving
27 uniformity of feature density and failed to sufficiently address adverse effects of the
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1 dummy fill on electric field and unwanted bulk capacitance. *See* Ex. A at 1:62–66. In
2 addition, these dummy fill methodologies only considered intralayer effects of dummy
3 fill, to the extent that they considered timing impact at all. *See* Ex. A at 1:66–2:3. Thus,
4 placement of dummy fill, even if advantageous on each individual layer, could create
5 problems when it overlapped with dummy fill features on successive layers, introducing
6 an additional bulk capacitance component that could be substantial. *See id.* at 4:11–17,
7 4:25–28. These methodologies failed to consider interlayer effects such as those caused
8 by the overlap of dummy fill features in successive layers, which could have a
9 substantial negative impact on timing. *See id.* at 2:3–6.

10 30. In light of the drawbacks of the prior art, the inventors of the '760 patent
11 recognized a need for “intelligent dummy fill placement to reduce interlayer
12 capacitance caused by overlaps of dummy fill area on successive layers,” which would
13 also “treat[] each consecutive pair of layers together when the intelligent dummy filling
14 placement is performed.” Ex. A at 2:7–13. The inventions claimed in the '760 patent
15 address this need.

16 31. The '760 patent contains two independent claims and 19 total claims.

17 Claim 1 reads:

18 1. A method for placing dummy fill patterns in an integrated circuit
fabrication process, comprising:

19 obtaining layout information of the integrated circuit, the integrated
20 circuit including a plurality of layers;

21 obtaining a first dummy fill space for a first layer based on the
layout information;

22 obtaining a second dummy fill space for a second layer, the second
23 layer being placed successively to the first layer;

24 determining an overlap between the first dummy fill space and the
second dummy fill space; and

25 minimizing the overlap by re-arranging a plurality of first dummy
26 fill features and a plurality of second dummy fill features,

27 wherein the first dummy fill space includes non-signal carrying
28 lines on the first layer and the second dummy fill space includes
non-signal carrying lines on the second layer.

1 32. This claim, as a whole, provides significant benefits and improvements to
2 the function of the semiconductor device, *e.g.*, minimizing interlayer bulk capacitance
3 and thus improving the timing characteristics and performance of the IC while meeting
4 interconnect density requirements during processing. *See, e.g.*, Ex. A at 1:37–55, 5:19–
5 39.

6 33. The claims of the '760 patent also recite inventive concepts that improve
7 the functioning of the fabrication process, particularly as to dummy filling. The claims
8 of the '760 patent disclose a new and novel solution to specific problems related to
9 improving semiconductor fabrication. As explained in detail above and in the '760
10 patent specification, the claimed inventions improve upon the prior art processes by
11 considering successive layers rather than each layer on its own, and then determining
12 the overlap between dummy fill features on successive layers before rearranging them
13 to minimize their overlap and thus reduce interlayer bulk capacitance. This has
14 advantages such as minimizing the parasitic capacitance of the interconnect layers,
15 especially the bulk capacitance contributed by the interlayer effects of overlapping
16 dummy fill features, while maintaining necessary interconnect density to meet
17 fabrication requirements.

18 **COUNT I – INFRINGEMENT OF U.S. PATENT NO. 6,436,807**

19 34. Bell Semic re-alleges and incorporates by reference the allegations of the
20 foregoing paragraphs as if fully set forth herein.

21 35. The '760 patent is valid and enforceable under the United States Patent
22 Laws.

23 36. Bell Semic owns, by assignment, all right, title, and interest in and to the
24 '760 patent, including the right to collect for past damages.

25 37. A copy of the '760 patent is attached at Exhibit A.

26 38. On information and belief, NXP has and continues to directly infringe
27 pursuant to 35 U.S.C. § 271(a) one or more claims of the '760 patent by using the
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1 patented methodology to design one or more semiconductor devices, including as one
2 example the NXP Accused Product, in the United States.

3 39. On information and belief, NXP employs a variety of design tools, for
4 example, Cadence, Synopsys, and/or Siemens tools, to make a layout for an
5 interconnect layer of a semiconductor device (the “Accused Processes”) as recited in
6 the ’807 patent claims. As one example, NXP’s Accused Processes allow arrangement
7 and rearrangement of dummy fill in a timing aware fashion, including with the ability
8 to stagger the dummy fill in successive layers so as to minimize the interlayer bulk
9 capacitance after determining their overlap as required by claim 1 of the ’760 patent.
10 NXP does so by employing a design tool, such as at least one of a Cadence, Synopsys,
11 and/or Siemens tool, rearrange the dummy fill features in successive layers of its
12 Accused Product.

13 40. NXP’s Accused Processes also form the dummy fill features in a grid
14 within one or more of the successive layers, provide square-shaped dummy fill features
15 in one or more of the successive layers, determine the dummy fill space based on a local
16 pattern density in one or more of the successive layers, and minimize total bulk
17 capacitance and/or certain of its components. NXP does so by employing a design tool,
18 such as at least one of the Cadence, Synopsys, and/or Siemens tools, to implement
19 dummy fill functionality in a timing-aware fashion and with consideration of interlayer
20 capacitive effects in creation and design of its Accused Product.

21 41. An exemplary infringement analysis showing infringement of one or more
22 claims of the ’760 patent is set forth in Exhibit B. The declaration of Dhaval
23 Brahmhatt, an expert in the field of semiconductor device design, is attached at Exhibit
24 C and further describes NXP’s infringement of the ’760 patent.

25 42. NXP’s Accused Processes infringe and continue to infringe one or more
26 claims of the ’807 patent during the pendency of the ’760 patent.

- (c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting NXP and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with NXP, from committing further acts of infringement;
- (d) a judgment requiring NXP to make an accounting of damages resulting from Infineon’s infringement of the ’760 patent;
- (e) the costs of this action, as well as attorneys’ fees as provided by 35 U.S.C. § 285;
- (f) pre-judgment and post-judgment interest at the maximum amount permitted by law;
- (g) all other relief, in law or equity, to which Bell Semic is entitled.

Dated: November 15, 2022

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**Pro Hac Vice application forthcoming*

Attorneys for Plaintiff Bell Semiconductor, LLC

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: November 15, 2022

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