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YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD., Plaintiff, v. MICRON TECHNOLOGY, INC., and MICRON CONSUMER PRODUCTS GROUP, LLC., Defendants.	Case No. _____ **COMPLAINT FOR PATENT INFRINGEMENT** DEMAND FOR JURY TRIAL

Plaintiff Yangtze Memory Technologies Company, Ltd. ("YMTC" or "Plaintiff"), by its attorneys Ropes & Gray LLP, as and for its complaint against Defendants Micron Technology, Inc. and Micron Consumer Products Group, LLC, (collectively, "Micron" or "Defendants"), on personal knowledge as to its own actions, and upon information and belief as to all others, alleges as follows:

NATURE OF THE ACTION

1. YMTC is one of the world's most innovative developers and manufacturers of 3D NAND flash memory chips. Although a relative newcomer, YMTC has developed and patented technologies that enable the production of better flash memory chips, having more capacity and a lower per-bit cost. YMTC's innovations have not gone unnoticed. In 2018, for example, YMTC received the award for the Most Innovative Flash Memory Start-up Company from the Flash Memory Summit in Santa Clara, CA, which award "recognizes the most creative and ambitious startup companies and applauds their entrepreneurial journey to becoming a market disruptor and champion of the storage industry."[1] YMTC has continued to innovate and has continued to receive important patents as a result. In 2022, YMTC received the award for Most Innovative Memory Technology for YMTC's Xtacking® 3.0 3D NAND Architecture from the Flash Memory Summit in Santa Clara, CA.[2]

2. No longer an upstart, YMTC has become a key player in the global 3D NAND market. Just the past November, TechInsights Inc., which analyzes and tracks the flash memory market, concluded that "[w]hat YMTC has accomplished has been nothing short of amazing"—YMTC "is now the leader in 3D NAND flash," having "leap-frogged Micron," another major player in the 3D NAND space.[3] Micron is threatened by YMTC's ascension.

3. 3D NAND flash memory is vital technology for many of the digital products that consumers have come to depend upon and enjoy, such as smartphones, laptops, and tablet computers,

[1] *See* Ex. 38 ("Flash Memory Summit 2018 Award Winners")

[2] *See* Ex. 9 ("Flash Memory Summit Announces 2022 Best of Show Award Winners")

[3] *See* Ex. 26 (https://www.techinsights.com/disruptive-event/ymtc-232l-tlc-3d-nand.)

as well as for the data centers and enterprise storage solutions in which 3D NAND is used. Competition and innovation in the NAND memory space inure to the benefit of consumers, as competition and innovation lead to better products at better prices. Attempts to stifle competition and hinder innovation do neither.

4. This action seeks to address one facet of Micron's attempts to hinder competition and innovation via its attempts to force YMTC out of the 3D NAND flash memory market. More specifically, this is an action to put an end to Micron's widespread and unauthorized use of YMTC's patented innovations. Micron has turned to use of YMTC's patented technologies in an effort to fend off competition from YMTC, and to gain and protect market share. And by Micron not paying its fair share to use YMTC's patented inventions, and instead freeriding on YMTC's innovations, Micron robs from the incentive to innovate.

5. In particular, this is an action brought by YMTC against Micron for infringement of United States Patent Nos. 10,950,623 (the "'623 Patent"), 11,501,822 (the "'822 Patent"), 10,658,378 (the "'378 Patent"), 10,937,806 (the "'806 Patent"), 10,861,872 (the "'872 Patent"), 11,468,957 (the "'957 Patent"), 11,600,342 (the "'342 Patent"), and 10,868,031 (the "'031 Patent") (collectively, the "Asserted Patents").

THE PARTIES

6. Plaintiff YMTC is headquartered in China and maintains a principal place of business in Wuhan, China. YMTC maintains a wholly-owned subsidiary, Yangtze Memory Technologies, Inc., which has its principal place of business in Santa Clara, CA, in this judicial District.

7. Upon information and belief, Micron Technology, Inc. is a publicly traded corporation organized under the laws of the State of Delaware, with its principal place of business at 8000 S. Federal Way, Boise, Idaho, 83716. Micron Technology, Inc. may be served with process through its registered agent, CSC – Lawyers Incorporating Service, at 2710 Gateway Oaks Dr., Ste. 150N, Sacramento, CA 95833.

8. Upon information and belief, Micron Consumer Products Group, LLC, is a wholly-owned subsidiary of Micron Technology, Inc., is directed and controlled by Micron Technology, Inc., and is organized under the laws of the State of Delaware, with its principal place of business at 110 Holger Way, San Jose, California, 95134. Micron Consumer Products Group, LLC may be served with process through its registered agent, CSC – Lawyers Incorporating Service, at 2710 Gateway Oaks Dr., Ste. 150N, Sacramento, CA 95833.

9. Defendants have been and are acting in concert, and are otherwise liable jointly, severally, or otherwise for relief related to or arising out of the same transaction, occurrence, or series of transactions or occurrences related to the making, using, selling, offering for sale, or otherwise distributing the Accused Memory Products (as defined below) in this District and elsewhere.

10. In addition, this action involves questions of law and fact that are common to both Defendants. For example, Defendants are making, using, offering for sale, selling, or otherwise distributing at least some of the same Accused Memory Products (as defined below) in this District and elsewhere.

JURISDICTION AND VENUE

11. This action arises under the patent laws of the United States, Title 35 of the United States Code. This Court has original subject matter jurisdiction under 28 U.S.C. §§ 1331 (federal question), and 1338(a) (action arising under an Act of Congress relating to patents).

12. This Court has personal jurisdiction over Micron because, upon information and belief, Micron, directly or through its agents, has regularly conducted business activities in this judicial District and throughout California and this action arises out of and relates to activities that Micron has purposefully directed at this judicial District and California. Micron Technology, Inc., maintains an office at 110 Holder Way, San Jose, California, 95134, within this judicial District.[4] Micron Consumer Products Group, Inc. is a resident of this State and maintains a headquarters office at 110 Holger Way,

[4] Ex. 28 (https://www.micron.com/about/locations?country=USA&city=San%20Jose) ("Micron San Jose").

San Jose, California, 95134.[5]

13. Upon information and belief, Micron has committed acts of infringement within this judicial District and California by, *inter alia*, directly and/or indirectly making, selling, offering for sale, importing, and/or using products that practice (or are made in a manner that practices) one or more claims of the Asserted Patents. Micron, directly and/or through intermediaries, uses, sells, ships, distributes, imports, offers for sale, and/or advertises or otherwise promotes its products throughout the United States, including in this judicial District and California.[6]

14. Micron maintains highly interactive and commercial websites, accessible to residents of this judicial District and California, through which Micron promotes and facilitates sales and use of its products and services, including products that infringe the Asserted Patents.[6]

15. Venue is proper in this judicial District pursuant to 28 U.S.C. §§ 1391 and 1400(b), because Micron has a regular and established place of business in this judicial District, and has committed and continues to commit acts of patent infringement in this judicial District, by, among other things, directly and/or indirectly making, using, selling, offering to sell, or importing products that practice (or are made in a manner that practices) one or more claims of the Asserted Patents.

16. This is an action concerning infringement by Micron with respect to its 3D NAND technologies and products incorporating the same. According to Micron, "Micron's 3D NAND-related design and product engineering occurs . . . in Micron's San Jose and Folsom, California facilities . . . ."[7]

[5] *See* Ex. 29 (Micron Consumer Products Group, Inc., Statement of Information filed with the California Secretary of State); *see also* Ex. 33 (San Jose Mercury news article titled, "Micron opens modern new north San Jose campus amid growth spurt").

[6] *See, e.g.*, Ex. 20 (https://www.micron.com).

[7] Ex. 34 at 2.

DIVISIONAL ASSIGNMENT

17. This case is an Intellectual Property Action under Civil Local Rule 3-2(c) and, pursuant to Civil Local Rule 3-5(b), shall be assigned on a district-wide basis.

YMTC'S INNOVATIONS AND PATENTS

18. YMTC is an integrated device manufacturer (IDM) dedicated to the development of memory products for the global market. With a focus on the design of superior 3D NAND flash memory, YMTC's innovations have gained significant recognition in a short amount of time. YMTC has succeeded in designing and manufacturing 3D NAND flash memory chips with bit densities, I/O speeds, and capacities that are highly praised in the industry. YMTC maintains ties to Silicon Valley through a wholly-owned subsidiary, Yangtze Memory Technologies, Inc., incorporated in California.[8]

19. YMTC's 3D NAND Chips have been recognized as the "Best of Show" for "Most Innovative Flash Memory Start-up Company."[9] In 2018, the Flash Memory Summit held in Santa Clara, CA, recognized YMTC as among "the most creative and ambitious startup companies and applaud[ed] their entrepreneurial journey to becoming a market disruptor and champion of the storage industry."[9] In 2022, the Flash Memory Summit recognized YMTC's Xtacking® 3.0 3D NAND Architecture as the "Most Innovative Memory Technology."[10] The Flash Memory Summit hosts up to 6,000 individuals and companies, including on average 100 global sponsors, and is the largest collection of flash memory experts.[11] YMTC innovations have resulted in "the world's most advanced

[8] *See* Ex. 35 (Yangtze Memory Technologies, Inc. Statement of Information filed with the California Secretary of State); *see also*, Ex. 36 (https://www.ymtc.com/en/contact.html).

[9] Ex. 38; *see also*, Ex. 39 (https://apnews.com/press-release/globe-newswire/technology-business-472edca95b4b227a486f5f8c4750cbb3).

[10] Ex. 9.

[11] *See* Ex. 10 (Flash Memory Summit Sponsor Prospectus); *see also* Ex. 9 (The Flash Memory Summit is "the world's largest event featuring the trends, innovations, and influencers driving the adoption of flash memory in demanding enterprise storage applications, as well as in smartphones, tablets, and mobile and embedded systems.").

3D NAND memory chip in a consumer device," having "the highest bit density seen in a commercially available NAND product."[12]

20. To promote the progress of science and useful arts, and protect its investments in research and development to facilitate further research and development efforts, YMTC has applied for and received numerous patents for its innovations, including many United States patents.

21. YMTC's patented innovations increase the speed, performance, density, reliability, and yield of 3D NAND chips, which in turn facilitate technological improvements in a wide variety of products including not just mobile phones, data centers, and personal computers, but also many types of products requiring memory, such as portable electronic devices and automotive infotainment systems. YMTC's innovations make possible, or improve, many of the electronic devices that consumers depend upon and enjoy.

MICRON'S ACCUSED PRODUCTS AND INFRINGING ACTIVITIES

22. Micron is a global manufacturer and supplier of memory components and devices for use in consumer and enterprise products, systems, and services.

23. Micron designs, makes, uses, sells, offers for sale, imports, supplies, or otherwise distributes into the United States, and provides support for, 96-Layer NAND memory chips and Micron products containing the same (collectively, the "96L Accused Products"), including products with the part or die name or number B27A, and other memory chips (and memory products containing the same) that have the same or similar structures, features, or functionalities, and/or are made by the same or similar manufacturing processes, as the aforementioned exemplary product. An exemplary technical analysis of the B27A is available for purchase at https://www.techinsights.com/products/car-1906-202 and https://www.techinsights.com/products/war-1912-801.

24. Micron designs, makes, uses, sells, offers for sale, imports, supplies, or otherwise distributes into the United States, and provides support for, 128-Layer NAND memory chips and

[12] Ex. 11 (https://www.techinsights.com/blog/china-does-it-again-nand-memory-market-first).

Micron products containing the same (collectively, the "128L Accused Products"), including products with the part or die name or number B37R and other memory chips (and memory products containing the same) that have the same or similar structures, features, or functionalities, and/or are made by the same or similar manufacturing processes, as the aforementioned exemplary product. An exemplary technical analysis of the B37R is available for purchase at https://www.techinsights.com/products/tcr-2104-805.

25. Micron designs, makes, uses, sells, offers for sale, imports, supplies, or otherwise distributes into the United States, and provides support for, 176-Layer NAND memory chips and Micron products containing the same, (collectively, the "176L Accused Products"), including products with the part or die name or number N48R or B47R, and other memory chips (and memory products containing the same) that have the same or similar structures, features, or functionalities, and/or are made by the same or similar manufacturing processes, as the aforementioned exemplary products. An exemplary technical analysis of the N48R is available for purchase at https://www.techinsights.com/products/mfr-2207-801. An exemplary technical analysis of the B47R is available for purchase at https://www.techinsights.com/blog/memory/micron-176l-3d-nand.

26. Micron designs, makes, uses, sells, offers for sale, imports, supplies, or otherwise distributes into the United States, and provides support for, 232-Layer NAND memory chips and Micron products containing the same (collectively, the "232L Accused Products"), including products with the part or die name or number B58R and other memory chips (and memory products containing the same) that have the same or similar structures, features, or functionalities, and/or are made by the same or similar manufacturing processes, as the aforementioned exemplary product. An exemplary technical analysis of the B58R is available for purchase at https://www.techinsights.com/products/tcr-2303-802.

27. The 96L Accused Products, 128L Accused Products, 176L Accused Products, and 232L Accused Products are collectively referred to as the "Accused Memory Products."

28. The Accused Memory Products are, or are integrated into, devices made, used, sold, offered for sale, imported, supplied, or otherwise distributed in the United States by among others,

Micron, Micron's customers, original equipment manufacturers ("OEMs"), original design manufacturers ("ODMs"), distributors, resellers, and other third parties, including under Micron's own brand name and under the Crucial brand name.[13]

29. Upon information and belief, Micron also conducts research, development, and testing of Accused Memory Products in the United States, including in this judicial District and in California.

30. Upon information and belief, Micron actively encourages others, such as its customers and distributors, to make, use, offer to sell, import, supply, or otherwise distribute into the United States the Accused Memory Products, and products containing the Accused Memory Products.[14] Micron maintains a website that advertises the Accused Memory Products, including identifying the applications for which they can be used, along with specifications for the Accused Memory Products.[15] Micron specifically intends for its customers and end-users to use the Accused Memory Products in such applications and provides instructions and encouragement for its customers and end-users to do so.[16]

31. Micron sells and offers to sell in the United States, and imports into the United States, the Accused Memory Products, which are essential, non-trivial components of the products into which they are integrated, constituting a material part of the claimed inventions of the Asserted Patents, and are not a staple article or commodity of commerce suitable for substantial non-infringing use.

32. Micron knows that the Accused Memory Products and products incorporating the same are used, marketed, sold, offered for sale in, and imported into, the United States. For example, Micron's website identifies distributors of the Accused Memory Products.[17] The website includes a

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[13] *See, e.g.*, Exs. 12-16.

[14] *See e.g.*, Ex. 17 ("We are dedicated to collaborating with you, our customers and partners…"); *see also*, Ex. 18.

[15] *See, e.g.*, Ex. 19.

[16] *See, e.g.*, Ex. 27 (Micron Form 10-K (FY 2023) at 10, *available at* https://investors.micron.com/static-files/25afc2b7-1b51-4f33-9d3b-9d1620fafa30.)

[17] *See, e.g.*, Ex. 21.

list of United States "authorized distributors" for purchasing the Accused Memory Products, including Arrow Electronics, Inc., ASI, Avnet, D&H, Digi-Key, Edge Electronics, Inc., MA Labs, Mouser Electronics, Phoenics Electronics, TD Synnex, and WPG Americas, Inc.[18]

33. Micron also has imported into the United States, and offered to sell, sold, and used within the United States, the Accused Memory Products, which are made by a process patented in the United States during the term of the Asserted Patents. Micron practices the patented processes, or owns or controls, or is owned or controlled by, the person who practices the patented processes. Micron sells its products to customers, including customers in this District, in the computer, networking, storage, consumer electronics, solid-state drive, and mobile telecommunications markets. Micron encourages its customers to import, sell, resell, and/or offer to sell the Accused Memory Products in the United States.[19]

34. Upon information and belief, Micron knew and knows that YMTC has patents in the 3D NAND technology space that are relevant to Micron's own 3D NAND products. There are a limited number of companies competing to make advanced generation 3D NAND products; Micron knows that YMTC is one of them; and Micron knows that YMTC actively patents in that area. Many YMTC-owned patents are cited on the face of Micron's own patents, demonstrating Micron's knowledge of YMTC's patent portfolio that is highly relevant to Micron's own 3D NAND products. Micron has actual knowledge of YMTC's patents in the 3D NAND space, and yet Micron has not sought or received authorization to use those patents.

35. Upon information and belief, Micron's development, sales, marketing, and manufacturing activities in the United States, including within this judicial District, directly contributed to over $8 billion of Micron's net revenue in the United States for the year of 2022 as of

[18] *See, e.g.*, Ex. 21; *see also, e,g.*, Ex. 22.

[19] *See e.g.*, Ex. 23 at 18-19 (Micron listed as a supplier for Dell Technologies, 2022); Ex. 24 at 5 (Micron listed as a supplier for HP, 2021); Ex. 25 at 16 (Micron listed as a "Top 100 Production and Service Suppliers" of Intel, 2020-2021)

September 1, 2022.[20]

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 10,950,623

36. YMTC incorporates by reference and re-alleges all the foregoing paragraphs of this Complaint as if fully set forth herein.

37. YMTC owns by assignment all rights, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 10,950,623, entitled "3D NAND Memory Device and Method of Forming the Same." A true and correct copy of the '623 Patent is attached as Exhibit 1.

38. The '623 Patent was duly and legally issued by the United States Patent and Trademark Office on March 16, 2021.

39. Upon information and belief, Micron infringes under 35 U.S.C. § 271(a) at least claim 1 of the '623 Patent, literally and/or under the doctrine of equivalents, by making, using, offering for sale, selling, and/or importing into the United States, without authorization, at least Micron's 96L Accused Products (for example, the Micron SSD model 1300 SATA, and the Micron SSD model c200) ("the '623 Accused Products"). Further identification of the '623 Accused Products will be provided in YMTC's infringement contentions disclosed pursuant to the Court's scheduling order, and/or as discovery progresses.

40. Upon information and belief, the '623 Accused Products embody and/or are made using each and every limitation of at least claim 1 of the '623 Patent. For example, the '623 Accused Products are memory devices comprising a substrate and a bottom select gate (a polysilicon source gate) disposed over the substrate.

41. Upon information and belief, the '623 Accused Products further comprise a plurality of word lines (layers of polysilicon) positioned over the bottom select gate (a polysilicon source gate)

[20] Ex. 27 at 43 (Micron's 10-K filing, 2022).

with a staircase configuration (a staircase shape at an edge of the of the layers of polysilicon to access the plurality of word lines).

42. Upon information and belief, the '623 Accused Products further comprise a plurality of silicon oxide (SiO) insulating layers disposed between the substrate, the bottom select gate, and the plurality of word lines.

43. Upon information and belief, the '623 Accused Products further comprise one or more first dielectric trenches formed in the bottom select gate extending in a length direction of the substrate to separate the bottom select gate into a plurality of sub-bottom select gates. For example, the '623 Accused Products include trenches formed in the polysilicon source gate and filled with silicon oxide (SiO) that extend in a first direction of the substrate, separating the polysilicon source gate into a plurality of sub-polysilicon source gates.

44. Upon information and belief, the '623 Accused Products further comprise one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the bottom select gate, the plurality of word lines, and the plurality of insulating layers. For example, the '623 Accused Products include one or more tungsten (W) common source lines formed in the memory device that extend in the first direction of the substrate, where the tungsten (W) common source lines extend through the polysilicon source gate, the plurality of word lines (layers of polysilicon) and the plurality of silicon oxide (SiO) insulating layers.

45. As a result of Micron's infringement of the '623 Patent, YMTC is entitled to monetary damages in an amount adequate to compensate for Micron's infringement, but in no event less than a reasonable royalty for the use made of the invention by Micron, together with interest and costs as fixed by the Court.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 11,501,822

46. YMTC incorporates by reference and re-alleges all the foregoing paragraphs of this Complaint as if fully set forth herein.

47. YMTC owns by assignment all rights, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 11,501,822, entitled "Non-Volatile Memory Device and Control Method." A true and correct copy of the '822 Patent is attached as Exhibit 2.

48. The '822 Patent was duly and legally issued by the United States Patent and Trademark Office on November 15, 2022.

49. Upon information and belief, Micron infringes under 35 U.S.C. § 271(a) at least claim 1 of the '822 Patent, literally and/or under the doctrine of equivalents, by making, using, offering for sale, selling, and/or importing into the United States, without authorization, at least Micron's 176L Accused Products (for example, the Micron SSD model 3400 NVMe), and 232L Accused Products (for example, the Micron SSD model 2250) (collectively, "the '822 Accused Products"). Further identification of the '822 Accused Products will be provided in YMTC's infringement contentions disclosed pursuant to the Court's scheduling order, and/or as discovery progresses.

50. Upon information and belief, the '822 Accused Products embody and/or are made using each and every limitation of at least claim 1 of the '822 Patent. For example, the '822 Accused Products are 3D NAND flash memory devices.

51. Upon information and belief, the '822 Accused Products comprise a plurality of memory strings. For example, the '822 Accused Products include a plurality of vertical channels, each respectively part of a plurality of memory cells, each memory cell having channel films, tunnel dielectric films, charge trap films, and blocking dielectric films intersecting with a gate.

52. Upon information and belief, the '822 Accused Products further comprise a bit line connected to a first memory string of the plurality of memory strings. For example, the '822 Accused Products include a metal layer that is a bit line that is connected to memory strings through respective plugs, plug contacts, and bit line contacts. When the '822 Accused Products undergo a program operation, a memory string that is not selected for programming functions as the first memory string.

53. Upon information and belief, the '822 Accused Products further comprise a select gate line connected to the first memory string of the plurality of memory strings. For example, when the

'822 Accused Products undergo a program operation, the memory string that is not selected for programming has gates that are selected by respective select gate lines.

54. Upon information and belief, the '822 Accused Products further comprise a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string. For example, when the '822 Accused Products undergo a program operation, a word line that is selected for programming and that is connected to the memory string that is not selected for programming functions as the selected word line.

55. Upon information and belief, the '822 Accused Products further comprise a control circuit. For example, the '822 Accused Products have a CMOS-under-Array ("CuA") structure, where the complementary metal-oxide-semiconductor ("CMOS") structure is the control circuit and underlies the array of memory cells.[21, 22]

56. Upon information and belief, the '822 Accused Products further comprise a control circuit configured to apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period, apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period, and apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period. For example, in the B47R die, transistors of the CMOS structure are electrically connected to respective word line contacts by "[i]nterconnection metals and contacts/vias for BEOL and CuA," and are configured to apply electrical signals to the respective word lines.[23] The B47R die is programmed by

[21] Ex. 30 (https://www.micron.com/products/nand-flash/176-layer-nand ("Replacement-gate architecture combines charge traps with CMOS-under-array (CuA) design")).

[22] Ex. 31 (https://semiengineering.com/micron-b47r-3d-ctf-cua-nand-die-worlds-first-176l-195t/).

[23] Ex. 32 (https://media-www.micron.com/-/media/client/global/documents/products/white-paper/micron_rg_3d_nand_whitepaper.pdf?la=en&rev=315635e4acb04255a9009c0ad9300cc7) ("The cells have wordlines connected to allow the application of a voltage. Applying voltage to a cell creates operations known as the NAND read-and-write-program functions."); Ex. 30.

a program pulse voltage on the selected word line.[24] When the B47R die undergoes a program operation, a first group of word lines, a second group of word lines, and a third group of word lines other than the word line selected for programming each experience respective electrical signals (pre-pulse signals) at respective voltage levels during a period prior to programming (pre-charge period). Micron's website "176-Layer Flash Memory" refers to Micron's whitepaper "Micron Transitions to Next-Generation Replacement Gate NAND Technology" to describe operation of its 176-layer 3D NAND products. In that whitepaper, Micron describes that different word lines experience different voltages during operation.[25]

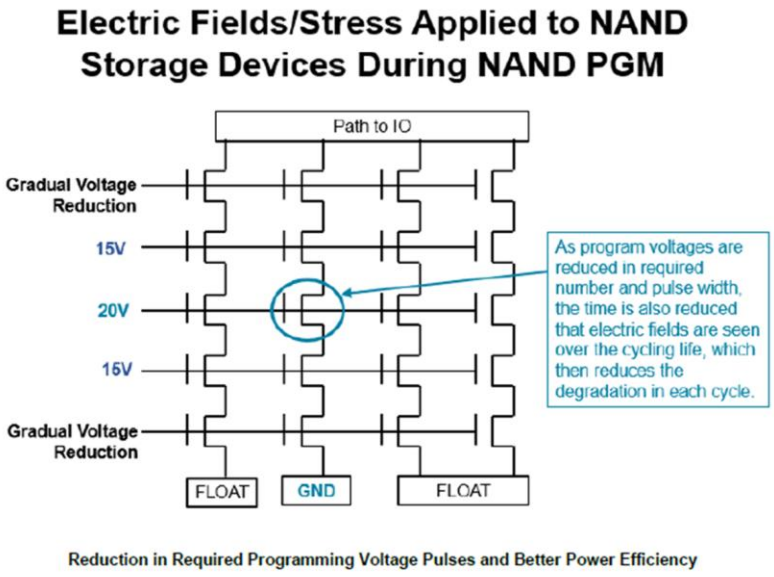

Figure 1[25]

57. Upon information and belief, the '822 Accused Products further comprise the voltage level of the second word line pre-pulse signal being greater than that of the first word line pre-pulse signal and a voltage level of the third word line pre-pulse signal being greater than that of the second

[24] Ex. 32 ("Reducing resistance by using a metal control gate allows the program pulse to ramp up quickly and enables further overhead reductions in complexities of the program and the read algorithms.").

[25] *See* Ex. 32.

word line pre-pulse signal. For example, Micron's whitepaper "Micron Transitions to Next-Generation Replacement Gate NAND Technology" discloses that during programming, different wordlines experience different voltages.[26] Upon information and belief, during the pre-charge period, the first, second, and third groups of word lines also experience pre-pulse signals with different voltages, such that the voltage of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal. *See* Figure 1, *supra*.[25]

58. As a result of Micron's infringement of the '822 Patent, YMTC is entitled to monetary damages in an amount adequate to compensate for Micron's infringement, but in no event less than a reasonable royalty for the use made of the invention by Micron, together with interest and costs as fixed by the Court.

COUNT III: INFRINGEMENT OF U.S. PATENT NO. 10,658,378

59. YMTC incorporates by reference and re-alleges all the foregoing paragraphs of this Complaint as if fully set forth herein.

60. YMTC owns by assignment all rights, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 10,658,378, entitled "Through Array Contract (TAC) for Three-Dimensional Memory Devices." A true and correct copy of the '378 Patent is attached as Exhibit 3.

61. The '378 Patent was duly and legally issued by the United States Patent and Trademark Office on May 19, 2020.

62. Upon information and belief, Micron infringes under 35 U.S.C. § 271(a) at least claim 15 of the '378 Patent, literally and/or under the doctrine of equivalents, by making, using, offering for sale, selling, and/or importing into the United States, without authorization, at least Micron's 128L Accused Products (for example, Micron BX500 2.5 480GB SSD), 176L Accused Products (for

[26] *See* Ex. 32.

example, the Micron SSD model 3400 NVMe and the Micron SSD model 2400 PCIe Gen 4), and 232L Accused Products (for example, the Micron SSD model 2250) (collectively, "the '378 Accused Products"). Further identification of the '378 Accused Products will be provided in YMTC's infringement contentions disclosed pursuant to the Court's scheduling order, and/or as discovery progresses.

63. Upon information and belief, the '378 Accused Products meet each and every limitation of at least claim 15 of the '378 Patent. For example, the '378 Accused Products are three-dimensional (3D) memory devices comprising a semiconductor substrate with an isolation structure of silicon oxide (SiO) dielectric material on a top portion of the semiconductor substrate.

64. Upon information and belief, the '378 Accused Products further comprise an alternating layer stack disposed on the semiconductor substrate. For example, the '378 Accused Products include a stack of alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers on the semiconductor substrate.

65. Upon information and belief, the '378 Accused Products further comprise a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure, and the dielectric structure is formed of a dielectric material. For example, the '378 Accused Products include a silicon oxide (SiO) dielectric structure on the silicon oxide (SiO) isolation structure extending through the stack of alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers where the stack of alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers abuts a sidewall of the dielectric structure formed of dielectric material silicon oxide (SiO).

66. Upon information and belief, the '378 Accused Products further comprise channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack. For example, the '378 Accused Products include channel structures having polysilicon within a dielectric layer and slit structures having silicon oxide (SiO) and germanium (Ge), where the channel

structures and slit structures extend through the stack of alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers.

67. Upon information and belief, the '378 Accused Products further comprise a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon, and a word line contact disposed on the conductor layer of each level. For example, the '378 Accused Products include a staircase shape formed in the stack of alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers, where each level of the staircase structure includes a tungsten (W) word line contact disposed on a titanium nitride (TiN) conductor layer of each level of the staircase structure.

68. Upon information and belief, the '378 Accused Products further comprise local contacts disposed on the channel structures and the slit structures. For example, the '378 Accused Products include local contacts disposed on the channel structures having polysilicon within a dielectric layer and slit structures having silicon oxide (SiO) and germanium (Ge).

69. Upon information and belief, the '378 Accused Products further comprise through array contacts (TACs) extending vertically through the dielectric and the isolation structures. For example, the '378 Accused Products include through array tungsten (W) contacts that extend vertically through the silicon oxide (SiO) dielectric structure and the silicon oxide (SiO) isolation structure.

70. Upon information and belief, Micron has infringed and continues to infringe under 35 U.S.C. § 271(g) by importing into the United States or offering to sell, selling, or using within the United States a product which is made by a process patented in the United States during the term of the '378 Patent. Micron has practiced the patented process; or owns or controls, or is owned or controlled by the person who has practiced the patented process. Micron sells its products to customers, including customers in this District, in the computer, networking, storage, consumer electronics, solid-state drive, and mobile telecommunications markets. Micron encourages its customers to import, sell, resell, offer to sell, and/or resell the '378 Accused Products.

71. As a result of Micron's infringement of the '378 Patent, YMTC is entitled to monetary damages in an amount adequate to compensate for Micron's infringement, but in no event less than a

reasonable royalty for the use made of the invention by Micron, together with interest and costs as fixed by the Court.

COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 10,937,806

72. YMTC incorporates by reference and re-alleges all the foregoing paragraphs of this Complaint as if fully set forth herein.

73. YMTC owns by assignment all rights, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 10,937,806, entitled "Through Array Contact (TAC) for Three-Dimensional Memory Devices." A true and correct copy of the '806 Patent is attached as Exhibit 4.

74. The '806 Patent was duly and legally issued by the United States Patent and Trademark Office on March 2, 2021.

75. Upon information and belief, Micron infringes under 35 U.S.C. § 271(a) at least claim 8 of the '806 Patent, literally and/or under the doctrine of equivalents, by making, using, offering for sale, selling, and/or importing into the United States, without authorization, at least Micron's 128L Accused Products (for example, Micron BX500 2.5 480GB SSD), 176L Accused Products (for example, the Micron SSD model 3400 NVMe and the Micron SSD model 2400 PCIe Gen 4), and 232L Accused Products (for example, the Micron SSD model 2250) (collectively, "the '806 Accused Products"). Further identification of the '806 Accused Products will be provided in YMTC's infringement contentions disclosed pursuant to the Court's scheduling order, and/or as discovery progresses.

76. Upon information and belief, the '806 Accused Products meet each and every limitation of at least claim 8 of the '806 Patent. For example, the '806 Accused Products are three-dimensional (3D) memory devices comprising an alternating conductor/dielectric layer stack (alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers).

77. Upon information and belief, the '806 Accused Products further comprise a dielectric structure extending vertically through the alternating conductor/dielectric layer stack. For example,

the ’806 Accused Products include a silicon oxide (SiO) dielectric structure extending vertically through the alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers.

78. Upon information and belief, the ’806 Accused Products further comprise first and second channel regions comprising first and second pluralities of channel structures, respectively. For example, the ’806 Accused Products include a first channel region comprising a first plurality of channel structures having polysilicon within a dielectric layer, and a second channel region comprising a second plurality of channel structures having polysilicon within a dielectric layer.

79. Upon information and belief, the ’806 Accused Products further comprise slit structures extending vertically through the alternating conductor/dielectric layer stack. For example, the ’806 Accused Products include slit structures having silicon oxide (SiO) and germanium (Ge) extend through the stack of alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers.

80. Upon information and belief, the ’806 Accused Products further comprise a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon. For example, the ’806 Accused Products include a staircase shape formed in the stack of alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers, where the staircase structure includes levels having a tungsten (W) and titanium nitride (TiN) conductor layer.

81. Upon information and belief, the ’806 Accused Products further comprise local contacts disposed on the first and second channel structures and the slit structures. For example, the ’806 Accused Products include local contacts disposed on the first and second channel structures having polysilicon within a dielectric layer and slit structures having silicon oxide (SiO) and germanium (Ge).

82. Upon information and belief, the ’806 Accused Products further comprise a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure. For example, the ’806 Accused Products include a through array contact region

comprising a plurality of through array tungsten (W) contacts that extend vertically through the silicon oxide (SiO) dielectric structure.

83. Upon information and belief, the '806 Accused Products further comprise a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions. For example, the '806 Accused Products include a plurality of dummy channel structures surrounding the through array contact region having the plurality of through array tungsten (W) contacts, and the dummy channel structures are between first and second regions of first and second channel structures having polysilicon within a dielectric layer.

84. Upon information and belief, Micron has infringed and continues to infringe under 35 U.S.C. § 271(g) by importing into the United States or offering to sell, selling, or using within the United States a product which is made by a process patented in the United States during the term of the '806 Patent. Micron has practiced the patented process; or owns or controls, or is owned or controlled by the person who has practiced the patented process. Micron sells its products to customers, including customers in this District, in the computer, networking, storage, consumer electronics, solid-state drive, and mobile telecommunications markets. Micron encourages its customers to import, sell, resell, offer to sell, and/or resell the '806 Accused Products.

85. As a result of Micron's infringement of the '806 Patent, YMTC is entitled to monetary damages in an amount adequate to compensate for Micron's infringement, but in no event less than a reasonable royalty for the use made of the invention by Micron, together with interest and costs as fixed by the Court.

COUNT V: INFRINGEMENT OF U.S. PATENT NO. 10,861,872

86. YMTC incorporates by reference and re-alleges all the foregoing paragraphs of this Complaint as if fully set forth herein.

87. YMTC owns by assignment all rights, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 10,861,872, entitled

"Three Dimensional Memory Device and Methods for Forming the Same." A true and correct copy of the '872 Patent is attached as Exhibit 5.

88. The '872 Patent was duly and legally issued by the United States Patent and Trademark Office on December 8, 2020.

89. Upon information and belief, Micron infringes under 35 U.S.C. § 271(a) at least claim 1 of the '872 Patent, literally and/or under the doctrine of equivalents, by making, using, offering for sale, selling, and/or importing into the United States, without authorization, at least Micron's 128L Accused Products (for example, Micron BX500 2.5 480GB SSD), 176L Accused Products (for example, the Micron SSD model 3400 NVMe and the Micron SSD model 2400 PCIe Gen 4), and 232L Accused Products (for example, the Micron SSD model 2250) (collectively, "the '872 Accused Products"). Further identification of the '872 Accused Products will be provided in YMTC's infringement contentions disclosed pursuant to the Court's scheduling order, and/or as discovery progresses.

90. Upon information and belief, the '872 Accused Products meet each and every limitation of at least claim 1 of the '872 Patent. For example, the '872 Accused Products are three-dimensional (3D) memory devices comprising a substrate and a memory stack comprising interleaved conductive layers and dielectric layers on the substrate (alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers).

91. Upon information and belief, the '872 Accused Products further comprise a staircase structure on one side of the memory stack and a staircase contact in the staircase structure. For example, the '872 Accused Products include a staircase shape formed in the stack of alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers and a contact that extends to the word line contact in staircase structure.

92. Upon information and belief, the '872 Accused Products further comprise a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact, wherein each of the dummy source structures comprises a conductive contact. For example, the '872 Accused Products include a plurality

of non-electrically functional dummy structures that extend vertically through the staircase shape formed in the stack of alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers and surrounding the staircase contact that extends to the word line contact in staircase structure.

93. As a result of Micron's infringement of the '872 Patent, Plaintiff is entitled to monetary damages in an amount adequate to compensate for Micron's infringement, but in no event less than a reasonable royalty for the use made of the invention by Micron, together with interest and costs as fixed by the Court.

COUNT VI: INFRINGEMENT OF U.S. PATENT NO. 11,468,957

94. YMTC incorporates by reference and re-alleges all the foregoing paragraphs of this Complaint as if fully set forth herein.

95. YMTC owns by assignment all rights, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 11,468,957, entitled "Architecture and Method for NAND Memory Operation." A true and correct copy of the '957 Patent is attached as Exhibit 6.

96. The '957 Patent was duly and legally issued by the United States Patent and Trademark Office on October 11, 2022.

97. Upon information and belief, Micron infringes under 35 U.S.C. § 271(a) at least claim 1 of the '957 Patent, literally and/or under the doctrine of equivalents, by making, using, offering for sale, selling, and/or importing into the United States, without authorization, at least Micron's 176L Accused Products (for example, the Micron SSD model 2400 PCIe Gen4) ("the '957 Accused Products"). Further identification of the '957 Accused Products will be provided in Plaintiff's infringement contentions disclosed pursuant to the Court's scheduling order, and/or as discovery progresses.

98. Upon information and belief, the '957 Accused Products embody and/or are made using each and every limitation of at least claim 1 of the '957 Patent. Upon information and belief, the '957 Accused Products are apparatuses for reading a memory device. For example, the '957 Accused

Products are 176-layer 3D NAND memory devices that include a "24% lower read latency than Micron's prior generation solution."[27]

99. Upon information and belief, the '957 Accused Products include a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate transistor, memory cells, and a top-select-gate transistor that are connected in series, the second memory cells string including a bottom-select-gate transistor, memory cells, and a top-select-gate transistor that are connected in series. For example, the '957 Accused Products are "charge trap" 176-layer NAND memory devices and have a plurality of memory cell strings, each of which include select-gate transistors at the top (top-select-gate transistors) and at the bottom (bottom-select-gate transistors) connected in series with memory cells arranged in between, and the top-select-gate and bottom-select-gate transistors of a memory cell string are used to turn on the memory cell string in the "charge trap" flash configuration. [27, 28]

100. Upon information and belief, the '957 Accused Products further comprise processing circuitry configured to apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell. For example, the '957 Accused Products contain processing circuitry for processing read and write commands including applying verify voltages and is programmed using a "charge trap" process that involves applying voltages to gate terminals of memory cells through wordlines.[27] For example, the '957 Accused Products include a "24% lower read latency than Micron's prior generation solution."[27] On information and belief, the '957 Accused Products' CMOS transistors are electrically connected to respective word line contacts by "[i]nterconnection metals and contacts/vias for BEOL and CuA," and are configured to apply electrical signals to the respective word lines, and therefore gate terminals of

[27] Ex. 37 (https://investors.micron.com/news-releases/news-release-details/micron-ships-industrys-first-176-layer-qlc-nand-volume-and).

[28] Ex. 31.

the memory cell strings.[29] The '957 Accused Products are programmed, read, and verified by voltages on the respective word lines.[30] In the '957 Accused Products, the memory cell strings include multiple memory cells that can be programmed; thus, the selected memory cell of a string that is programmed has first and second memory cells adjacent to it. In the '957 Accused Products, individual memory cells of the memory cell strings include respective gate terminals having a "replacement-gate architecture."[31]

101. Upon information and belief, the '957 Accused Products further comprise a processing circuitry configured to apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed. For example, in the '957 Accused Products, prior to verification, a memory cell that is not programmed experiences a voltage on its gate terminal, which is a first bias voltage.

102. Upon information and belief, the '957 Accused Products further comprise a processing circuitry configured to apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string. For example, in the '957 Accused Products, during verification, the memory cell that is being programmed (the selected memory cell) experiences a voltage on its gate terminal, which is a second verify voltage.

103. Upon information and belief, the '957 Accused Products further comprise a processing circuitry configured to apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage. For example, in '957 Accused Products, the memory cell that is not programmed (which experienced the first bias voltage) subsequently during verification experiences a voltage on its gate terminal that is smaller than the first bias voltage (the second bias voltage). Micron's website "176-Layer Flash Memory" refers to Micron's whitepaper "Micron

[29] Exs. 32 ("The cells have wordlines connected to allow the application of a voltage. Applying voltage to a cell creates operations known as the NAND read-and-write-program functions."); 30.

[30] Ex. 32.

[31] Ex. 37.

Transitions to Next-Generation Replacement Gate NAND Technology" to describe operation of its 176-layer 3D NAND products. In that whitepaper, Micron describes that different word lines experience different voltages during operation.[32]

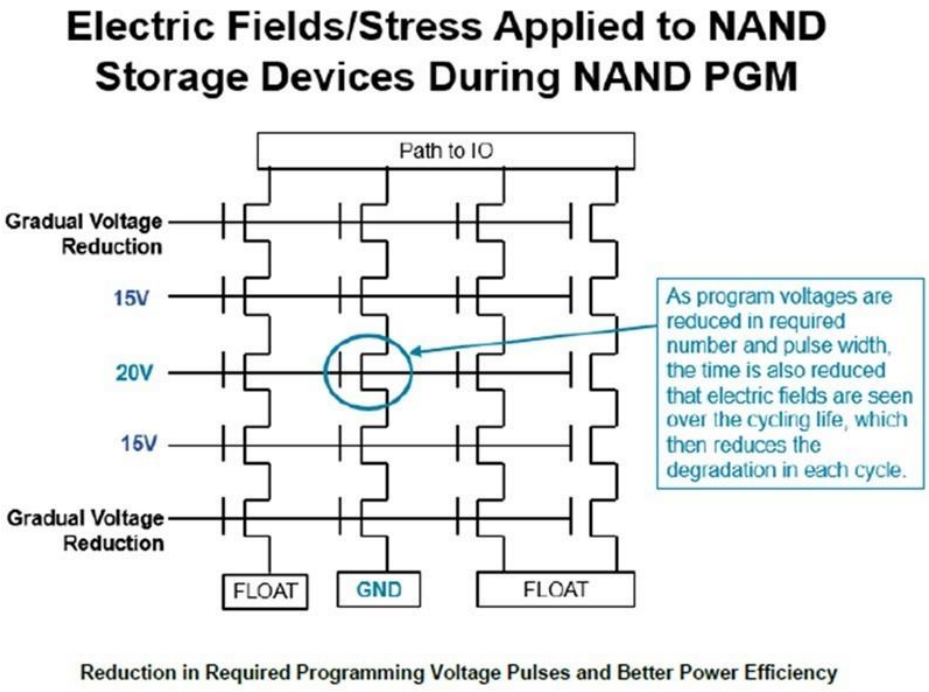

Figure 2[32]

104. As a result of Micron's infringement of the '957 Patent, Plaintiff is entitled to monetary damages in an amount adequate to compensate for Micron's infringement, but in no event less than a reasonable royalty for the use made of the invention by Micron, together with interest and costs as fixed by the Court.

COUNT VII: INFRINGEMENT OF U.S. PATENT NO. 11,600,342

105. YMTC incorporates by reference and re-alleges all the foregoing paragraphs of this Complaint as if fully set forth herein.

[32] Ex. 32.

106. YMTC owns by assignment all rights, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 11,600,342, entitled "Method for Reading Three-Dimensional Flash Memory." A true and correct copy of the '342 Patent is attached as Exhibit 7.

107. The '342 Patent was duly and legally issued by the United States Patent and Trademark Office on March 7, 2023.

108. Upon information and belief, Micron infringes under 35 U.S.C. § 271(a) at least claim 1 of the '342 Patent, literally and/or under the doctrine of equivalents, by making, using, offering for sale, selling, and/or importing into the United States, without authorization, at least Micron's 176L Accused Products (for example, Micron SSD model 2400 PCIe Gen 4) and 232L Accused Products (for example, the Micron SSD model 2250) (collectively, "the '342 Accused Products").

109. Upon information and belief, the '342 Accused Products are used to perform and/or practice each and every limitation of at least claim 1 of the '342 Patent. For example, the '342 Accused Products are three-dimensional (3D) memory devices on which read-verification operations are conducted. For example, the '342 Accused Products include a "24% lower read latency than Micron's prior generation solution."[33] Further identification of the '342 Accused Products will be provided in YMTC's infringement contentions disclosed pursuant to the Court's scheduling order, and/or as discovery progresses.

110. Upon information and belief, the '342 Accused Products conduct a read-verification operation by a method comprising the steps of applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period. For example, the '342 Accused Products are a "charge trap" 3D NAND devices and have a plurality of memory cell strings, each of which include select-gate transistors at the top (top-select-gate transistors) and at the bottom (bottom-select-gate transistors) connected in series with memory cells arranged in between, and the top-select-gate and bottom-select-gate transistors of a

[33] Ex. 37.

memory cell string are used to turn on the memory cell string in the "charge trap" flash configuration.[35] The '342 Accused Products are programmed, verified, and read using a "charge trap" process which involves applying voltages to gate terminals of memory cells through wordlines.[34] The '342 Accused Products include a "24% lower read latency than Micron's prior generation solution."[34] On information and belief, the '342 Accused Products' CMOS transistors are electrically connected to respective word line contacts by "[i]nterconnection metals and contacts/vias for BEOL and CuA," and are configured to apply electrical signals to the respective word lines, and therefore gate terminals of the memory cell strings.[35] On information and belief, the '342 Accused Products are read and verified, as they are programmed, by varying voltages on the respective word lines.[36]

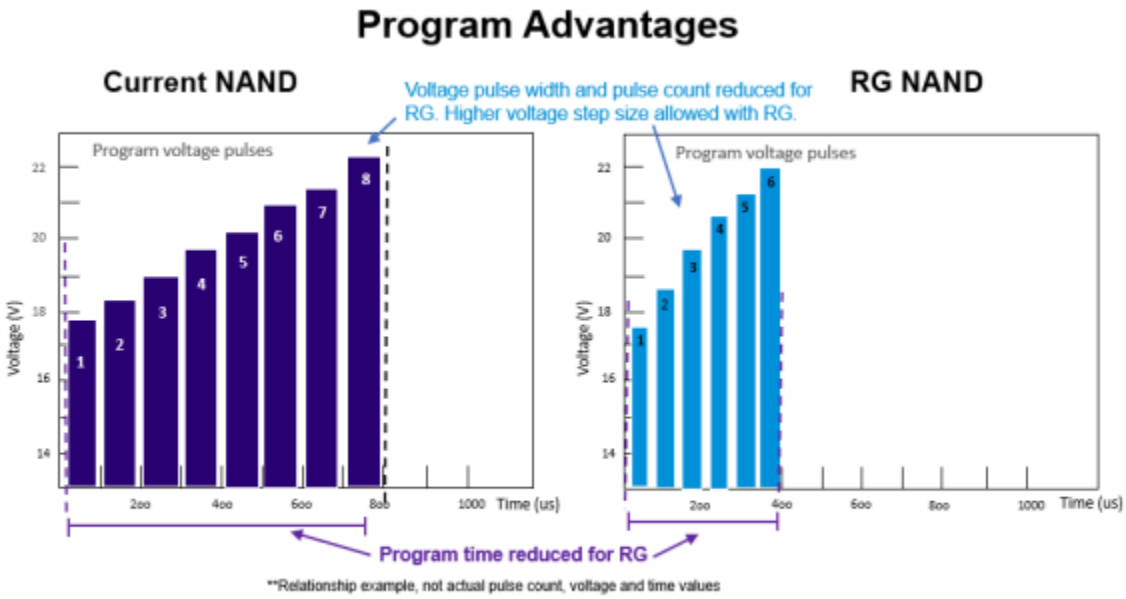

Figure 2: Comparison of Voltage Pulse Widths and Pulse Counts

Figure 3[36]

111. During verification, the top select gate of a memory string that is not selected experiences voltage during a first time period to turn on the top-select-gate transistor that is a prepare

[34] Ex. 37.

[35] Exs. 31; 37.

[36] Ex. 32.

voltage and subsequently experiences a different voltage to turn off the transistor during a second time period that is an off voltage.

112. Upon information and belief, the '342 Accused Products further conduct a read-verification operation by a method comprising the step of applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period. On information and belief, the '342 Accused Products are read and verified, as they are programmed, by varying voltages on the respective word lines.[37] On information and belief, during verification, the word line of the memory cell that is selected for programming (selected word line) experiences a voltage (off voltage) during the first time period to turn off the selected word line and subsequently experiences a different voltage (read voltage) to turn on the selected word line for reading of the selected memory cell.

113. Upon information and belief, the '342 Accused Products further conduct a read-verification operation by a method comprising the step of applying, on an unselected word line, a pass voltage during the first time period and the second time period. On information and belief, the '342 Accused Products are read and verified, as they are programmed, by varying voltages on the respective word lines.[37] On information and belief, during verification, a word line that is not selected for programming experiences a non-zero voltage (pass voltage) to turn on its constituent memory cells during the first and second time periods.

114. Upon information and belief, the '342 Accused Products further conduct a read-verification operation by a method comprising the step of the read-verification operation removing fast charges of the target memory cell during the first time period. For example, when memory cells of the '342 Accused Products are programmed, fast charges accumulate in shallow traps in the charge trap layer which is a "nonconductive layer of silicon nitride (SiN)," and the read-verification operation removes these charges to result in an accurate and reliable threshold voltage for the programmed memory cell.[37]

[37] Ex. 32.

115. As a result of Micron's infringement of the '342 Patent, Plaintiff is entitled to monetary damages in an amount adequate to compensate for Micron's infringement, but in no event less than a reasonable royalty for the use made of the invention by Micron, together with interest and costs as fixed by the Court.

COUNT VIII: INFRINGEMENT OF U.S. PATENT NO. 10,868,031

116. YMTC incorporates by reference and re-alleges all the foregoing paragraphs of this Complaint as if fully set forth herein.

117. YMTC owns by assignment all rights, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 10,868,031, entitled "Multiple-Stack Three-Dimensional Memory Device And Fabrication Method Thereof." A true and correct copy of the '031 Patent is attached as Exhibit 8.

118. The '031 Patent was duly and legally issued by the United States Patent and Trademark Office on December 15, 2020.

119. Upon information and belief, Micron infringes under 35 U.S.C. § 271(a) at least claim 1 of the '031 Patent, literally and/or under the doctrine of equivalents, by making, using, offering for sale, selling, and/or importing into the United States, without authorization, at least Micron's 128L Accused Products (for example, Micron BX500 2.5 480GB SSD), and Micron's 176L Accused Products (for example, the Micron SSD model 3400 NVMe and the Micron SSD model 2400 PCIe Gen 4) (collectively, "the '031 Accused Products"). Further identification of the '031 Accused Products will be provided in YMTC's infringement contentions disclosed pursuant to the Court's scheduling order, and/or as discovery progresses.

120. Upon information and belief, the '031 Accused Products meet each and every limitation of at least claim 1 of the '031 Patent. For example, the '031 Accused Products are three-dimensional (3D) memory devices comprising a substrate, including polysilicon.

121. Upon information and belief, the '031 Accused Products further comprise a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate,

wherein each of the plurality of staircase structures comprises a plurality of conductor layers, and wherein each of the plurality of conductor layers is located between two insulating layers (silicon oxide (SiO). For example, the '031 Accused Products include a lower deck and upper deck stair case structure forming a multi-stack staircase shape having a stack of alternating tungsten (W) and/or titanium nitride (TiN)) conductor layers and silicon oxide (SiO) dielectric layers, where each staircase structure includes levels having a tungsten (W) and titanium nitride (TiN) conductor layer between two insulating layers of silicon oxide (SiO).

122. Upon information and belief, the '031 Accused Products further comprise a filling structure surrounding the multiple-stack staircase structure. For example, the '031 Accused Products include a filling structure (silicon dioxide (SiO2)) that surrounds the multiple-stack staircase structure.

123. Upon information and belief, the '031 Accused Products further comprise a semiconductor channel extending through the multiple-stack staircase structure, wherein the semiconductor channel comprises unaligned sidewall surfaces. For example, the '031 Accused Products include a semiconductor channel having a silicon nitride (SiN) charge trap film, polysilicon channel and silicon oxide (SiO) core extending through the stack of alternating tungsten (W) conductor layers and silicon oxide (SiO) dielectric layers where the semiconductor channel comprises unaligned sidewall surfaces that are not contiguous along a substantially straight line.

124. Upon information and belief, the '031 Accused Products further comprise a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure, wherein the supporting pillar comprises aligned sidewall surfaces. For example, the '031 Accused Products include a silicon oxide (SiO) dielectric structure comprising titanium nitride (TiN) and tungsten (W) surrounded by an insulating material (silicon oxide (SiO)) extending through the stack of alternating conductor layers and silicon oxide (SiO) dielectric layers, wherein the supporting pillar comprises aligned sidewall surfaces that are contiguous along a substantially straight line.

125. As a result of Micron's infringement of the '031 Patent, Plaintiff is entitled to monetary damages in an amount adequate to compensate for Micron's infringement, but in no event less than a

reasonable royalty for the use made of the invention by Micron, together with interest and costs as fixed by the Court.

PRAYER FOR RELIEF

WHEREFORE, YMTC respectfully requests judgment in its favor and against Micron, and respectfully requests the following relief:

1. A judgment in favor of YMTC that Micron has infringed and is infringing, either literally and/or under the doctrine of equivalents, one or more claims of the Asserted Patents;

2. An order pursuant to 35 U.S.C. § 283 enjoining Micron and its subsidiaries, parents, divisions, affiliates, successors, assigns, transferees, officers, directors, attorneys, agents, servants, employees, parties in privity with, and all other persons in active concert or participation with any of the foregoing, from continued acts of infringement of any claim of the Asserted Patents;

3. A judgment and order requiring Micron to pay YMTC its damages, costs, expenses, and pre-judgment and post-judgment interest for Micron's infringement;

4. If a permanent injunction is not granted, then a judicial determination of the conditions for Micron's future infringement, such as an ongoing royalty;

5. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to YMTC its reasonable attorneys' fees against Micron; and

6. All other relief that the Court deems just and proper.

JURY TRIAL DEMAND

YMTC respectfully demands a jury trial pursuant to Rule 38(b) of the Federal Rules of Civil Procedure on all claims and issues so triable.

Dated: November 9, 2023

By: */s/ Andrew T. Radsch*

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Andrew T. Radsch (CSB # 303665)
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