

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF MICHIGAN**

BELL SEMICONDUCTOR, LLC

Plaintiff,

v.

SOCIONEXT AMERICA , INC.

Defendant.

Civil Action No. _____

JURY TRIAL DEMANDED

ORIGINAL COMPLAINT

Plaintiff Bell Semiconductor, LLC (“Bell Semic” or “Plaintiff”) brings this Complaint against Defendant Socionext America, Inc. (“Socionext”) for infringement of U.S. Patent No. 7,231,626 (“the ’626 patent”) and U.S. Patent No. 7,396,760 (“the ’760 patent”). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1. This is a patent infringement suit relating to Socionext’s unauthorized and unlicensed use of the ’626 patent and ’760 patent. The circuit design methodologies claimed in the ’626 patent and ’760 patent are used by Socionext in the production of one or more of its semiconductor chips, including its SynQuacer SC2A11 chips. (“Socionext Accused Product”).

2. Traditionally, the process flow for IC design is highly linear, with each phase of the design process depending on the previous steps. Accordingly, when revisions to portions of the physical design are made, as typically happens numerous times during the design process, all the subsequent steps typically need to be redone in their entirety for at least the layer, if not the entire device. This is because regardless of the size or extent of the revision to the physical design, the changes must be merged into a much larger integrated circuit design and then the remaining steps of the design process flow re-run.

3. Before the inventions claimed in the '626 patent, the typical turnaround time for implementing a change to the physical design for cutting edge devices was approximately one week regardless of the size of the change. This is extremely inefficient in most instances where the change relates to only a small fraction of the overall design. *See* Ex. A at 3:16–18 & Fig. 1.

4. The '626 patent's inventors solved this problem by defining a window that encloses a change specified by the revision to physical design. The window defines an area that is less than the area of the entire circuit design. Only the nets within that window are routed pursuant to the revision, leaving the remaining nets in the design unaffected. Then, the results of that incremental routing are inserted into a copy of the original IC design to produce a revised IC design that effects the physical design change without needing to redo the entire process flow.

5. Manufacturers use a process called Chemical Mechanical Planarization/Polishing (“CMP”) to smooth out the surface of the device to prepare the device for further processing, such as deposition of another layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be “polished” away at different rates, leading to erosion or dishing on the surface.

6. To reduce this problem “dummy” material, also known as “dummy fill,” is typically inserted into low-density regions of the device to increase the overall uniformity of the structures on the surface of the layer and reduce the density variability across the surface of the device. However, dummy fill can increase capacitance if it is placed too close to signal wires, which slows the transmission speed of signals and degrades the overall performance of the device.

7. Just as unwanted capacitance can result from the interaction of elements within the layer of an integrated circuit, it can also result from interaction of elements across adjacent layers. While certain elements (such as signal lines and power lines) cannot be easily moved without affecting circuit performance, there is substantially more flexibility regarding placement, positioning, and spacing of non-

signal carrying features such as dummy fill, even when certain quantities of dummy fill are needed within layers and portions of layers to meet processing requirements.

8. Prior to development of the methodology described in the '760 patent, the placement of dummy fill in the open areas of the interconnect layer was performed based primarily upon meeting density requirements. To the extent that timing and capacitance effects were considered in dummy fill dimensions, orientation, positioning, or otherwise in dummy fill placement, the conventional dummy fill tools at the time only considered intralayer effects—i.e., interactions between dummy fill features and other elements (such as signal nets) on that same layer. However, use of dummy fill that overlapped on successive layers could and often did create a substantial interlayer bulk capacitive effect that had a negative impact on circuit timing and performance, and which was not considered by the conventional dummy fill tools at the time even when they considered certain intralayer timing effects. *See* Ex. D at 1:43–2:6, 4:11–16.

9. Recognizing these drawbacks, as well as the importance of having a flat or planarized surface on the devices, the inventors of the '760 patent set out to develop a design process that would also consider the interlayer bulk capacitance created by overlapping dummy fill and consider those intralayer effects in arranging dummy fill in the chip layout so as to minimize the unwanted bulk capacitance created by overlapping dummy fill features.

10. The inventors of the '760 patent ultimately conceived of a method for addressing the interlayer capacitive effects of dummy fill by treating each successive set of layers as a pair and then rearranging the dummy fill in one or both layers so as to minimize their overlap. This was particularly advantageous in “intelligent dummy fill placement,” i.e., when timing impact is considered when placing dummy fill. *See* Ex. D at 2:10–19.

11. The inventions disclosed in the '760 patent provide many advantages over the prior art. In particular, rearranging the dummy fill features such that they do not align vertically in successive layers can reduce unwanted bulk capacitance introduced by dummy fill and thus minimize the interlayer capacitance. *See* Ex. D at 2:45–48, 2:47–59, 3:30–33, 5:19–39. This removed unwanted bulk capacitance that would otherwise slow down signals in the circuit and adversely affect timing in the IC, thus improving its speed and performance. *See* Ex. D at 2:3–6. These significant advantages are achieved through the use of the patented inventions and thus the '760 patent presents significant commercial value for companies like ASMedia.

12. Bell Semic brings this action to put a stop to Socionext’s unauthorized and unlicensed use of the inventions claimed in the '626 and '760 patent.

THE PARTIES

13. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

14. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America's greatest technology incubators. Bell Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

15. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor-related inventions was developed over many years by some of the world's leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation ("LSI"). This portfolio reflects technology that

underlies many important innovations in the development of semiconductors and integrated circuits for high-tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

16. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since those early days at Bell Labs. For example, Bell Semic's CTO was a LSI Fellow and Broadcom Fellow. He is known throughout the world as an innovator with more than 300 patents to his name, and he has a sterling reputation for helping semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from the semiconductor world to work with Nortel Networks in the telecom industry during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees and employees. In addition, several Bell Semic executives previously served as engineers at many of these companies and were personally involved in creating the ideas claimed throughout Bell Semic's extensive patent portfolio.

17. On information and belief, Socionext is organized and exists under the laws of the State of California. Socionext develops, designs, and/or manufactures products in the United States, including in this District, according to the '626 and/or '760 patented process/methodology; and/or uses the '626 and/or '760 patented

process/methodology in the United States, including in this District, to make products; and/or distributes, markets, sells, or offers to sell in the United States and/or imports products into the United States, including in this District, that were manufactured or otherwise produced using the patented process. Additionally, Socionext introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

JURISDICTION AND VENUE

18. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

19. This Court has personal jurisdiction over Socionext under the laws of the State of Michigan, due at least to its substantial business in Michigan and in this District. Socionext has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of Michigan, and in this District by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of Michigan and in this District, Socionext, directly or through intermediaries: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the '626 and/or '760 patented

process/methodology; (iii) distributes, markets, sells, or offers to sell products formed according to the '626 and/or '760 patented process/methodology; and/or (iv) imports products formed according to the '626 and/or '760 patented process/methodology.

20. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because Socionext has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, Socionext maintains a regular and established place of business at 34441 Eight Mile Road Suite 110, Livonia, MI 48152.

21. Venue is also convenient in this District. This is at least true because of this District's close ties to this case—including the technology, relevant witnesses, and sources of proof noted above—and its ability to quickly and efficiently move this case to resolution.

22. On information and belief, Bell Semic's causes of action arise directly from Socionext's circuit design work and other activities in this District. Moreover, on information and belief, Socionext has derived substantial revenues from its infringing acts occurring within the State of Michigan and within this District.

U.S. PATENT NO. 7,231,626

23. Bell Semiconductor owns by assignment the entire right, title, and interest in the '626 patent, entitled "Method Of Implementing An Engineering Change Order In An Integrated Circuit Design By Windows."

24. A true and correct copy of the '626 patent is attached as Exhibit A.

25. The '626 patent issued to inventors Jason K. Hoff, Viswanathan Lakshmanan, Michael Josephides, Daniel W. Prevedel, Richard D. Blinne, and Johathan P. Kuppinger.

26. The application that resulted in issuance of the '626 patent, United States Patent Application No. 11/015,123, was filed December 17, 2004. It issued on June 12, 2007 and expires on July 26, 2025.

27. The '626 patent generally relates to "methods of implementing an engineering change order (ECO) in an integrated circuit design." Ex. A at 1:1–13.

28. The background section of the '626 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior circuit design methodology was disadvantageous because "[i]n previous methods for implementing an engineering change order (ECO) request in an integrated circuit design, design tools are run for the entire integrated circuit design, even though the engineering change order typically is only a small fraction of the size of the integrated circuit design" Ex. A at 2:15–19.

29. The '626 patent elaborates that because “cell placement, routing, design rule check validation, and timing closure run times typically scale with the size of the entire integrated circuit design,” Ex. A at 2:20–22, this produced a “typical turnaround time” of “about one week regardless of the size of the engineering change order. . . . because although the engineering change order may only have a size of a few cells, it must be merged with an integrated circuit design that typically has a much greater size.” *Id.* at 2:37–44. Certain of these steps “may be especially time consuming and resource intensive.” *Id.* at 3:16–17.

30. The inventions disclosed in the '626 patent provide many advantages over the prior art. In particular, they provide a simple and efficient method for ensuring that revisions to the physical design of the IC do not unduly delay the completion of the design process. As the '626 patent explains, “significant savings in the resources required to perform routing, design rule check verification, net delay calculation, and parasitic extraction may be realized by creating windows in the integrated circuit design that include only the incremental changes to the overall integrated circuit design.” Ex. A at 3:19–23.

31. As mentioned above, this is very beneficial because it substantially reduces the run time of the routing tools and related follow-on steps of the layout portion of the design process flow (such as calculation of net delay, design rule check, and parasitic extraction). Thus, it shortens the overall design timeline, and

avoids cost overruns and delays, making it less costly to make changes later in the design process or more often. *See id.*

32. Given the aforementioned increased complexity of circuit designs and the corresponding delays from design changes, these efficiency gains have become more and more important in completing the design process without affecting time-to-market. These significant advantages are achieved through the use of the patented inventions and thus the '626 patent presents significant commercial value for chip designers.

33. In light of the drawbacks of the prior art, the '626 patent's inventors recognized the need for a circuit design methodology in which the time required to implement an ECO "depend[s] on the number of net changes in the [ECO] rather than on the total number of nets in the entire integrated circuit design." Ex. A at 2:51–53. The inventions claimed in the '626 patent address this need.

34. The '626 patent contains two independent claims and 8 total claims, covering a method and computer readable medium for implementing a change order in an integrated circuit design. Claim 1 reads:

1. A method comprising steps of:

(a) receiving as input an integrated circuit design;

(b) receiving as input an engineering change order to the integrated circuit design;

(c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;

(d) performing an incremental routing of the integrated circuit design only for each net in the integrated circuit design that is enclosed by the window;

(e) replacing an area in a copy of the integrated circuit design that is bounded by the coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and

(f) generating as output the revised integrated circuit design.

35. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device design process, *e.g.*, providing a novel and substantially more efficient process flow in which only the affected nets would be considered in the incremental routing. This results in substantial reduction in the expected time of the design portion of producing semiconductor devices.

36. The claims of the '626 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to post-ECO routing. The claims of the '626 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the '626 patent specification, the claimed inventions improve upon the prior art processes by ignoring nets that are unaffected by an ECO in performing routing following the ECO. This has the advantage of substantially reducing the

impact on design schedule of ECOs and other layout changes, thus increasing the efficiency of the design process and making it easier to improve the design and fix design errors without unduly delaying time-to-market. By making it easier to fix errors as they are found, and causing substantially less incremental delay upon finding and fixing errors, the claimed inventive processes also increase the performance and reliability of the finished product. Because of the claimed inventive processes, individual less impactful design issues that still impact design performance (albeit not on a critical scale) can be caught and fixed without costing the same delay as more substantial errors.

U.S. PATENT NO. 7,396,760

37. Bell Semic is the owner by assignment of the '760 patent. The '760 patent is titled "Method and System for Reducing Inter-Layer Capacitance in Integrated Circuits."

38. A true and correct copy of the '760 patent is attached as Exhibit D.

39. The inventors of the '760 patent are Kunal Taravade, Neal Callan, and Paul Filseth.

40. The '760 patent issued on July 8, 2008 from an application filed on November 17, 2004.

41. The '760 patent generally relates to “a method for reducing inter-layer capacitance” in integrated circuits “through dummy fill methodology.” Ex. D at 1:8–10.

42. The background section of the '760 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior dummy fill methodologies were disadvantageous because they typically focused on achieving uniformity of feature density and failed to sufficiently address adverse effects of the dummy fill on electric field and unwanted bulk capacitance. *See* Ex. D at 1:62–66. In addition, these dummy fill methodologies only considered intralayer effects of dummy fill, to the extent that they considered timing impact at all. *See* Ex. D at 1:66–2:3. Thus, placement of dummy fill, even if advantageous on each individual layer, could create problems when it overlapped with dummy fill features on successive layers, introducing an additional bulk capacitance component that could be substantial. *See id.* at 4:11–17, 4:25–28. These methodologies failed to consider interlayer effects such as those caused by the overlap of dummy fill features in successive layers, which could have a substantial negative impact on timing. *See id.* at 2:3–6.

43. In light of the drawbacks of the prior art, the inventors of the '760 patent recognized a need for “intelligent dummy fill placement to reduce interlayer capacitance caused by overlaps of dummy fill area on successive layers,” which

would also “treat[] each consecutive pair of layers together when the intelligent dummy filling placement is performed.” Ex. D at 2:7–13. The inventions claimed in the ’760 patent address this need.

44. The ’760 patent contains two independent claims and 19 total claims.

Claim 1 reads:

1. A method for placing dummy fill patterns in an integrated circuit fabrication process, comprising:

obtaining layout information of the integrated circuit, the integrated circuit including a plurality of layers;

obtaining a first dummy fill space for a first layer based on the layout information;

obtaining a second dummy fill space for a second layer, the second layer being placed successively to the first layer;

determining an overlap between the first dummy fill space and the second dummy fill space; and

minimizing the overlap by re-arranging a plurality of first dummy fill features and a plurality of second dummy fill features,

wherein the first dummy fill space includes non-signal carrying lines on the first layer and the second dummy fill space includes non-signal carrying lines on the second layer.

45. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, minimizing interlayer bulk capacitance and thus improving the timing characteristics and performance of the

IC while meeting interconnect density requirements during processing. *See, e.g.*, Ex. D at 1:37–55, 5:19–39.

46. The claims of the '760 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to dummy filling. The claims of the '760 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the '760 patent specification, the claimed inventions improve upon the prior art processes by considering successive layers rather than each layer on its own, and then determining the overlap between dummy fill features on successive layers before rearranging them to minimize their overlap and thus reduce interlayer bulk capacitance. This has advantages such as minimizing the parasitic capacitance of the interconnect layers, especially the bulk capacitance contributed by the interlayer effects of overlapping dummy fill features, while maintaining necessary interconnect density to meet fabrication requirements.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,231,626

47. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

48. The '626 patent is valid and enforceable under the United States Patent Laws.

49. Bell Semic owns, by assignment, all right, title, and interest in and to the '626 patent, including the right to collect for past damages.

50. A copy of the '626 patent is attached at Exhibit A.

51. On information and belief, Socionext has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the '626 patent by using the patented methodology to design one or more semiconductor devices, including as one example the Socionext Accused Product, in the United States.

52. On information and belief, Socionext employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to perform incremental routing in implementing an ECO (the "Accused Processes") as recited in the '626 patent claims. As one example, Socionext's Accused Processes perform a method for only routing the nets affected by the ECO and merging that changed area into the overall circuit layout as required by claim 1 of the '626 patent. Socionext does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to perform incremental routing as part of implementing an ECO for the Socionext Accused Product to generate a revised integrated circuit design.

53. Socionext's Accused Processes also calculate and perform a parasitic extraction only for each net in the IC design enclosed by the window defining the ECO. (This parasitic extraction is also how the Accused Processes further calculate a net delay only for each net in the IC design enclosed by the window defining the

ECO.) Socionext does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to perform the incremental routing during implementation of the ECO for the Socionext Accused Product's circuit designs.

54. Socionext's Accused Processes also perform a design rule check only for each net in the IC design enclosed by the ECO window. Socionext does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, perform the incremental ECO and automatically perform a DRC for those nets to ensure that the ECO did not violate any design rules when it fixed other issues.

55. An exemplary infringement analysis showing infringement of one or more claims of the '626 patent is set forth in Exhibit B. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit C and further describes Socionext's infringement of the '626 patent.

56. Socionext's Accused Processes infringe and continue to infringe one or more claims of the '626 patent during the pendency of the '626 patent.

57. On information and belief, Socionext has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the '626 patent. Socionext has and continues to infringe pursuant to 35 U.S.C. §

271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the '626 patent.

58. Socionext's infringement of the '626 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

59. Bell Semic has been damaged by Socionext's infringement of the '626 patent and will continue to be damaged unless Socionext is enjoined by this Court. Bell Semic has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

60. Bell Semic is entitled to recover from Socionext all damages that Bell Semic has sustained as a result of Socionext's infringement of the '626 patent, including without limitation and/or not less than a reasonable royalty.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 7,396,760

61. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

62. The '760 patent is valid and enforceable under the United States Patent Laws.

63. Bell Semic owns, by assignment, all right, title, and interest in and to the '760 patent, including the right to collect for past damages.

64. A copy of the '760 patent is attached at Exhibit D.

65. On information and belief, Socionext has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the '760 patent by using the patented methodology to design one or more semiconductor devices, including as one example the Accused Product, in the United States.

66. On information and belief, Socionext employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to rearrange dummy fill to minimize its overlap in successive layers (the "Accused Processes") as recited in the '760 patent claims. As one example, Socionext's Accused Processes allow arrangement and rearrangement of dummy fill in a timing aware fashion, including with the ability to stagger the dummy fill in successive layers so as to minimize the interlayer bulk capacitance after determining their overlap as required by claim 1 of the '760 patent. Socionext does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, rearrange the dummy fill features in successive layers of its Accused Product.

67. Socionext's Accused Processes also form the dummy fill features in a grid within one or more of the successive layers, provide square-shaped dummy fill features in one or more of the successive layers, determine the dummy fill space

based on a local pattern density in one or more of the successive layers, and minimize total bulk capacitance and/or certain of its components. Socionext does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to implement dummy fill functionality in a timing-aware fashion and with consideration of interlayer capacitive effects in creation and design of its Accused Product.

68. An exemplary infringement analysis showing infringement of one or more claims of the '760 patent is set forth in Exhibit E. The declaration of Dhaval Brahmhatt, an expert in the field of semiconductor device design, is attached at Exhibit F and further describes Socionext's infringement of the '760 patent.

69. Socionext's Accused Processes infringe and continue to infringe one or more claims of the '760 patent during the pendency of the '760 patent.

70. On information and belief, Socionext has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the '760 patent. Socionext has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the '760 patent.

71. Socionext's infringement of the '760 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

72. Bell Semic has been damaged by Socionext's infringement of the '760 patent and will continue to be damaged unless Socionext is enjoined by this Court. Bell Semic has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

73. Bell Semic is entitled to recover from Socionext all damages that Bell Semic has sustained as a result of Socionext's infringement of the '760 patent, including without limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

- (a) a judgment declaring that Socionext has infringed one or more claims of the '626 patent and '760 patent in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;
- (b) an award of damages adequate to compensate Bell Semic for infringement of the '626 patent and '760 patent by ASMedia, in an amount to be proven at trial, including supplemental post-verdict damages until such time as Socionext ceases its infringing conduct;
- (c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting Socionext and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others

acting in privity with Socionext from committing further acts of infringement;

- (d) a judgment requiring Socionext to make an accounting of damages resulting from Socionext's infringement of the '626 patent and '760 patent;
- (e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;
- (f) pre-judgment and post-judgment interest at the maximum amount permitted by law;
- (g) all other relief, in law or equity, to which Bell Semic is entitled.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: November 14, 2022

s/ Patrick G. Seyferth

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