IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

OAK IP, LLC, Plaintiff, v. GLOBALFOUNDRIES INC. AND GLOBALFOUNDRIES U.S., INC., Defendants.	§	CIVIL ACTION NO. _____ **JURY TRIAL DEMANDED**

PLAINTIFF'S ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Oak IP, LLC ("Oak" or "Plaintiff") files this Original Complaint against Defendants GlobalFoundries Inc. ("GF") and GlobalFoundries U.S., Inc. ("GF U.S.") (collectively, "Defendants" or "GlobalFoundries") and alleges at follows:

NATURE OF THE ACTION

1. This is a civil action for patent infringement (hereinafter the "Action"), brought under the patent laws of the United States, 35 U.S.C. §§ 271, *et seq.*, seeking damages and other relief arising out of GlobalFoundries' infringement of United States Patent No. 9,905,691 (the "'691 Patent"); United States Patent No. 10,090,395 (the "'395 Patent"); and United States Patent No. 10,937,880 (the "'880 Patent" and collectively, the "Asserted Patents" or "Patents-in-Suit"). Plaintiff owns the entire right, title, and interest in and to each of the Asserted Patents.

2. Plaintiff asserts that GlobalFoundries infringes each Asserted Patent by, without Plaintiff's authorization, making, offering to sell, selling, and/or importing into the United States the Accused Products (as defined below) intended for inclusion in processors and/or encouraged others to use their products and services in an infringing manner, as set forth herein.

THE PARTIES

3. Plaintiff Oak IP, LLC is Texas limited liability corporation located at 812 W. McDermott Dr., #1026, Allen, Texas 75013.

4. On information and belief Defendant GF is a corporation organized under the laws of the Cayman Islands with a registered legal address at P.O. Box 309, Ugland House, George Town KY1-1104, Cayman Islands.

5. On information and belief, Defendant GF U.S. is a corporation organized under the laws of Delaware that maintains an established place of business at 400 Stonebreak Road Ext., Malta, NY 12020. GF U.S. may be served with process through its registered agent, Corporation Service Company, 251 Little Falls Drive, Wilmington DE 19808.

6. On information and belief, GF U.S. is a wholly owned subsidiary of GF.

7. On information and belief, GlobalFoundries has semiconductor fabrication plants in the United States and other countries throughout the world and manufactures chips, including the Accused Products, for later integration into processors at those plants. GlobalFoundries also sells the Accused Products in the United States, offers for sale the Accused Products in the United States, and/or imports the Accused Products into the United States. Defendants have at least imported, advertised, distributed, sold, and/or offered to sell products, including the Accused Products, in this District, e.g., through sales and distribution channels owned, managed, and/or used by Defendants.

8. On information and belief, GlobalFoundries places, has placed, and/or contributed to placing Accused Products into the stream of commerce via an established distribution channel knowing or understanding that such Accused Products would be sold in the United States, including in this District. GlobalFoundries has also derived substantial revenues from infringing acts in this District, including from the sale of the Accused Products.

JURISDICTION AND VENUE

9. This is an Action for patent infringement, which arises under the patent laws of the United States; in particular, 35 U.S.C. §§ 271, 281, 283, 284, and 285. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331, 1332, 1338(a) and 1367.

10. This Court has specific and personal jurisdiction over Defendants consistent with the requirements of the Due Process Clause of the United States Constitution and the Delaware Long Arm Statute at least because Defendants have committed, directly or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), acts of patent infringement in this State and/or the United States. *See 10 Del C.* § 3104(c); *see also Power Integrations, Inc. v. BCD Semiconductor Corp.*, 547 F. Supp. 2d 365, 373 (D. Del. Apr. 11, 2008) ("A non-resident firm's intent to serve the United States market is sufficient to establish an intent to serve the Delaware market, unless there is evidence that the firm intended to exclude from its marketing and distribution efforts some portion of the country that includes Delaware."). Such acts of infringement include making, offering to sell, and/or selling the Accused Products in the United States, this State, and this District and/or importing the Accused Products into the United States and this State. Indeed, Defendants have purposefully and voluntarily placed, and is continuing to place, one or more Accused Products into the stream of commerce through established distribution channels (including the Internet) with the expectation and intent that such products will be sold to and purchased by consumers in the United States, this State, and this District; and with the knowledge and expectation that such products (whether in standalone form or as integrated in downstream products) will be imported into the United States, this State, and this District.

11. Moreover, GF U.S. is incorporated in this District, thus signifying its consent to the laws of this District's state and courts. GF U.S. has also availed itself of this forum by bringing multiple patent infringement actions in this District to enforce its own patents. *See, e.g.*, 1:19-cv-01571; 1:19-cv-01572; 1:19-cv-01573; 1:19-cv-01574; 1:19-cv-01575; 1:19-cv-01576. These are purposeful acts and transactions in this State and this District such that Defendants reasonably should know and expect that they could be hailed into this Court because of such activities.

12. Defendants have derived substantial revenues from its infringing acts occurring within the United States, this State, and this District. It has substantial business in the United States, this State, and this District, including: (i) at least part of its infringing activities alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent conduct, and/or deriving substantial revenue from infringing goods offered for sale, sold, and imported to Delaware residents vicariously through and/or in concert with its alter egos, intermediaries, agents, distributors, importers, customers, subsidiaries, and/or consumers.

13. This Court has personal jurisdiction over Defendants, directly or through intermediaries (e.g., subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), including its U.S.-based subsidiaries. Through direction and control of such subsidiaries, Defendants have committed acts of direct patent infringement within this State and elsewhere within the United States giving rise to this action and/or has established minimum contacts with this forum such that the exercise of personal jurisdiction over Defendants would not offend traditional notions of fair play and substantial justice. On information and belief, GF U.S. is a wholly-owned subsidiary of GF. On information and belief, the primary business of GF U.S. is the fabrication of semiconductors, specifically chips for integration into processors, in the United States. On information and belief, GF has a direct financial interest in GF U.S., and vice versa. For

example, GF does not separately report revenue from GF U.S. in its filings to the Securities Exchange Commission, but rather reports combined revenue from its various subsidiaries. As a further example, the U.S. Commerce Department awarded a $1.5 billion government subsidy to GF to expand semiconductor production in Malta, New York and Vermont.[1] GF has also stated that it will invest $13 billion over the next 10 plus years in its U.S. manufacturing sites.[2]

14. On information and belief, GF controls and otherwise directs and authorizes all activities of its U.S.-based sales subsidiaries, including GF U.S. Such directed and authorized activities include the U.S.-based subsidiaries offering for sale, selling, and/or importing the Accused Products, their components, and/or products containing the same that incorporate and/or perform the fundamental technologies covered by the Asserted Patents. On information and belief, GF's U.S.-based subsidiaries, including GF U.S., are expressly authorized to import, distribute, offer to sell, and sell the Accused Products on behalf of GF. For example, on information and belief, GF directs its U.S.-based subsidiaries, including GF U.S., to generally conduct themselves as GF and develop, manufacture, import, distribute, offer for sale, and/or sell Accused Products in the United States. GF's website indicates that it has multiple United States locations:

[1] *See* https://www.reuters.com/technology/us-finalizes-15-billion-chips-award-globalfoundries-expand-production-2024-11-20/?utm_source=chatgpt.com.
[2] *See id.*

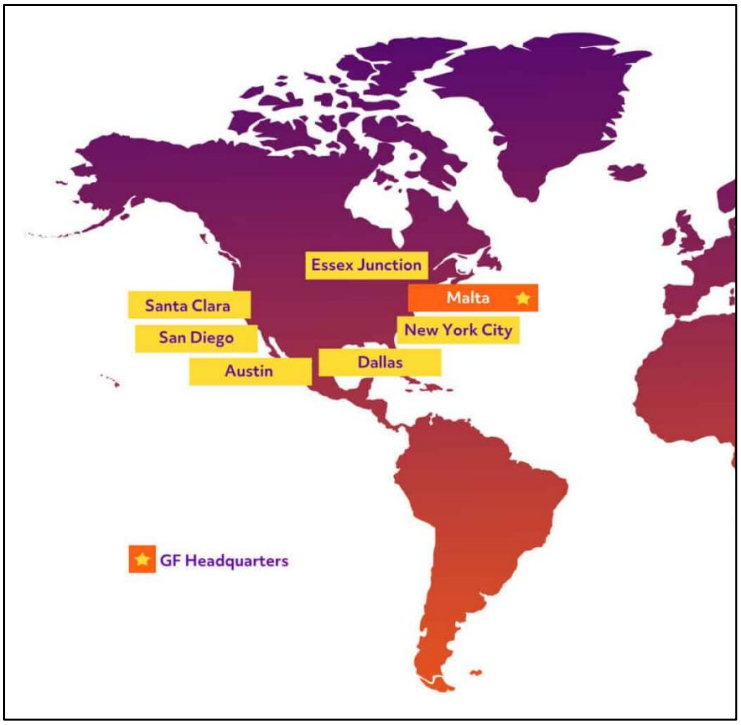

Figure 1.[3]

In particular, GF's website indicates its Malta location is at 400 Stonebreak Road Ext., Malta, NY 12020.

Figure 2.[4]

[3] https://gf.com/about-us/contact-us/worldwide-locations/.
[4] *Id.*

And Saratoga County's publicly available online property search indicates GF U.S. owns the property at the same address:

SWIS - Municipality	Tax ID	Owner	Street #	Street Name
414089 - Malta	230.-1-72.12	GlobalFoundries US Inc.	400	Stonebreak Rd

Figure 3.[5]

GF's website makes no such distinction between itself and GF U.S. or any of its additional U.S.-based subsidiaries. Nor does the same online property search indicate that GF owns any property in Malta, New York:

SWIS - Municipality	Tax ID	Owner	Street #	Street Name
414089 - Malta	230.-1-72.12	GlobalFoundries US Inc.	400	Stonebreak Rd
414089 - Malta	230.-1-72.111	GlobalFoundries Innovation LLC		Ermine Lair
414089 - Malta	230.-1-72.112	GlobalFoundries Innovation LLC		Route 9P
414089 - Malta	230.-1-76.111	GlobalFoundries Innovation LLC		Rocket Dr
414089 - Malta	230.-1-76.112	GlobalFoundries Innovation LLC		Luther Forest Boulevard Ext
414089 - Malta	230.-1-91	GlobalFoundries US Inc		Cold Spring Road Rear
415289 - Stillwater	241.-1-4	GlobalFoundries Innovation LLC	40	Substation Dr
415289 - Stillwater	241.-1-5	GlobalFoundries Innovation LLC		Luther Forest Boulevard Ext
414089 - Malta	241.-1-48	GlobalFoundries Innovation LLC	100	Stonebreak Rd Ext
414089 - Malta	241.-1-49	GlobalFoundries Innovation LLC	300	Luther Forest Blvd W
414089 - Malta	241.-1-50.1	GlobalFoundries Innovation LLC	20	Rocket Dr
414089 - Malta	241.-1-50.2	GlobalFoundries Innovation LLC	16	Rocket Dr
414089 - Malta	241.-1-51	GlobalFoundries Innovation LLC	30	Rocket Dr
414089 - Malta	241.-1-52	GlobalFoundries Innovation LLC	200	Luther Forest Blvd W
414089 - Malta	241.-1-53	GlobalFoundries Innovation LLC	2300	100 Acre Woods Way
414089 - Malta	241.-1-55	GlobalFoundries Innovation LLC	40	Rocket Dr

Figure 4.[6]

Nonetheless, GF represents to the public that it manufactures chips at the Malta, New York location.[7] Thus, GF's U.S.-based subsidiaries, including GF U.S., conduct infringing activities on GF's behalf.

15. On information and belief, because GF's U.S.-based subsidiaries are authorized by GF to make, import, distribute, offer to sell, and sell Accused Products, GF's U.S.-based

[5] https://saratoga.sdgnys.com/viewlist.aspx?sort=printkey&swis=all&ownernamel=Globalfoundries&advanced=true.
[6] *Id.*
[7] https://gf.com/gf-press-release/globalfoundries-moves-corporate-headquarters-its-most-advanced-semiconductor/.

subsidiaries' corporate presences in the United States give GF substantially the same business advantages it would enjoy if it conducted its business through its own offices and personnel.

16. Defendants have, thus, in the multitude of ways described above, availed themselves of the benefits and privileges of conducting business in this State and willingly subjected themselves to the exercise of this Court's personal jurisdiction. Indeed, Defendants have sufficient minimum contacts with this forum through their transaction of substantial business in the United States, this State, and this District and their commission of acts of patent infringement as alleged in this Complaint that are purposefully directed towards the United States, this State, and this District.

17. Alternatively, the Court maintains personal jurisdiction over GF under Federal Rule of Civil Procedure 4(k)(2).

18. Venue is proper in this District for GF pursuant to 28 U.S.C. § 1391 because, among other things, GF is not a resident of the United States, and thus may be sued in any judicial district, including this one, pursuant to 28 U.S.C. § 1391(c)(3). *See In re HTC Corp.*, 889 F.3d 1349, 1357 (Fed. Cir. 2018) (holding that "[t]he Court's recent decision in TC Heartland does not alter" the alien-venue rule).

19. Venue is proper in this District for GF U.S. pursuant to 28 U.S.C. § 1400(b) which states "[a]ny civil action for patent infringement may be brought in the judicial district where the defendant resides." GF U.S. is incorporated in this District. *See TC Heartland LLC v. Kraft Foods Grp. Brands LLC*, 581 U.S. 258, 270 (2017) ("As applied to domestic corporations, 'reside[nce]' in §1400(b) refers only to the State of incorporation.").

THE ASSERTED PATENTS

20. Plaintiff is the sole and exclusive owner of all right, title, and interest in the '691 Patent, '395 Patent, and '880 Patent and holds the exclusive right to take all actions necessary to enforce its rights in, and to, the Asserted Patents, including the filing of this patent infringement lawsuit. Plaintiff also has the right to recover all damages for past, present, and future infringements of the Asserted Patents and to seek injunctive relief as appropriate under the law.

21. The '691 Patent is titled "Method for Depinning the Fermi Level of a Semiconductor at an Electrical Junction and Devices Incorporating Such Junctions." The '691 patent lawfully issued on February 27, 2018, and stems from U.S. Patent Application No. 15/048,877, which was filed on February 19, 2016. A true and correct copy of the '691 patent is attached hereto as Exhibit 1.

22. The '395 Patent is titled "Method for Depinning the Fermi Level of a Semiconductor at an Electrical Junction and Devices Incorporating Such Junctions." The '395 patent lawfully issued on October 2, 2018, and stems from U.S. Patent Application No. 15/877,837, which was filed on January 23, 2018. A true and correct copy of the '395 patent is attached hereto as Exhibit 2.

23. The '880 Patent is titled "Method for Depinning the Fermi Level of a Semiconductor at an Electrical Junction and Devices Incorporating Such Junctions." The '880 Patent lawfully issued on March 2, 2021, and stems from U.S. Patent Application No. 15/929,592, which was filed on May 12, 2020. A true and correct copy of the '880 patent is attached hereto as Exhibit 3.

24. Plaintiff and its predecessors complied with the requirements of 35 U.S.C. § 287, to the extent necessary, such that Plaintiff may recover pre-suit damages dating six years from the date of the filing of this Complaint.

25. The claims of the Asserted Patents are directed to patent eligible subject matter under 35 U.S.C. § 101. They are not directed to an abstract idea, and as detailed below, the technologies covered by the claims comprise devices, systems and/or consist of ordered combinations of features and functions that, at the time of invention, were not, alone or in combination, well-understood, routine, or conventional.

26. The inventions claimed in the Asserted Patents relate generally to semiconductor processing and semiconductor devices. (*See, e.g.*, '691 Patent, 1:25-26.)[8] In particular, the inventions relate to "a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction." (*Id.* at 1:26-29.) These innovations have enabled the design and manufacture of chips for computers and mobile devices that are smaller, faster, lighter, and more efficient than ever before.

27. Semiconductor devices are ubiquitous in modern electronic systems. They are electronic components that utilize the electronic properties of semiconductor materials (typically silicon, germanium, or gallium arsenide) in order to control electrical conduction. Controlling the conduction of electricity through semiconductors forms the basis of diodes, transistors, and logic gates, all of which are fundamental to modern electronic circuits or integrated circuits.

28. Semiconductor materials have an electrical conductivity falling somewhere between that of a conductor (such as copper) and an insulator (such as glass). Semiconductor materials are useful because their conducting behavior can be manipulated. For example, semiconductor devices may be designed to provide a specific level of electrical resistance, to allow current to pass more easily in one direction than another, or to show sensitivity to light or heat.

[8] For convenience and readability, Plaintiff cites herein to the '691 Patent, which shares a virtually identical specification with all of the Asserted Patents.

29. Metal-semiconductor junctions are a type of electrical junction in which a metal comes in close contact with a semiconductor material. (*See id.* at 1:33-36.) These junctions can be inherently rectifying, which means that they will tend to conduct current in one direction more favorably than in the other direction. (*See id.* at 1:36-39.) One researcher, Walter H. Schottky, described this rectifying behavior in the 1930s as depending on a "barrier" at the surface of contact between the metal and the semiconductor. (*See id.* at 1:46-48.) The height of the "barrier," in Schottky's model, was measured by the energy needed to move an electron between the metal and the semiconductor. (*See id.* at 1:49-63.) This became known as the "Schottky barrier." Schottky predicted that the height of the Schottky barrier, Φb, could be measured by the difference between (i) the work function of the metal Φm (the amount of energy needed to remove an electron from the metal to a point in the vacuum immediately outside the metal) and (ii) the electron affinity of the semiconductor Xs (the difference between the energy of a free electron and the conduction band edge of the semiconductor). (*See id.*) Expressed mathematically, his theory was as follows: Φb= Φm-Xs. *See id.* The below energy-band diagram illustrates the values that make up Schottky's formula:

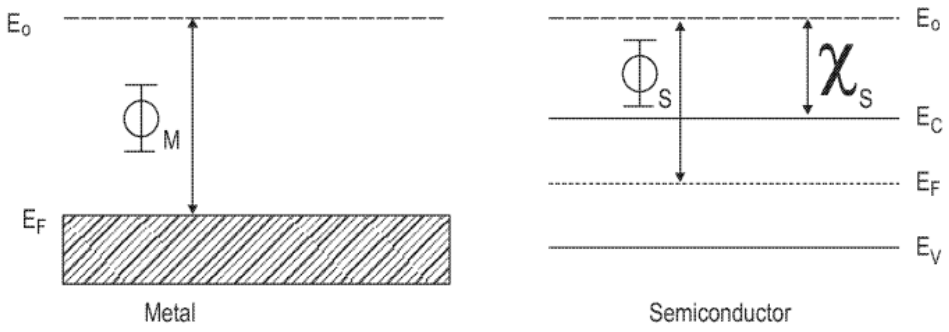

Figure 5.[9]

[9] '691 Patent, Figure 2.

30. Schottky was wrong. The Schottky barrier at a metal-semiconductor junction is generally different than Schottky's equation would predict. (*See id.* at 1:64-2:3.) The energy-band diagram below illustrates an increased Schottky barrier at a metal-semiconductor junction:

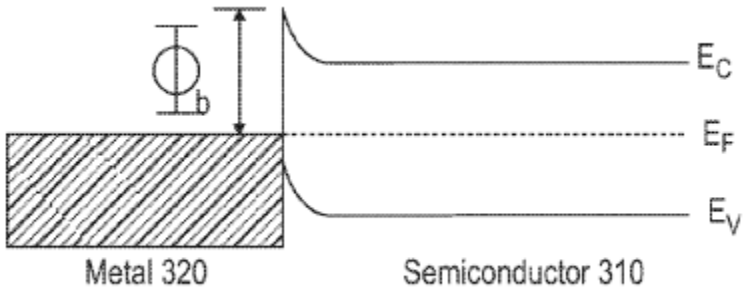

Figure 6.[10]

31. The Asserted Patents explain that "a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, [metal induced gap states] and inhomogeneities." (*Id.* at 2:67-3:3.) According to the Asserted Patents, "[t]he importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of designer characteristics. Such barrier height tuning may become even more important as device sizes shrink even further." (*Id.* at 3:4-10.)

32. In or around 2002, researchers attempting to minimize contact resistance at a metal-semiconductor junction in a semiconductor device generally used three techniques: (i) doping the silicon at the interface to the greatest extent possible; (ii) maximizing the area of the metal-semiconductor junction within the geometric constraints of a particular node; and (iii) making the connection between the metal and the semiconductor as direct as possible by eliminating any oxide

[10] '691 Patent, Figure 4.

layer that might naturally occur between the metal and the semiconductor. While these techniques were mostly workable for the size of semiconductor devices in 2002, it was clear to inventors Dr. Daniel E. Grupp and Dr. Daniel J. Connelly that these techniques would not sufficiently minimize contact resistance for progressively smaller semiconductor devices. Dr. Grupp and Dr. Connelly applied their considerable expertise and experience to the problem.

33. Around this time, Dr. Grupp and Dr. Connelly were working to develop a new type of field-effect transistor ("FET") that they hoped would be smaller and faster than prior FETs. A FET is a semiconductor device that has three terminals and uses an electric field to control the flow of current through the device. The three terminals are the source, the gate, and the drain. Applying a voltage to the gate alters the conductivity between the source and the drain, either by inducing a conductive channel that allows current to flow between them, or by stopping current flow through the channel between them, depending on the type of FET.

34. The FET that Dr. Grupp and Dr. Connelly were working on required source and drain portions made of metal. The channel portion of their device was made of silicon. The design thus included two metal-silicon junctions, one between the source and the channel, and another between the channel and the drain.

35. With two metal-silicon junctions in their design, Dr. Grupp and Dr. Connelly had to contend with a Schottky barrier at both junctions. And these Schottky barriers severely limited the functionality of the device Dr. Grupp and Dr. Connelly were developing. The device Dr. Grupp and Dr. Connelly were developing required less resistance at the source/channel and channel/drain interfaces. So, Dr. Grupp and Dr. Connelly worked to find a way to reduce the Schottky barriers.

36. Dr. Grupp and Dr. Connelly knew that inserting an insulating interface layer between a metal and a semiconductor could be used to reduce a Schottky barrier. For example, an

insulating interface layer can reduce a Schottky barrier because it "depins" the Fermi level of the conductor from a point between the valence and conduction bands of the semiconductor. But an insulating interface layer was not generally considered to be a solution for applications where the goal was to reduce resistance in a design. This is because adding an insulating layer between a metal and a semiconductor typically increases resistance in the design. The idea of adding an insulator to reduce resistance is counterintuitive.

37. At this point, Dr. Grupp and Dr. Connelly came to a remarkable insight that no one in the art had yet reached. They theorized that there may be a way to balance the potential Schottky-barrier reduction that would result from adding an insulating interface layer between the metal and the semiconductor with the increased resistance that would result from adding that insulating interface layer. As shown in the below figure, they theorized that there might be a specific interface-layer thickness that was thick enough to effectively reduce the Schottky barrier, while still being thin enough to avoid introducing too much resistance into the design. They hoped that a low point for contact resistance—such as in the figure below—might exist at a certain interface-layer thickness.

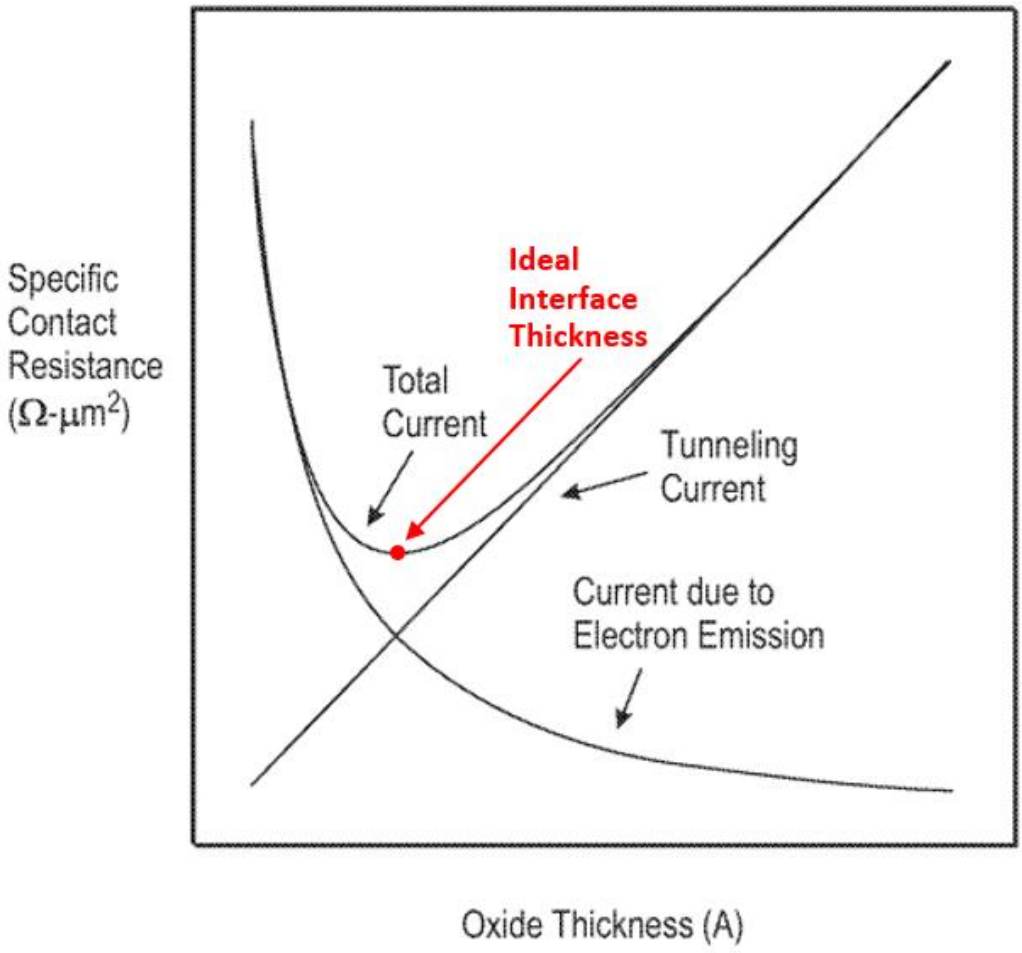

Figure 7.[11]

38. Experimentation and modeling confirmed their theory. Dr. Grupp and Dr. Connelly found that inserting a very thin insulating interface layer between a metal and a semiconductor could in fact reduce resistance across the contact. In their early experiments, performed with Aluminum-Insulator-Silicon junctions, Dr. Grupp and Dr. Connelly found a contact resistance that was 10,000x lower than it was without the insulator. This remarkable result occurred at such a specific and difficult-to-create interface thickness that it would not have been found had Dr. Grupp and Dr. Connelly not been looking specifically for it. Their discovery—which allows the

[11] '691 Patent, Figure 8 (emphasis added).

production of more effective semiconductor devices—underlies the inventions claimed in the Asserted Patents.

39. When Dr. Grupp and Dr. Connelly published their insight and results, they received widespread industry recognition. And, as the inventors correctly predicted, their innovations have become even more important as electronic devices have continued to shrink.

THE ACCUSED PRODUCTS

40. GlobalFoundries makes, sells, offers for sale, and/or imports certain chips that incorporate the fundamental technologies covered by the Asserted Patents including, but not limited to (i) chips/products manufactured via GlobalFoundries' 14 nm FinFET fabrication process; (ii) chips/products manufactured via GlobalFoundries' 12 nm FinFET fabrication process; and (iii) other chips/products that have been manufactured via the same or similar processes by GlobalFoundries (collectively, the "Accused Products").

41. On information and belief, GlobalFoundries partners with at least Advanced Micro Devices, Inc. ("AMD") to, in turn, integrate these chips into certain processors including, but not limited to, the (i) AMD Radeon RX 480; (ii) AMD Ryzen 5 2600; and (iii) AMD Ryzen 5 1600 AF. For example, on November 5, 2015, GlobalFoundries announced that it had "demonstrated silicon success on the first AMD (NASDAQ: AMD) products using GF's most advanced 14nm FinFET process technology. As a result of this milestone, GF's silicon-proven technology is planned to be integrated into multiple AMD products that address the growing need for high-performance, power-efficient compute and graphics technologies across a broad set of applications, from personal computers to data centers to immersive computing devices."[12]

[12] https://gf.com/gf-press-release/globalfoundries-achieves-14nm-finfet-technology-success-next-generation-amd-products/.

42. On information and belief, GlobalFoundries manufactured and/or continues to manufacture chips at its Fab 8 facility in New York using its 14nm FinFET fabrication process.[13] These chips have been and/or continue to be integrated into at least the AMD Radeon RX 480 processor:

	AMD Radeon RX 480 (8GB)	AMD Radeon RX 480 (4GB)
Stream Processors	2304 (36 CUs)	
Texture Units	144	
ROPs	32	
Base Clock	1120MHz	
Boost Clock	1266MHz	
Memory Clock	7-8 Gbps GDDR5	7Gbps GDDR5
Memory Bus Width	256-bit	
VRAM	8GB	4GB
Transistor Count	5.7B	
Typical Board Power	150W	
Manufacturing Process	GloFo 14nm FinFET	
Architecture	GCN 4	
GPU	Polaris 10	
Launch Date	06/29/16	
Launch Price	$239	$199

Figure 8.[14]

43. Further, on information and belief, at least as early as September 2017, GlobalFoundries began developing a 12nm FinFET fabrication process.[15] On information and belief, GlobalFoundries manufactured and/or continues to manufacture chips at its Fab 8 facility

[13] *See id.*; https://www.anandtech.com/show/12438/the-future-of-silicon-an-exclusive-interview-with-dr-gary-patton-cto-of-globalfoundries.
[14] https://www.anandtech.com/show/10446/the-amd-radeon-rx-480-preview.
[15] *See* https://gf.com/blog/gfs-12lp-process-behind-covers/.

in New York using its 12nm fabrication process.[16] These chips have been and/or continue to be integrated into at least the AMD Ryzen 5 2600 and AMD Ryzen 5 1600 AF processors.[17] On information and belief, the Accused Products are also integrated into additional processors.

COUNT I

(Infringement Of U.S. Patent No. 9,905,691)

44. Plaintiff incorporates the preceding paragraphs herein by reference.

45. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

46. Plaintiff is the owner of all substantial rights, title, and interest in and to the '691 patent including the right to exclude others and to enforce, sue, and recover damages for past infringements.

47. The '691 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on February 27, 2018, after full and fair examination.

48. GlobalFoundries directly infringed one or more claims of the '691 Patent in this District and elsewhere in Delaware and the United States by making, selling, offering to sell, and/or importing the Accused Products.

[16] *See id.*; https://www.anandtech.com/show/12438/the-future-of-silicon-an-exclusive-interview-with-dr-gary-patton-cto-of-globalfoundries.

[17] *See* https://www.tomshardware.com/reviews/amd-ryzen-5-2600,5625.html; https://www.anandtech.com/show/11854/globalfoundries-adds-12lp-process-tech-amd-first-customer; https://www.anandtech.com/show/12625/amd-second-generation-ryzen-7-2700x-2700-ryzen-5-2600x-2600; https://www.techpowerup.com/cpu-specs/ryzen-5-2600.c2015; https://www.anandtech.com/show/12625/amd-second-generation-ryzen-7-2700x-2700-ryzen-5-2600x-2600/2.

49. GlobalFoundries directly infringed, either by itself or via its agent(s), at least claim 19 of the '691 Patent[18] as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the Accused Products.

50. By way of illustration only, each Accused Product comprises each and every element of claim 19 of the '691 Patent. On information and belief, each Accused Product comprises "a semiconductor region in a substrate." For example, each Accused Product comprises an n-doped silicon semiconductor region. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, this n-doped silicon semiconductor region can be seen in maroon:

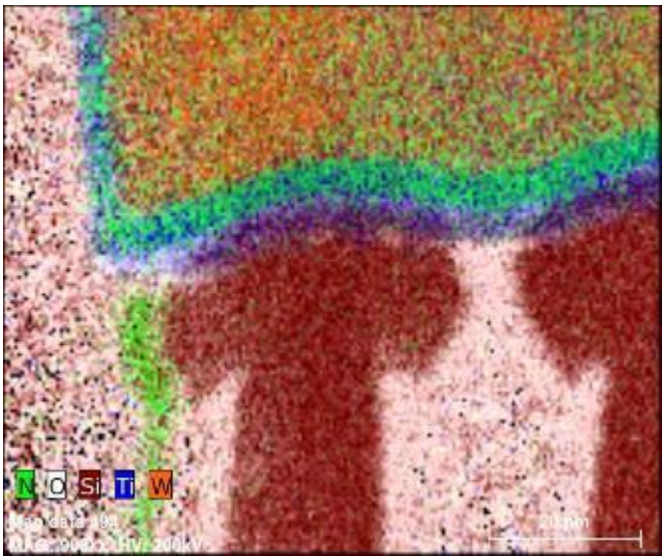

Figure 9.

51. On information and belief, each Accused Product comprises "a metal electrical contact to said semiconductor region." For example, each Accused Product comprises a tungsten and titanium nitride metal electrical contact to the n-doped silicon semiconductor region. In the

[18] Throughout this Complaint, wherever Plaintiff identifies specific claims of the Asserted Patents infringed by Defendants, Plaintiff expressly reserves the right to identify additional claims and products in its infringement contentions in accordance with applicable local rules and the Court's case management orders. Specifically identified claims throughout this Complaint are provided for notice pleading only.

microscopic image below of a chip from the AMD Ryzen 5 1600 AF, this tungsten and titanium nitride metal contact can be seen in orange, green, and blue:

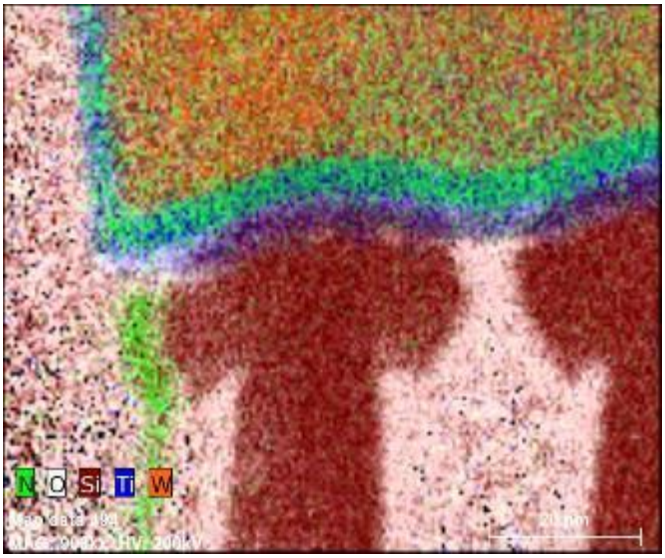

Figure 10.

52. On information and belief, each Accused Product comprises "a passivating dialectic tunnel barrier layer between said semiconductor region and said metal electrical contact." For example, each Accused Product comprises a passivating dielectric tunnel barrier layer of titanium silicon oxide and silicon oxide located between the n-doped silicon semiconductor region and the tungsten and titanium nitride metal contact. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, this passivating dielectric tunnel barrier layer of titanium silicon oxide and silicon oxide can be seen in purple and pink (or maroon-white) between the tungsten and titanium nitride metal contact and the n-doped silicon semiconductor region:

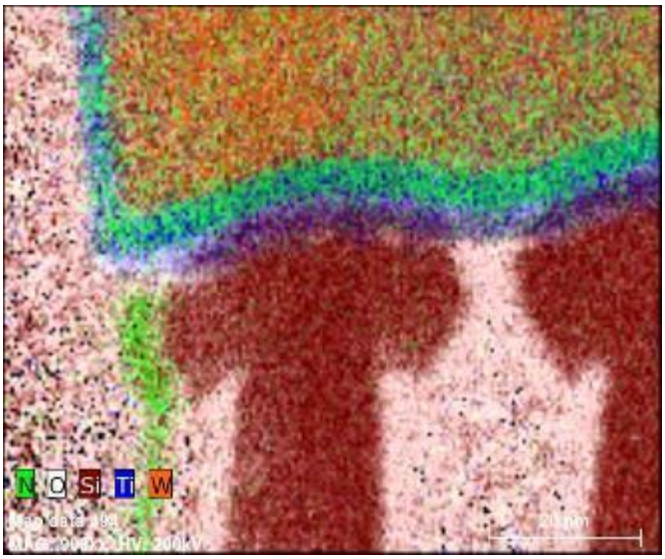

Figure 11.

53. On information and belief, each Accused Product comprises the semiconductor region being electrically connected to the metal electrical contact through the passivating dielectric tunnel barrier layer. For example, each Accused Product comprises a passivating dielectric tunnel barrier layer of titanium silicon oxide and silicon oxide located between the n-doped silicon semiconductor region and the tungsten and titanium nitride metal contact such that the n-doped silicon semiconductor region and the tungsten and titanium nitride metal contact are electrically connected to allow for the flow of an electric current. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, this passivating dielectric tunnel barrier layer of titanium silicon oxide and silicon oxide can be seen in purple and pink (or maroon-white) between the tungsten and titanium nitride metal contact and the n-doped silicon semiconductor region:

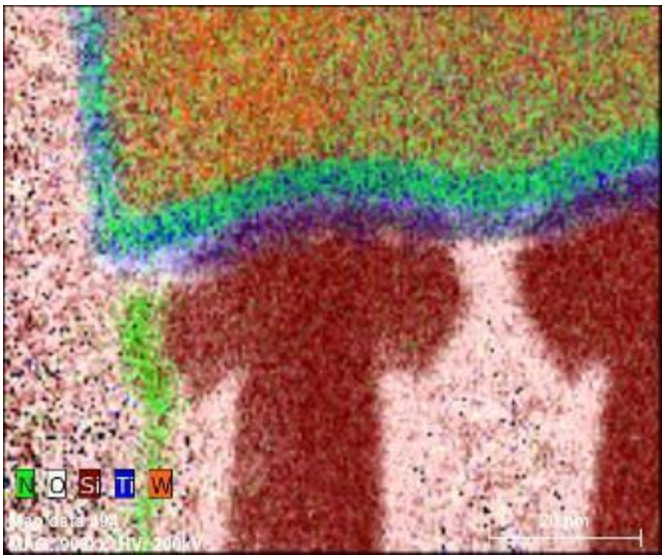

Figure 12.

54. On information and belief, each Accused Product comprises the passivating dielectric tunnel barrier layer that itself comprises a metal oxide and a semiconductor oxide. For example, and as detailed above, each Accused Product comprises a passivating dielectric tunnel barrier layer of titanium silicon oxide and silicon oxide. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, this passivating dielectric tunnel barrier layer of titanium silicon oxide and silicon oxide can be seen in purple and pink (or maroon-white):

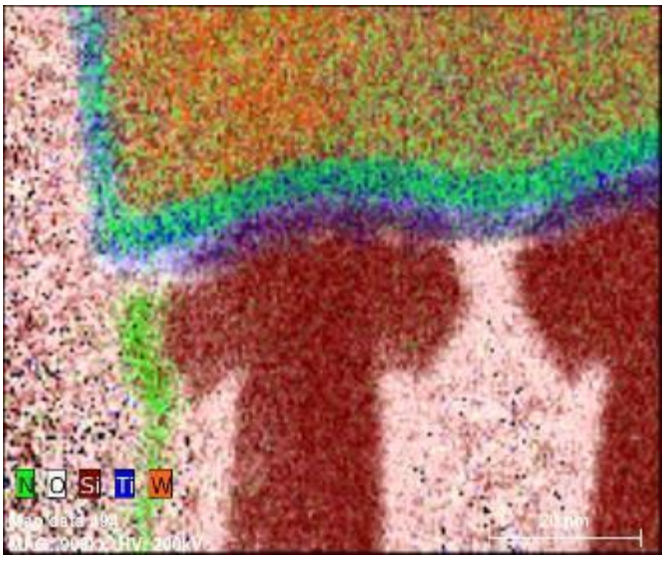

Figure 13.

55. On information and belief, each Accused Product comprises the semiconductor region that itself comprises silicon. For example, and as detailed above, each Accused Product comprises an n-doped semiconductor region. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, this n-doped silicon semiconductor region can be seen in maroon:

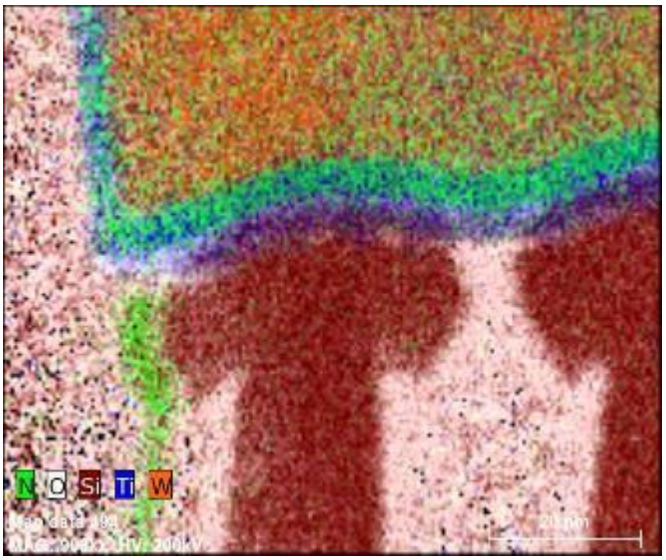

Figure 14.

56. On information and belief, each Accused Product also comprises the semiconductor oxide that itself comprises an oxide of silicon. For example, and as detailed above, each Accused Product comprises a dielectric tunnel barrier layer of titanium silicon oxide and silicon oxide. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, this dielectric tunnel barrier layer of titanium silicon oxide and silicon oxide can be seen in purple and pink (or maroon-white):

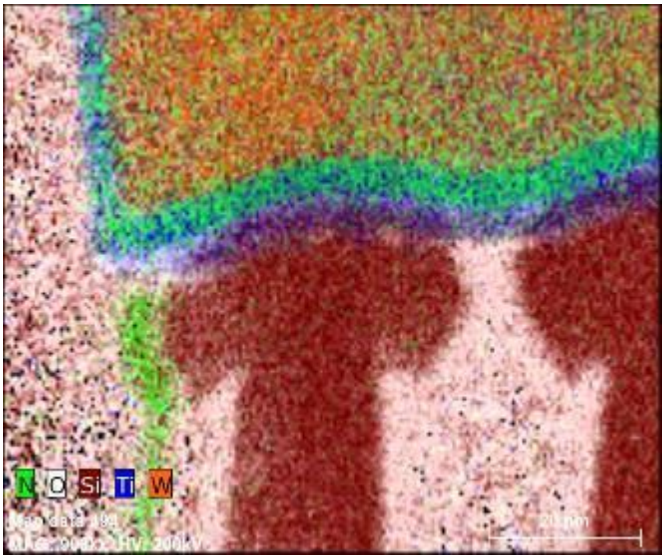

Figure 15.

57. On information and belief, each Accused Product also comprises the dielectric tunnel barrier layer that itself comprises an oxide of titanium. For example, and as detailed above, each Accused Product comprises a dielectric tunnel barrier of, in part, titanium silicon oxide. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, this dielectric tunnel barrier layer of, in part, titanium silicon oxide can be seen in purple:

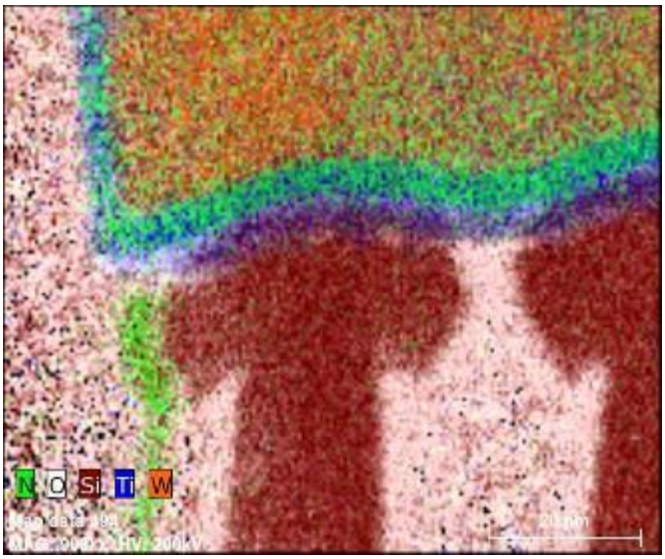

Figure 16.

58. On information and belief, each Accused Product also comprises the metal electrical contact that itself comprises titanium. For example, and as detailed above, each Accused Product comprises a metal electrical contact of, in part, titanium. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, the titanium portion of the metal contact can be seen in blue:

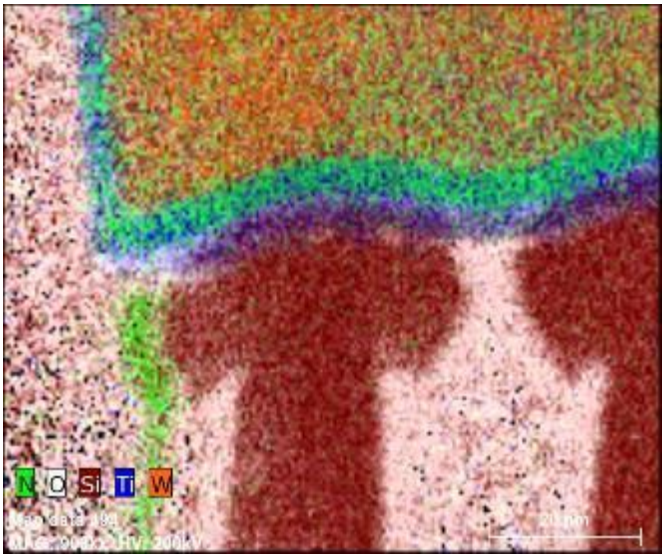

Figure 17.

59. Plaintiff has been damaged as a result of GlobalFoundries' infringing conduct described in this Count. GlobalFoundries is, thus, liable to Plaintiff in an amount that adequately compensates Plaintiff for GlobalFoundries's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT II

(Infringement Of U.S. Patent No. 10,090,395)

60. Plaintiff incorporates the preceding paragraphs herein by reference.

61. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

62. Plaintiff is the owner of all substantial rights, title, and interest in and to the '395 Patent including the right to exclude others and to enforce, sue, and recover damages for past infringements.

63. The '395 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on October 2, 2018, after full and fair examination.

64. GlobalFoundries directly infringed one or more claims of the '395 Patent in this District and elsewhere in Delaware and the United States by making, selling, offering to sell, and/or importing the Accused Products.

65. GlobalFoundries directly infringed, either by itself or via its agent(s), at least claim 17 of the '395 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the Accused Products.

66. By way of illustration only, each Accused Product comprises each and every element of claim 17 of the '395 Patent. On information and belief, each Accused Product comprises "a source or drain of a transistor, said source or drain comprising a semiconductor." For example, each Accused Products comprises a silicon semiconductor source or drain where the

electrical current enters (source) and exits (drain). In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, the silicon semiconductor source/drain can be seen in maroon:

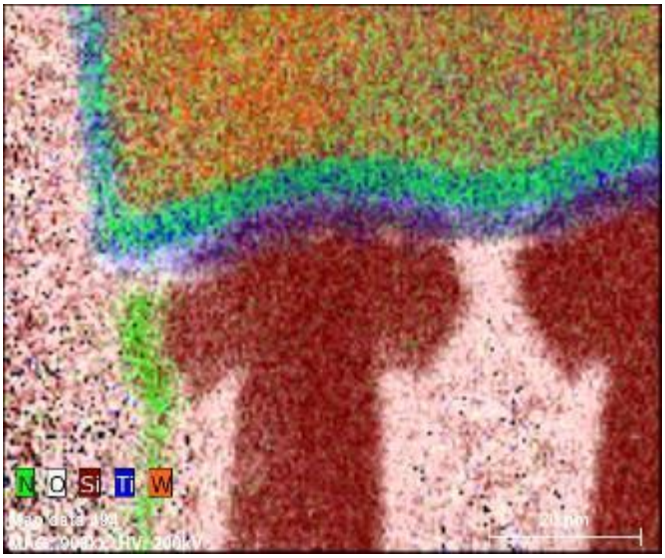

Figure 18.

67. On information and belief, each Accused Product comprises "a metal electrical contact to said source or drain." For example, each Accused Product comprises a tungsten and titanium nitride metal electrical contact. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, this tungsten and titanium nitride metal contact can be seen in orange, green, and blue:

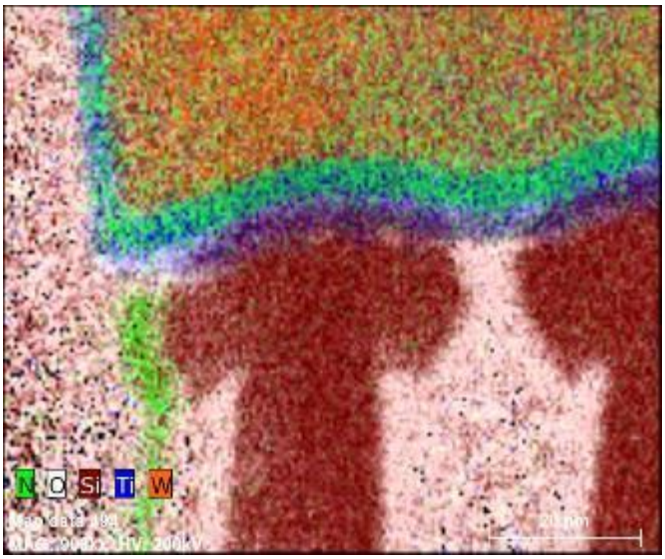

Figure 19.

68. On information and belief, each Accused Product comprises "an interface layer disposed between and in contact with said source or drain and said metal electrical contact, said source or drain being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising an oxide of titanium and an oxide of the semiconductor." For example, each Accused Product comprises an interface layer of titanium silicon oxide and silicon oxide disposed between and in contact with the silicon semiconductor source/drain and the tungsten and titanium nitride metal electrical contact. The titanium silicon oxide and silicon oxide interface layer electrically connects the silicon semiconductor source/drain and the tungsten and titanium nitride metal electrical contact to allow for the flow of an electrical current. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, the titanium silicon oxide and silicon oxide interface layer can be seen in purple and pink (or maroon-white) between the tungsten and titanium nitride metal contact and the silicon semiconductor source/drain:

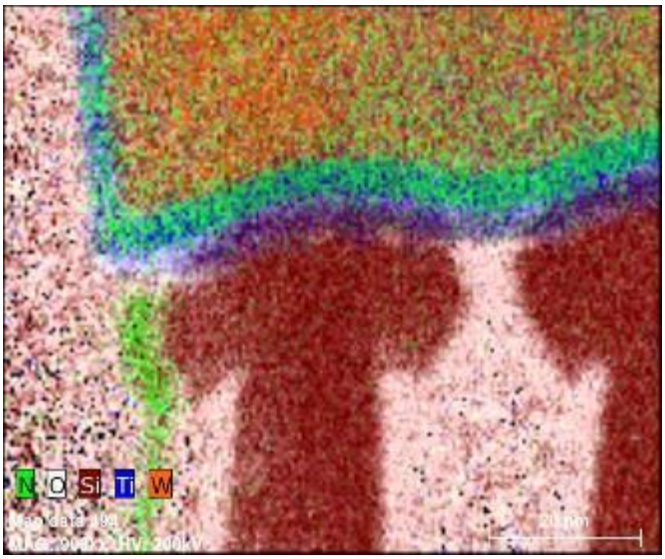

Figure 20.

69. Plaintiff has been damaged as a result of GlobalFoundries' infringing conduct described in this Count. GlobalFoundries is, thus, liable to Plaintiff in an amount that adequately compensates Plaintiff for GlobalFoundries's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT III

(Infringement Of U.S. Patent No. 10,937,880)

70. Plaintiff incorporates the preceding paragraphs herein by reference.

71. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

72. Plaintiff is the owner of all substantial rights, title, and interest in and to the '880 Patent including the right to exclude others and to enforce, sue, and recover damages for past infringements.

73. The '880 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on March 2, 2021, after full and fair examination.

74. GlobalFoundries directly infringed one or more claims of the ’880 Patent in this District and elsewhere in Delaware and the United States by making, selling, offering to sell, and/or importing the Accused Products.

75. GlobalFoundries directly infringed, either by itself or via its agent(s), at least claim 1 of the ’880 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the Accused Products.

76. By way of illustration only, each Accused Product comprises each and every element of claim 1 of the ’880 Patent. On information and belief, each Accused Product comprises “an interface layer disposed between a contact metal and a source or drain of a transistor.” For example, each Accused Products comprises an interface layer of titanium silicon oxide and silicon oxide disposed between a tungsten and titanium nitride metal electrical contact and a silicon semiconductor source or drain. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, the titanium silicon oxide and silicon oxide interface layer can be seen in purple and pink (or maroon-white) between the tungsten and titanium nitride metal electrical contact and the silicon semiconductor source/drain:

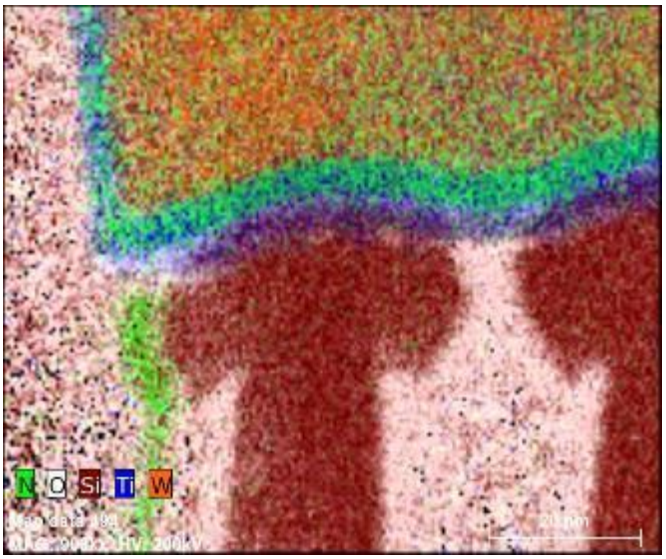

Figure 21.

77. On information and belief, each Accused Product comprises "the source or drain of the transistor comprising a silicon-based semiconductor." For example, and as detailed above, each Accused Product comprises a silicon semiconductor source or drain where the electrical current enters (source) and exits (drain). In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, the silicon semiconductor source/drain can be seen in maroon:

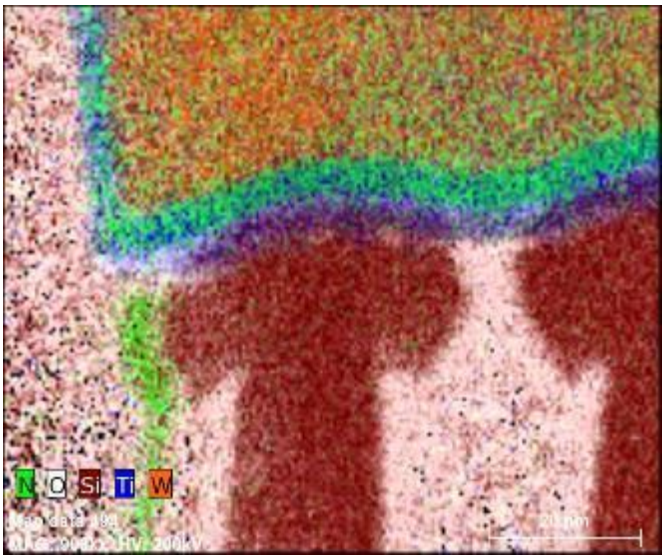

Figure 22.

78. On information and belief, each Accused Product comprises the interface layer that itself comprises "a spacer layer that is an oxide of titanium and a semiconductor oxide passivation layer." For example, and as detailed above, each Accused Product comprises an interface layer of titanium silicon oxide (the spacer layer) and silicon oxide (the passivation layer). In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, the titanium silicon oxide and silicon oxide interface layer can be seen in purple and pink (or maroon-white) between the tungsten and titanium nitride metal electrical contact and the silicon semiconductor source/drain:

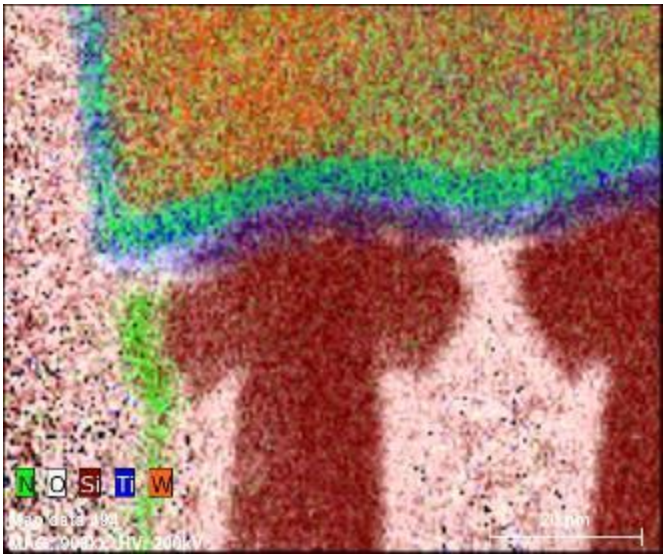

Figure 23.

79. On information and belief, each Accused Product comprises a semiconductor oxide passivation layer that "has a thickness of less than about 1 nm." For example, and as detailed above, each Accused Product comprises an interface layer of, in part, a silicon oxide passivation layer. The silicon oxide passivation layer is less than about one (1) nanometer. In the microscopic image below of a chip from the AMD Ryzen 5 1600 AF, the silicon oxide passivation layer can be seen in pink (or maroon-white) between the tungsten and titanium nitride metal electrical contact and the silicon semiconductor source/drain:

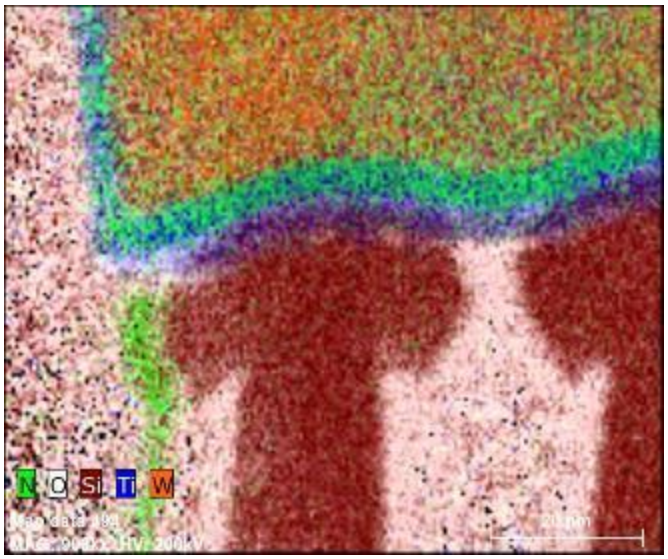

Figure 24.

80. Plaintiff has been damaged as a result of GlobalFoundries' infringing conduct described in this Count. GlobalFoundries is, thus, liable to Plaintiff in an amount that adequately compensates Plaintiff for GlobalFoundries's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

CONCLUSION

81. Plaintiff is entitled to recover from GlobalFoundries the damages sustained by Plaintiff as a result of GlobalFoundries' wrongful acts in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

82. Plaintiff has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute may give rise to an exceptional case within the meaning of 35 U.S.C. § 285, and Plaintiff is entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

JURY DEMAND

83. Plaintiff hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

PRAYER FOR RELIEF

84. Plaintiff respectfully requests that the Court find in its favor and against GlobalFoundries, and that the Court grant Plaintiff the following relief:

(i) A judgment that one or more claims of the Asserted Patents have been infringed, either literally and/or under the doctrine of equivalents, by GlobalFoundries;

(ii) A judgment that GlobalFoundries account for and pay to Plaintiff all damages and costs incurred by Plaintiff because of GlobalFoundries' infringing activities and other conduct complained of herein, including an accounting for any sales or damages not presented at trial;

(iii) A judgment that GlobalFoundries account for and pay to Plaintiff a reasonable, ongoing, post judgment royalty because of GlobalFoundries' infringing activities, and other conduct complained of herein;

(iv) A judgment that Plaintiff be granted pre-judgment and post judgment interest on the damages caused by GlobalFoundries' infringing activities and other conduct complained of herein;

(v) A judgment that this case is exceptional under the provisions of 35 U.S.C. § 285 and award enhanced damages; and

(vi) Such other and further relief as the Court deems just and equitable.

Dated: February 4, 2025

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