UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

CHIP PACKAGING TECHNOLOGIES, LLC, *Plaintiff*, v. INFINEON TECHNOLOGIES AG, *Defendant*.	Civil Action No. **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT AND DAMAGES
AND DEMAND FOR JURY TRIAL

Plaintiff Chip Packaging Technologies, LLC ("Chip Packaging" or "Plaintiff") files this Complaint for Patent Infringement and Damages against Infineon Technologies AG ("Infineon" or "Defendant") and alleges as follows:

THE PARTIES

1. Chip Packaging is the current owner and assignee of the Asserted Patents.

2. Chip Packaging is a Texas limited liability company with its principal place of business located at 5830 Granite Parkway, Suite #100-216, Plano, TX 75024.

3. Upon information and belief, Infineon is a corporation formed under the laws of the Federal Republic of Germany, with a principal place of business at Am Campeon 1-15, 85579, Neubiberg, Germany.

JURISDICTION AND VENUE

4. This civil action arises under the patent laws of the United States, 35 U.S.C. § 1 *et seq.*, including without limitation 35 U.S.C. §§ 271, 281, 283, 284, and 285. Accordingly, this Court has subject matter jurisdiction under, *inter alia*, 28 U.S.C. §§ 1331 and 1338(a).

5. This Court has personal jurisdiction over Defendant. Defendant conducts business and has committed acts of patent infringement in this Judicial District, the State of Texas, and elsewhere in the United States.

6. Plaintiff's causes of action arise, at least in part, from Defendant's contacts with and activities in this District and the State of Texas.

7. Defendant has infringed the Asserted Patents within this District and the State of Texas by making, using, distributing, marketing, offering, and/or importing in or into this District and elsewhere in the State of Texas, products that infringe the Asserted Patents, including the Accused Products. Defendant, directly and through intermediaries, makes, uses, offers, imports, distributes, advertises, promotes, and/or otherwise commercializes such infringing products in or into this District and the State of Texas. Defendant regularly conducts and solicits business in, engages in other persistent courses of conduct in, and/or derives substantial revenue from goods and services provided to residents of this District and the State of Texas.

8. This Court has personal jurisdiction over Defendants pursuant to TEX. CIV. PRAC. & REM. CODE § 17.041 *et seq*.

9. Personal jurisdiction exists over Defendant because Defendant has minimum contacts with this forum as a result of business regularly conducted within this District and the State of Texas, and, on information and belief, specifically as a result of, at least, committing the tort of patent infringement within this District and the State of Texas.

10. This Court also has personal jurisdiction over Defendant, in part, because Defendant does continuous and systematic business in this District, including by providing infringing products to the residents of this District that Defendant knew would be used within this District, and by soliciting business from the residents of this District.

11. Venue is proper in this Judicial District pursuant to 28 U.S.C. § 1391 because, among other things, Defendant is not a resident in the United States, and thus may be sued in any judicial district pursuant to 28 U.S.C. § 1391(c)(3).

THE ASSERTED PATENTS

12. On February 16, 2016, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 9,263,299 (the "'299 Patent") entitled "Exposed Die Clip Bond Power Package." A true and correct copy of the '299 Patent is attached hereto as Exhibit A.

13. CPT is the owner and assignee of all right, title, and interest in and to the '299 Patent, including the right to assert all causes of action arising under the '299 Patent and the right to sue and obtain any remedies for past, present, or future infringement.

14. On March 29, 2016, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 9,299,646 (the "'646 Patent") entitled "Lead Frame With Power And Ground Bars." A true and correct copy of the '646 Patent is attached hereto as Exhibit B.

15. Chip Packaging is the owner and assignee of all right, title, and interest in and to the '646 Patent, including the right to assert all causes of action arising under the '646 Patent and the right to sue and obtain any remedies for past, present, or future infringement.

16. On September 4, 2012, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 8,258,611 (the "'611 Patent") entitled "Leadframe Structure For Electronic Packages." A true and correct copy of the '611 Patent is attached hereto as Exhibit C.

17. Chip Packaging is the owner and assignee of all right, title, and interest in and to the ’611 Patent, including the right to assert all causes of action arising under the ’611 Patent and the right to sue and obtain any remedies for past, present, or future infringement.

18. On June 20, 2017, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 9,685,351 (the “’351 Patent”) entitled “Wire Bond Mold Lock Method And Structure.” A true and correct copy of the ’351 Patent is attached hereto as Exhibit D.

19. Chip Packaging is the owner and assignee of all right, title, and interest in and to the ’351 Patent, including the right to assert all causes of action arising under the ’351 Patent and the right to sue and obtain any remedies for past, present, or future infringement.

20. On March 12, 2013, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 8,394,713 (the “’713 Patent”) entitled “Method Of Improving Adhesion Of Bond Pad Over Pad Metallization With A Neighboring Passivation Layer By Depositing A Palladium Layer.” A true and correct copy of the ’713 Patent is attached hereto as Exhibit E.

21. Chip Packaging is the owner and assignee of all right, title, and interest in and to the ’713 Patent, including the right to assert all causes of action arising under the ’713 Patent and the right to sue and obtain any remedies for past, present, or future infringement.

22. Chip Packaging has at all times complied with the marking provisions of 35 U.S.C. § 287 with respect to the Asserted Patents.

<u>FACTUAL ALLEGATIONS</u>

23. The Asserted Patents relate to groundbreaking improvements to semiconductor packaging technologies.

24. The technology in U.S. Patent No. 9,263,299 (“the ’299 Patent”) was developed by Leonardus Antonius Elisabeth van Gemert and Emil Casey Israel of NXP B.V.

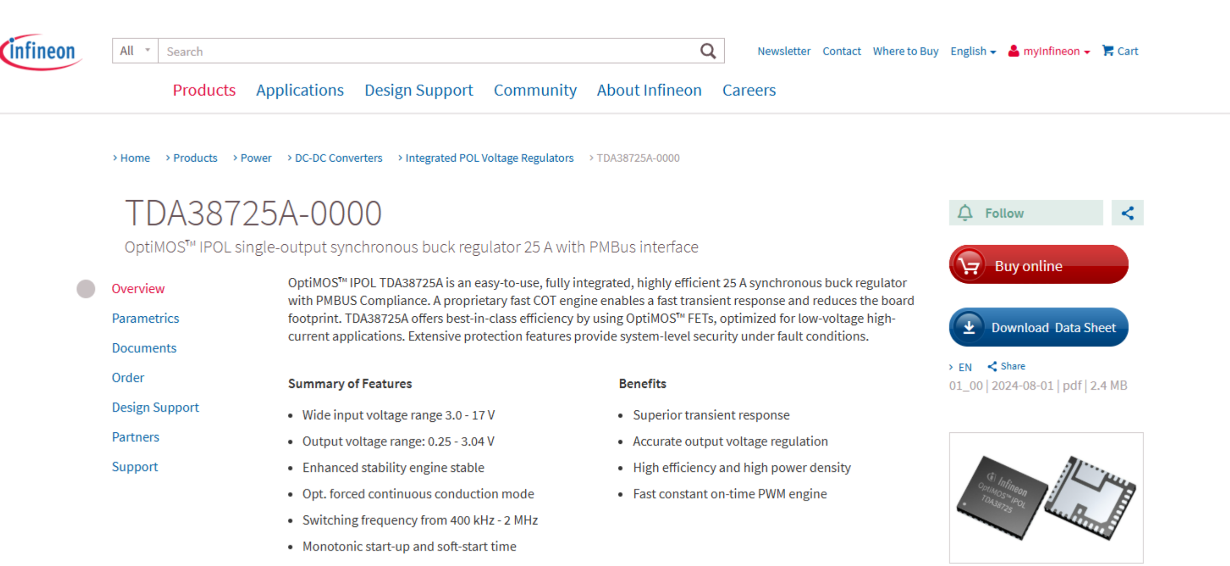
25. The technology in U.S. Patent No. 9,299,646 ("the '646 Patent") was developed by Shailesh Kumar and Piyush Kumar Mishra of Freescale Semiconductor, Inc.

26. The technology in U.S. Patent No. 8,258,611 ("the '611 Patent") was developed by Ronald Schravendeel and Peter Schelwald of NXP B.V.

27. The technology in U.S. Patent No. 9,685,351 ("the '351 Patent") was developed by Leo M. Higgins, III of NXP USA, Inc.

28. The technology in U.S. Patent No. 8,394,713 ("the '713 Patent") was developed by Varughese Mathew of Freescale Semiconductor, Inc.

29. On information and belief, each of the Infineon products identified herein, including the Infineon OPTIREG Buck Regulator product line, the Infineon PROFET Smart High-Side Power Switch product line, the Infineon CoolGaN Integrated Power Stage products, the Infineon TC1782 AUDO MAX Microcontroller, Infineon TLF51801 OPTIREG Asynchronous DC/DC Step-Down Converter, and the Infineon TLE9872 Motix 32-bit Microcontroller have been available for purchase in the United States, including but not limited to, directly from Infineon, through Infineon's website, and/or through Infineon-authorized Americas distributors. By way of example only, the Infineon Buck Regulator products are available for purchase in the United States, including but not limited to through Infineon's website through Infineon-authorized Global or Americas distributors:



TDA38725A-0000

OptiMOS™ IPOL single-output synchronous buck regulator 25 A with PMBus interface

OptiMOS™ IPOL TDA38725A is an easy-to-use, fully integrated, highly efficient 25 A synchronous buck regulator with PMBUS Compliance. A proprietary fast COT engine enables a fast transient response and reduces the board footprint. TDA38725A offers best-in-class efficiency by using OptiMOS™ FETs, optimized for low-voltage high-current applications. Extensive protection features provide system-level security under fault conditions.

Summary of Features

- Wide input voltage range 3.0 - 17 V
- Output voltage range: 0.25 - 3.04 V
- Enhanced stability engine stable
- Opt. forced continuous conduction mode
- Switching frequency from 400 kHz - 2 MHz
- Monotonic start-up and soft-start time
- Thermally compensated internal OCP
- PMBus system interface for reporting
- Multiple time programming (MTP)
- Digitally programmable load-line
- Thermal shut down
- Operating temp: -40°C < Tj < 125°C

Benefits

- Superior transient response
- Accurate output voltage regulation
- High efficiency and high power density
- Fast constant on-time PWM engine

Potential Applications

- DC-DC power conversion for telecom infrastructure
- Base stations
- FPGA power
- Storage

We offer the following online ordering options

TDA38725A0000AUMA1

Products > Power > DC-DC Converters > Integrated POL Voltage Regulators > TDA38725A-0000

	Stock*	Price per unit	Quantity
Infineon	1137	$ 4.95	1
Standard Global Shipping		$ 4.99	

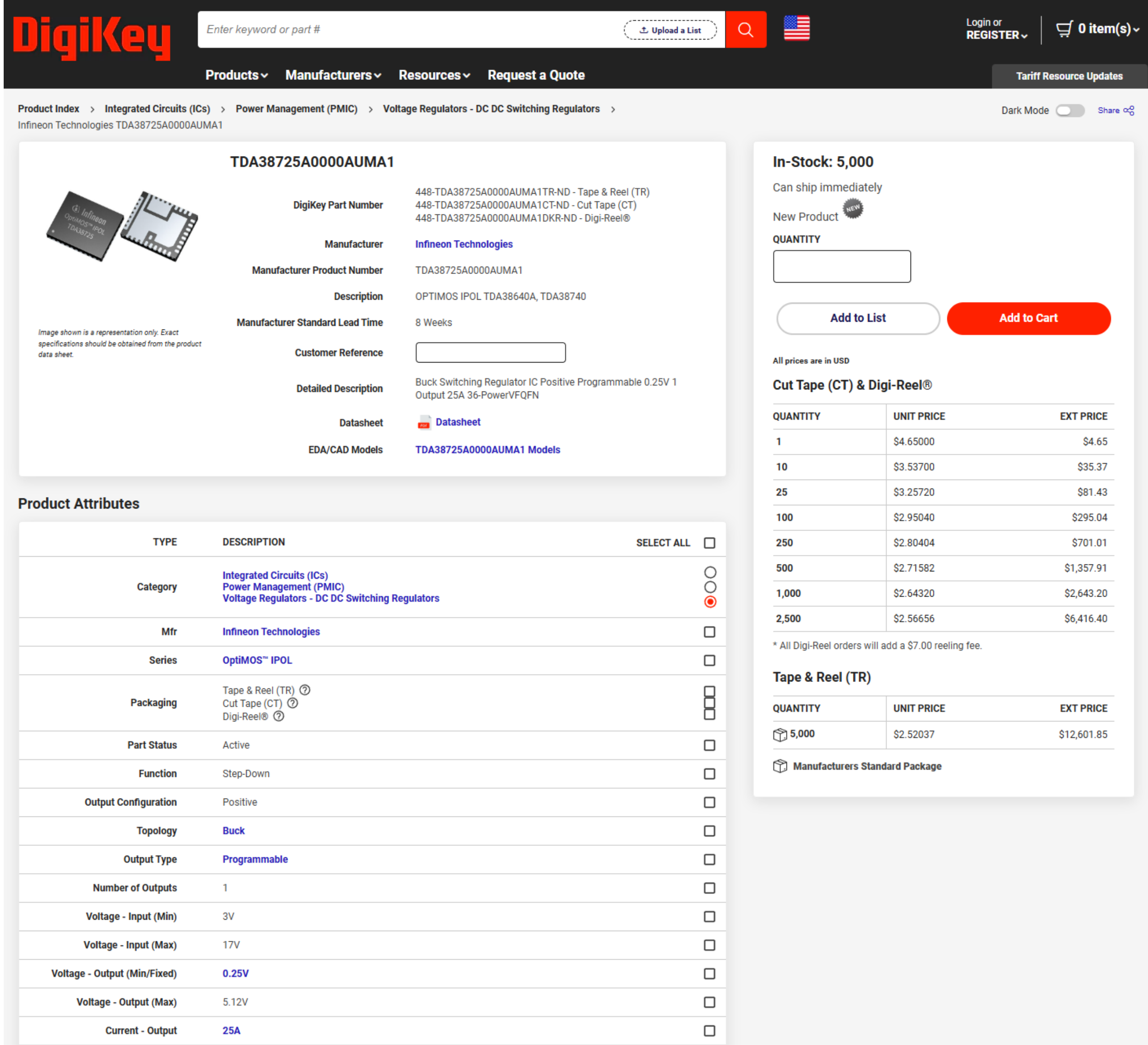
Add to cart

AMERICAS (in stock) EMEA (in stock) ASIA (in stock) JAPAN (in stock)

Distributor	Stock*	
DigiKey	5000	› Order now
MOUSER ELECTRONICS	2274	› Order now
ARROW	100	› Order now
AVNET	0	› Order now
FUTURE ELECTRONICS	0	› Order now
Newark	0	› Order now

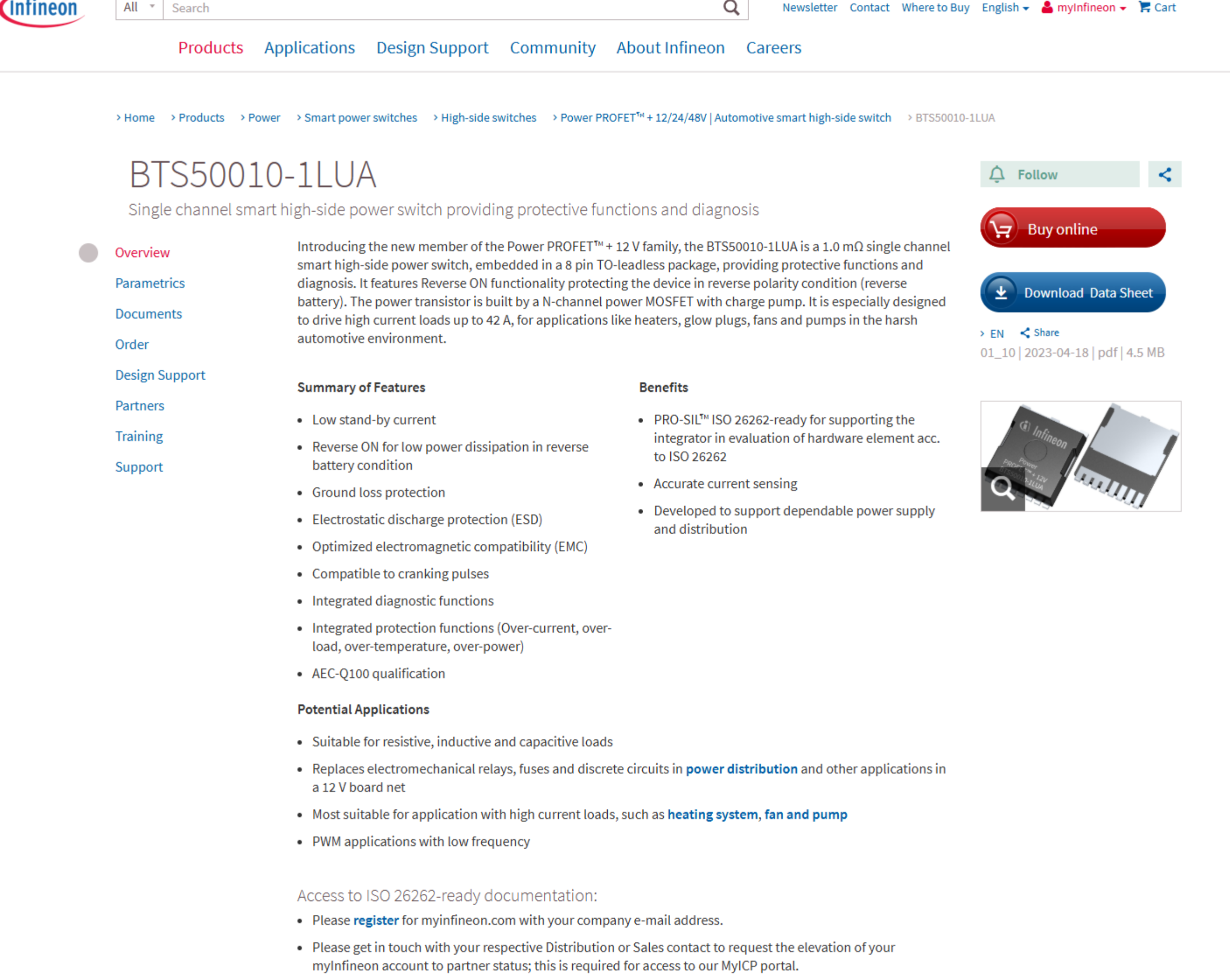
*stock values are subject to change

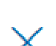
See https://www.infineon.com/cms/en/product/power/dc-dc-converters/integrated-pol-voltage-regulators/tda38725a-0000/ (last visited 1/27/2025).



See https://www.digikey.com/en/products/detail/infineon-technologies/TDA38725A0000AUMA1/25595596?curr=usd&utm_campaign=buynow&utm_medium=aggregator&utm_source=octopart (last visited 1/27/2025).

30. As another example, the Infineon Smart High-Side Power Switch product line are available for purchase in the United States, including but not limited to through Infineon's website through Infineon-authorized Global or Americas distributors:





We offer the following online ordering options

BTS500101LUAAUMA1

Products > Power > Smart power switches > High-side switches > Power PROFET™ + 12/24/48V | Automotive smart high-side switch > BTS50010-1LUA

	Stock*	Price per unit	Quantity
Infineon	1044	$ 4.96	1
Standard Global Shipping		$ 4.99	

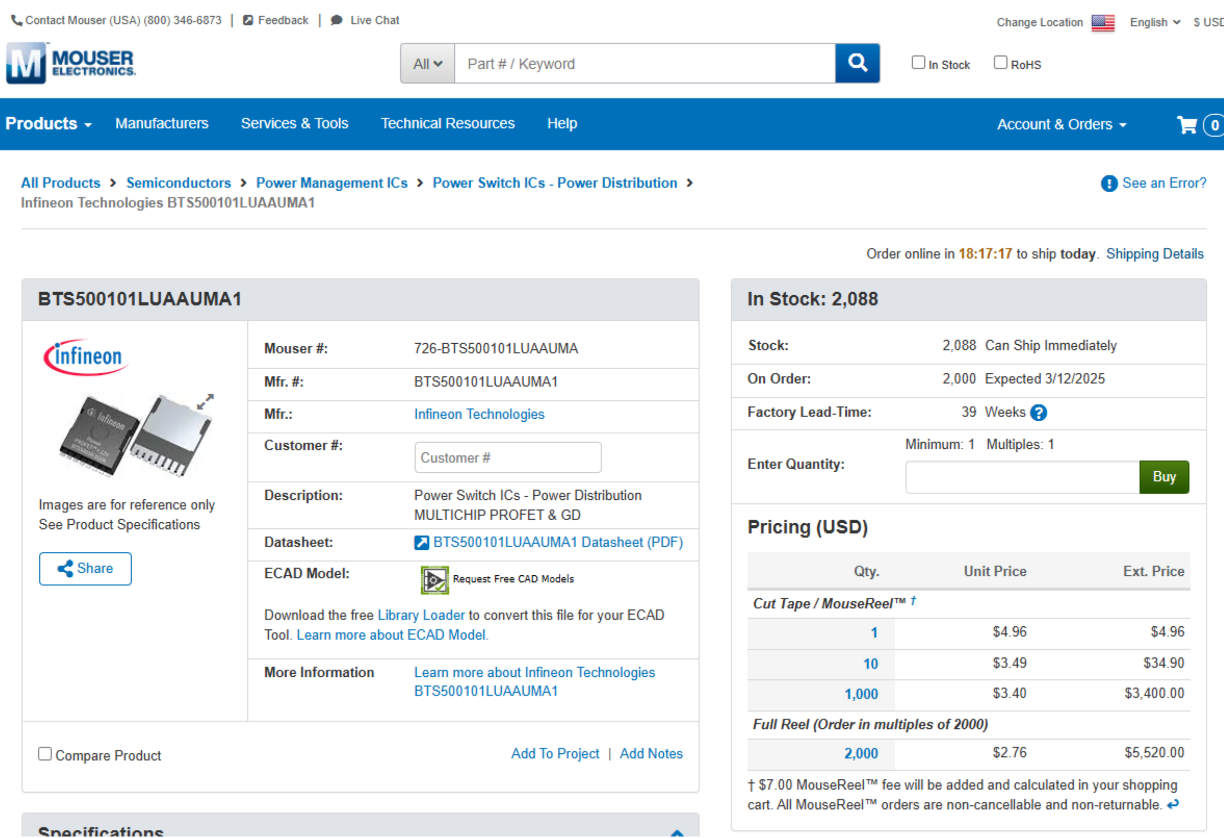
Add to cart

AMERICAS (in stock) EMEA (in stock) ASIA (in stock) JAPAN (in stock)

Distributor	Stock*	
Rochester Electronics **	3739	› Order now
Mouser Electronics	2088	› Order now
DigiKey	0	› Order now
Arrow	0	› Order now
AVNET	0	› Order now
Newark	0	› Order now
RS	0	› Order now

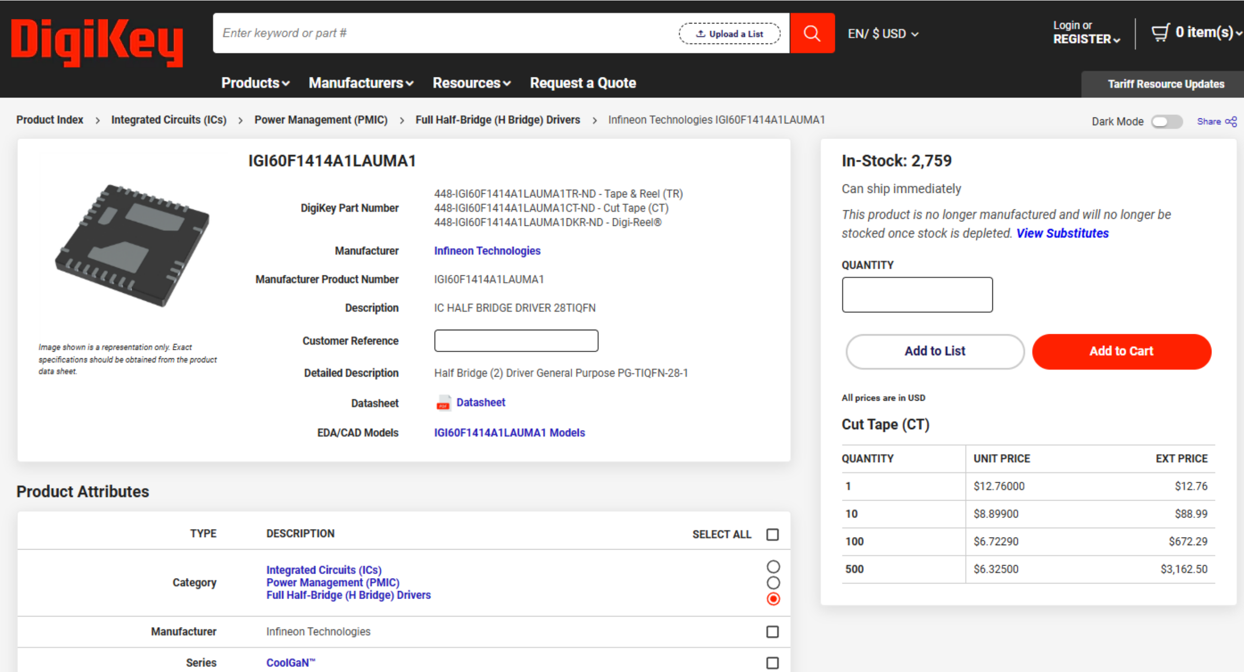
*stock values are subject to change
**Authorized resellers for overstock, and discontinued products which are warranted for reliability by the reseller, no longer by Infineon

See https://www.infineon.com/cms/en/product/power/smart-power-switches/high-side-switches/power-profet-plus-12v-automotive-smart-high-side-switch/bts50010-1lua/ (last visited 1/27/2025).



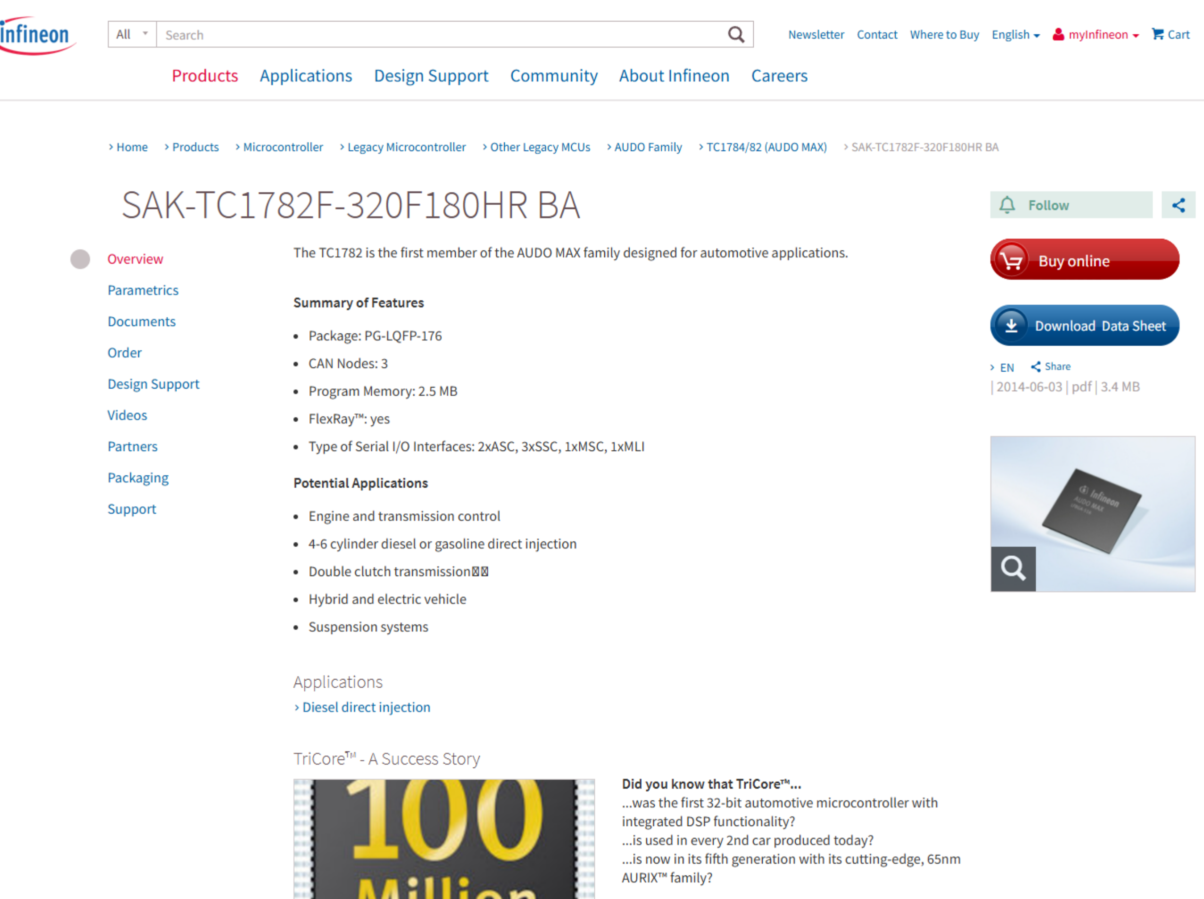
See https://www.mouser.com/ProductDetail/Infineon-Technologies/BTS500101LUAAUMA1?qs=8Wlm6%252BaMh8RV1CWLPmP8Ug%3D%3D&utm_source=octopart&utm_medium=aggregator&utm_campaign=726-BTS500101LUAAUMA&utm_content=Infineon (last visited 1/27/2025).

31. As another example, the Infineon CoolGaN Integrated Power Stage are available for purchase in the United States, including but not limited to through Infineon-authorized Global or Americas distributors:



See https://www.digikey.com/en/products/detail/infineon-technologies/IGI60F1414A1LAUMA1/15776244 (last visited 1/27/2025).

32. As another example, the Infineon 32-bit MCU TriCore Package product line are available for purchase in the United States, including but not limited to through Infineon's website through Infineon-authorized Global or Americas distributors:


infineon
All
Search
Newsletter
Contact
Where to Buy
English
myInfineon
Cart
Products
Applications
Design Support
Community
About Infineon
Careers
› Home › Products › Microcontroller › Legacy Microcontroller › Other Legacy MCUs › AUDO Family › TC1784/82 (AUDO MAX) › SAK-TC1782F-320F180HR BA
SAK-TC1782F-320F180HR BA
Follow
Overview
Parametrics
Documents
Order
Design Support
Videos
Partners
Packaging
Support
The TC1782 is the first member of the AUDO MAX family designed for automotive applications.
Summary of Features
Package: PG-LQFP-176
CAN Nodes: 3
Program Memory: 2.5 MB
FlexRay™: yes
Type of Serial I/O Interfaces: 2xASC, 3xSSC, 1xMSC, 1xMLI
Potential Applications
Engine and transmission control
4-6 cylinder diesel or gasoline direct injection
Double clutch transmission
Hybrid and electric vehicle
Suspension systems
Applications
› Diesel direct injection
TriCore™ - A Success Story
100
Million
Did you know that TriCore™...
...was the first 32-bit automotive microcontroller with integrated DSP functionality?
...is used in every 2nd car produced today?
...is now in its fifth generation with its cutting-edge, 65nm AURIX™ family?
Buy online
Download Data Sheet
› EN
Share
| 2014-06-03 | pdf | 3.4 MB

We offer the following online ordering options

TC1782F320F180HRBAKXUMA2

Products > Microcontroller > Legacy Microcontroller > Other Legacy MCUs > AUDO Family > TC1784/82 (AUDO MAX) > SAK-TC1782F-320F180HR BA

	Stock*	Price per unit	Quantity
infineon Infineon	987	$ 23.98	1
Standard Global Shipping		$ 4.99	

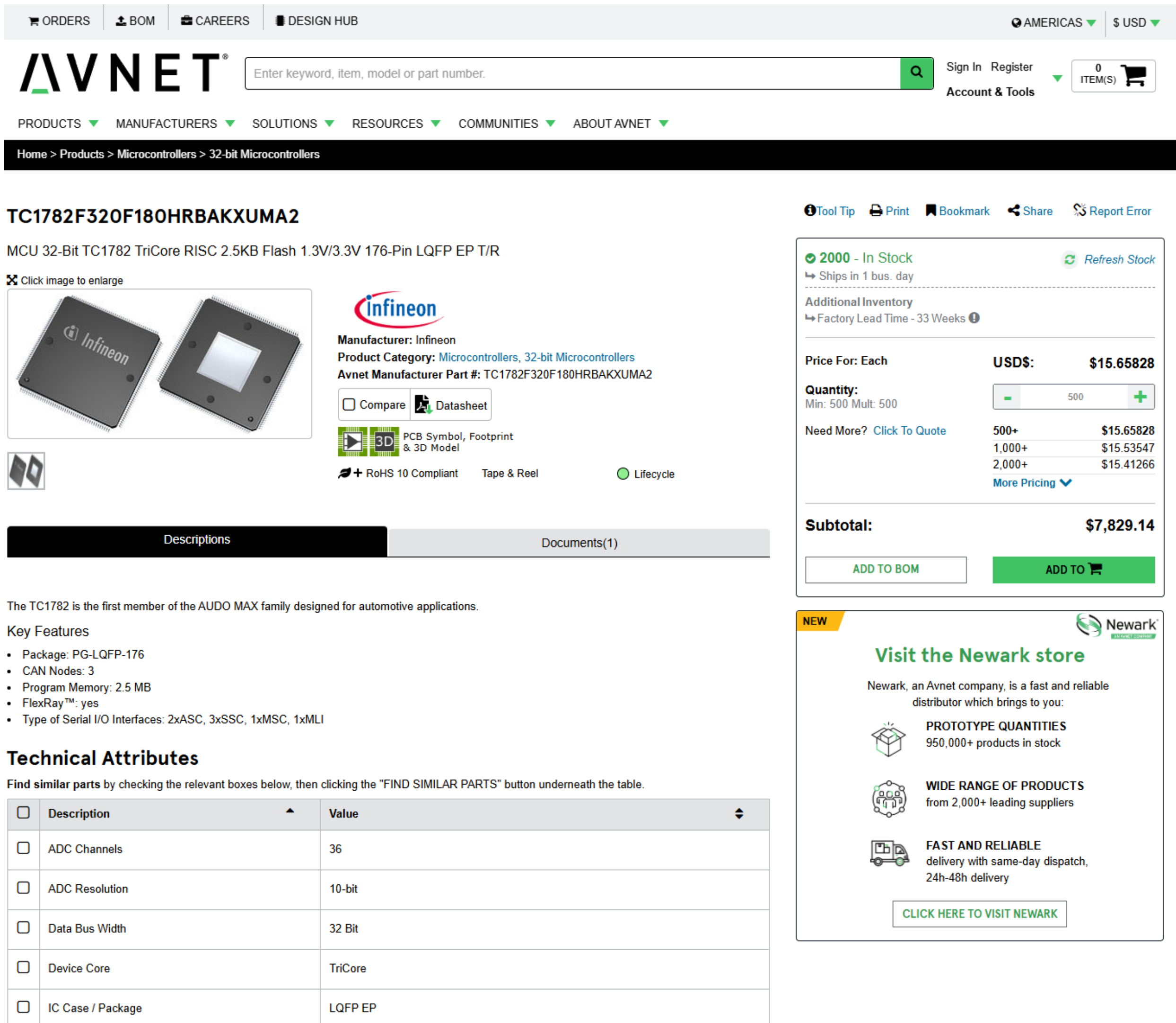
Add to cart

AMERICAS (in stock) EMEA (in stock) ASIA (in stock) JAPAN (in stock)

Distributor	Stock*	
AVNET	2000	› Order now
MOUSER ELECTRONICS	1975	› Order now
RS	1500	› Order now
Newark	729	› Order now
Rochester Electronics **	96	› Order now
DigiKey	0	› Order now
ARROW	0	› Order now

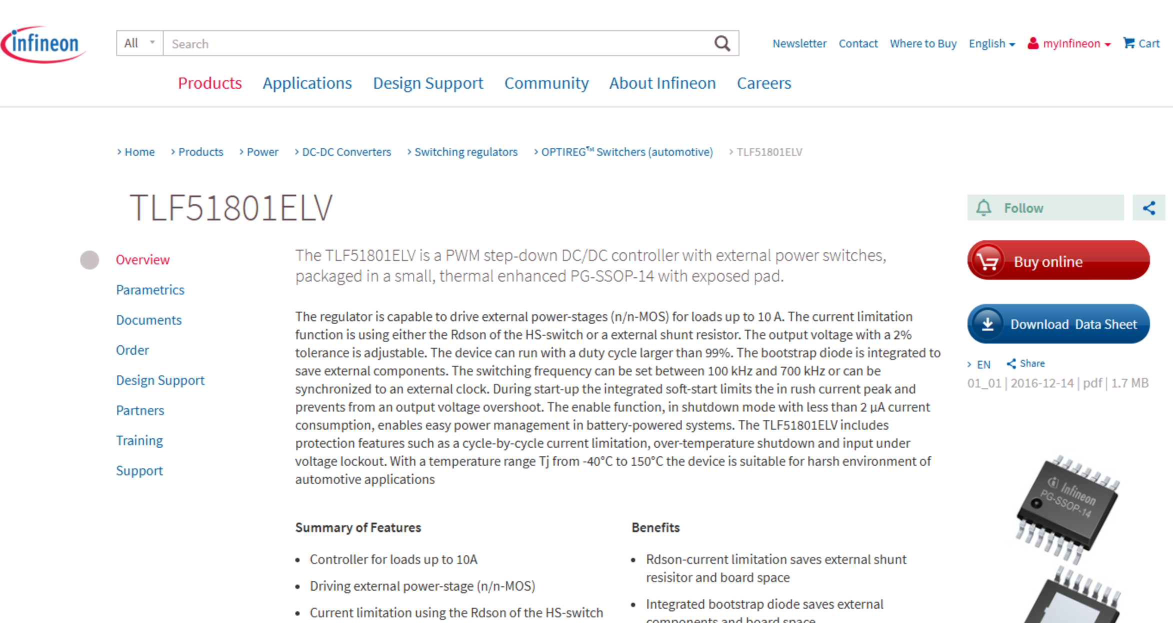
*stock values are subject to change
**Authorized resellers for overstock, and discontinued products which are warranted for reliability by the reseller, no longer by Infineon

See https://www.infineon.com/cms/en/product/microcontroller/legacy-microcontroller/other-legacy-mcus/audo-family/tc1784-82-audo-max/sak-tc1782f-320f180hr-ba/ (last visited 1/27/2025).



See https://www.avnet.com/shop/us/products/infineon/tc1782f320f180hrbakxuma2-3074457345624887968?CMP=EMA_Octopart_inventoryfeed_VSE (last visited 1/27/2025).

33. As another example, the Infineon TLF51801 Asynchronous DC/DC Step-Down Converter product line are available for purchase in the United States, including but not limited to through Infineon's website through Infineon-authorized Global or Americas distributors:



Infineon

All | Search

Newsletter Contact Where to Buy English myInfineon Cart

Products Applications Design Support Community About Infineon Careers

› Home › Products › Power › DC-DC Converters › Switching regulators › OPTIREG™ Switchers (automotive) › TLF51801ELV

TLF51801ELV

Follow

Overview
Parametrics
Documents
Order
Design Support
Partners
Training
Support

The TLF51801ELV is a PWM step-down DC/DC controller with external power switches, packaged in a small, thermal enhanced PG-SSOP-14 with exposed pad.

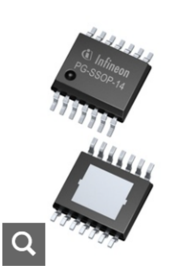
The regulator is capable to drive external power-stages (n/n-MOS) for loads up to 10 A. The current limitation function is using either the Rdson of the HS-switch or a external shunt resistor. The output voltage with a 2% tolerance is adjustable. The device can run with a duty cycle larger than 99%. The bootstrap diode is integrated to save external components. The switching frequency can be set between 100 kHz and 700 kHz or can be synchronized to an external clock. During start-up the integrated soft-start limits the in rush current peak and prevents from an output voltage overshoot. The enable function, in shutdown mode with less than 2 µA current consumption, enables easy power management in battery-powered systems. The TLF51801ELV includes protection features such as a cycle-by-cycle current limitation, over-temperature shutdown and input under voltage lockout. With a temperature range Tj from -40°C to 150°C the device is suitable for harsh environment of automotive applications

Buy online

Download Data Sheet

› EN Share

01_01 | 2016-12-14 | pdf | 1.7 MB



Summary of Features

- Controller for loads up to 10A
- Driving external power-stage (n/n-MOS)
- Current limitation using the Rdson of the HS-switch or via shunt-resistor
- Adjustable output voltage: 1.2V up to Dmax*Vs
- ± 2% output voltage tolerance
- Duty cycle > 99%
- Integrated bootstrap diode
- Input voltage range from 4.75V to 45V
- Adjustable switching frequency: 100 kHz up to 700 kHz
- Syncronization input
- EN for ultra-low shut-down current (< 2 µA)
- Integrated soft-start function
- Suited for automotive applications: Tj = -40 °C to +150 °C
- Green Product (RoHS compliant)
- AEC Qualified

Benefits

- Rdson-current limitation saves external shunt resisitor and board space
- Integrated bootstrap diode saves external components and board space
- High duty cycle allows low drop-out operation
- Integrated soft- start function saves external components and board space

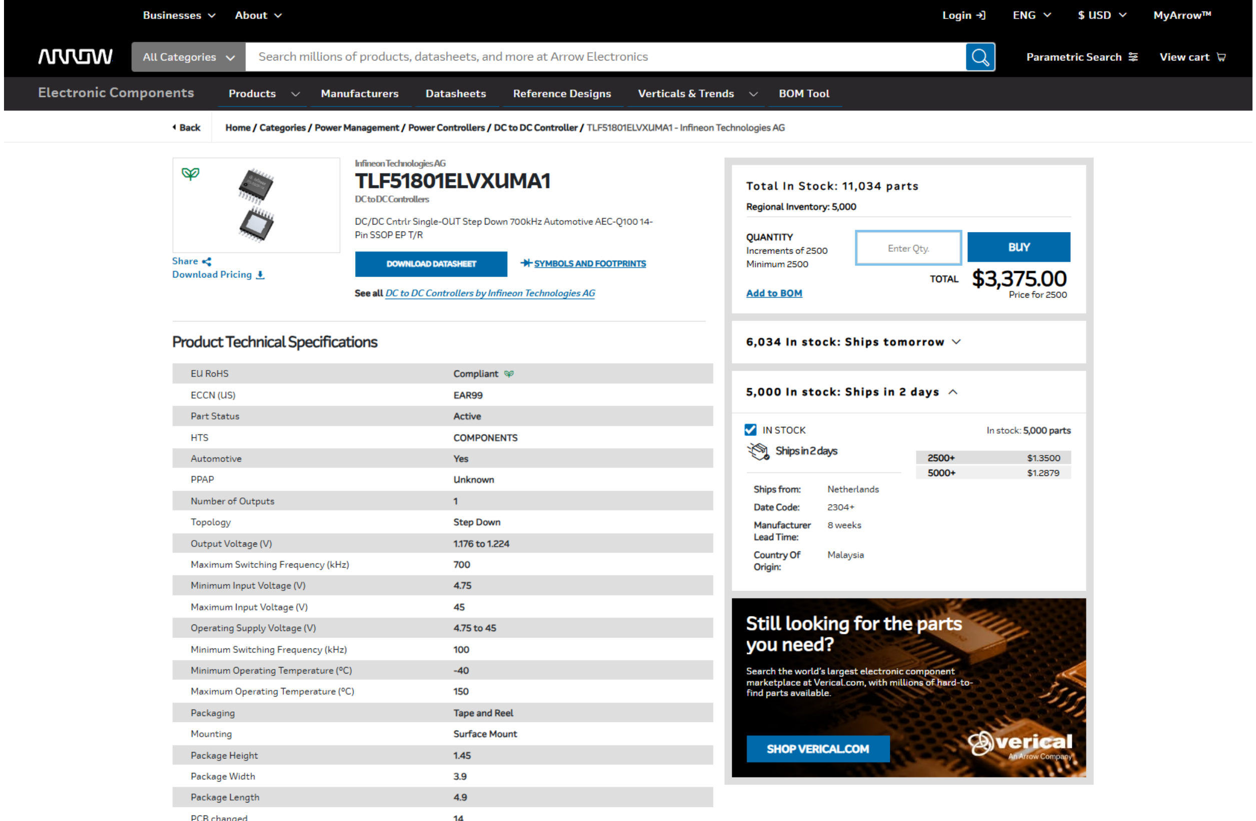
We offer the following online ordering options

AMERICAS (in stock) **EMEA** (in stock) **ASIA** (in stock) **JAPAN** (in stock)

Distributor	Stock*	
RS	9945	› Order now
DigiKey	6011	› Order now
MOUSER ELECTRONICS	5045	› Order now
ARROW	5000	› Order now
Rochester Electronics **	2357	› Order now
Newark	1740	› Order now
FUTURE ELECTRONICS	0	› Order now
AVNET	0	› Order now

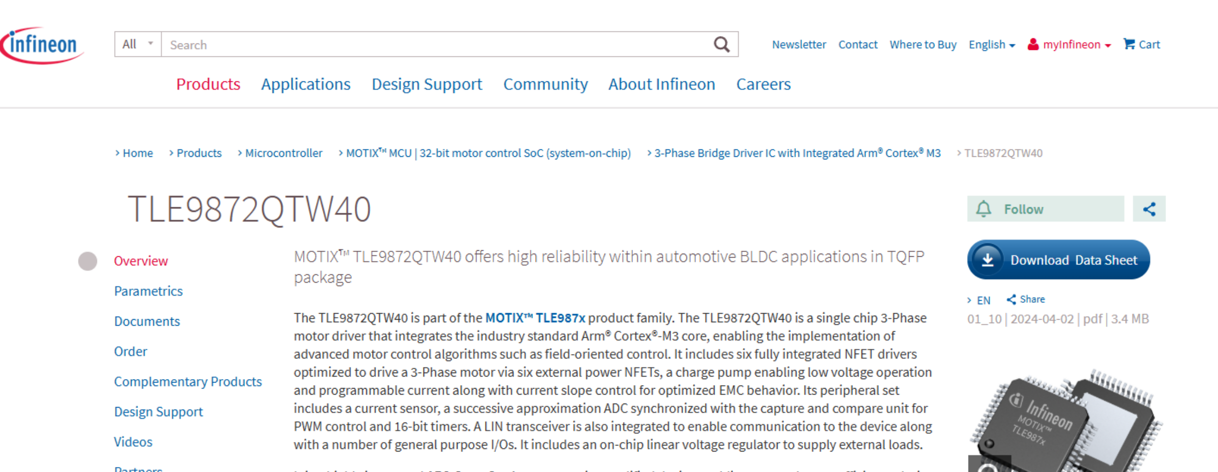
*stock values are subject to change
**Authorized resellers for overstock, and discontinued products which are warranted for reliability by the reseller, no longer by Infineon

See https://www.infineon.com/cms/en/product/power/dc-dc-converters/switching-regulators/optireg-switchers-automotive/tlf51801elv/ (last visited 1/27/2025).



See https://www.arrow.com/en/products/tlf51801elvxuma1/infineon-technologies-ag?region=europe&utm_campaign=octopart_2022&utm_content=inv_listing&utm_currency=USD&utm_keyword=TLF51801ELVXUMA1&utm_medium=aggregator&utm_source=octopart (last visited 1/27/2025).

34. As another example, the Infineon TLE9872 Microcontroller product line are available for purchase in the United States, including but not limited to through Infineon's website through Infineon-authorized Global or Americas distributors:



TLE9872QTW40

- Overview
- Parametrics
- Documents
- Order
- Complementary Products
- Design Support
- Videos
- Partners
- Training
- Support

MOTIX™ TLE9872QTW40 offers high reliability within automotive BLDC applications in TQFP package

The TLE9872QTW40 is part of the **MOTIX™ TLE987x** product family. The TLE9872QTW40 is a single chip 3-Phase motor driver that integrates the industry standard Arm® Cortex®-M3 core, enabling the implementation of advanced motor control algorithms such as field-oriented control. It includes six fully integrated NFET drivers optimized to drive a 3-Phase motor via six external power NFETs, a charge pump enabling low voltage operation and programmable current along with current slope control for optimized EMC behavior. Its peripheral set includes a current sensor, a successive approximation ADC synchronized with the capture and compare unit for PWM control and 16-bit timers. A LIN transceiver is also integrated to enable communication to the device along with a number of general purpose I/Os. It includes an on-chip linear voltage regulator to supply external loads.

It is a highly integrated **AEC-Q100 Grade 0** automotive qualified device enabling cost and space efficient solutions for BLDC motor drive applications.

Buy online

Summary of Features:

- Six current programmable Drivers with charge pump for N-Channel MOSFET
- Integrated LIN transceiver compatible with LIN 2.2 and SAEJ2602
- Two Full duplex serial interface (UART) with LIN support
- Two Synchronous serial channel (SSC)
- On-chip OSC and PLL for clock generation
- One high voltage monitoring input with wake up functionality
- High speed operational amplifier for motor current sensing via shunt
- Measurement unit:
  - 8-bit ADC module with 10 multiplexed inputs
  - 10-bit ADC module with 8 multiplexed inputs, 5 external Analog inputs
  - On chip temperature and battery voltage measurement unit
- Increased Temperature Shutdown supports operation up to Tjmax = 175 °C
- Independent Programmable window watchdog
- 5V/1.5V Internal supplies

Features of the Microcontroller:

- 32 bit Arm® Cortex®-M3 Core, up to 40 MHz clock frequency
- 256 kByte flash memory for code and data
- 32 kByte Boot ROM memory in code space (used for boot code and IP storage)
- 8 kByte RAM memory
- Harvard architecture
- Thumb®-2 Instruction Set and hardware divide and multiplication unit
- Four 16-Bit timers
- Capture/compare unit for PWM signal generation (CCU6) with 2 x 16-bits timers

General Characteristics:

- Operating supply voltage Vs=5.5 to 27V, maximum rating 40V
- Extended operating range Vs=3.0 to 28V, MCU / Flash fully functional
- ESD performance :
  - up to 2kV / handling on all pins
  - 4kV @ HV inputs
  - 6kV @ LIN pin

We offer the following online ordering options

TLE9872QTW40XUMA1

Products > Microcontroller > MOTIX™ MCU | 32-bit motor control SoC (system-on-chip) > 3-Phase Bridge Driver IC with Integrated Arm® Cortex® M3 > TLE9872QTW40

	Stock*	Price per unit	Quantity
Infineon	1207	$ 7.09	1
Standard Global Shipping		$ 4.99	

Add to cart

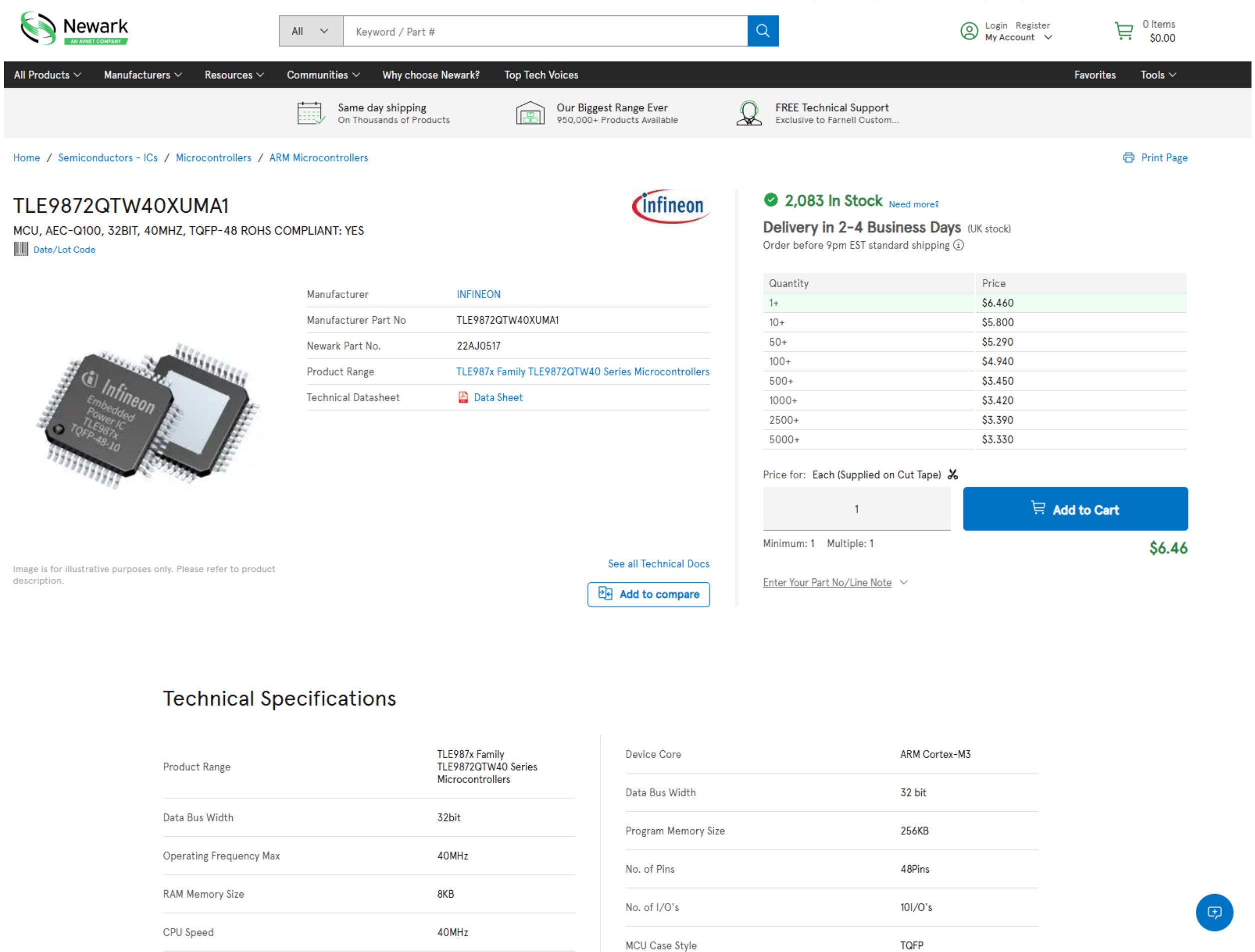
AMERICAS (in stock) EMEA (in stock) ASIA (in stock) JAPAN (in stock)

Distributor	Stock*	
DigiKey	2604	› Order now
Mouser Electronics	2415	› Order now
Newark	2083	› Order now
Rochester Electronics **	2072	› Order now
Arrow	0	› Order now
Future Electronics	0	› Order now
Avnet	0	› Order now

*stock values are subject to change

**Authorized resellers for overstock, and discontinued products which are warranted for reliability by the reseller, no longer by Infineon

See https://www.infineon.com/cms/en/product/microcontroller/embedded-power-ics-system-on-chip-/3-phase-bridge-driver-integrated-arm-cortex-m3/tle9872qtw40/ (last visited 1/27/2025).



See https://www.newark.com/infineon/tle9872qtw40xuma1/mcu-aec-q100-32bit-40mhz-tqfp/dp/22AJ0517?CMP=AFC-OP (last visited 1/27/2025).

FIRST COUNT
(Infringement of U.S. Patent No. 9,263,299)

35. Chip Packaging incorporates by reference the allegations set forth in Paragraphs 1-34 of the Complaint as though fully set forth herein.

36. The claims of the ’299 Patent are valid and enforceable.

37. Infineon has and continues to directly infringe the ’299 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products made using the patented methods including, but not limited to, products that satisfy each and every limitation of one or more claims of the ’299 Patent. Upon information and belief, such products include at least the Infineon OPTIREG Buck Regulator product line, including but not limited to: TDA38725. On information and belief, this further includes the Infineon Smart High-Side Power Switch product line including but not limited to the BTS50005-1LUA.

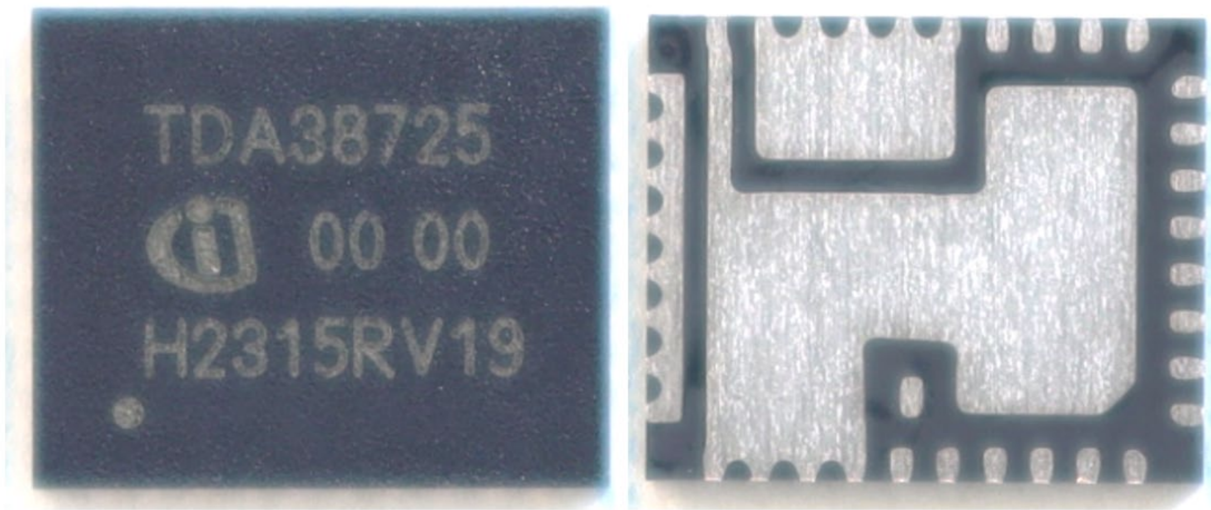
38. For example, the Accused Products incorporates and/or implements elements that are identical or equivalent to each claimed element of the patented invention pointed out by at least Claim 1 of the ’299 Patent.

39. Claim 1 of the ’299 Patent recites:

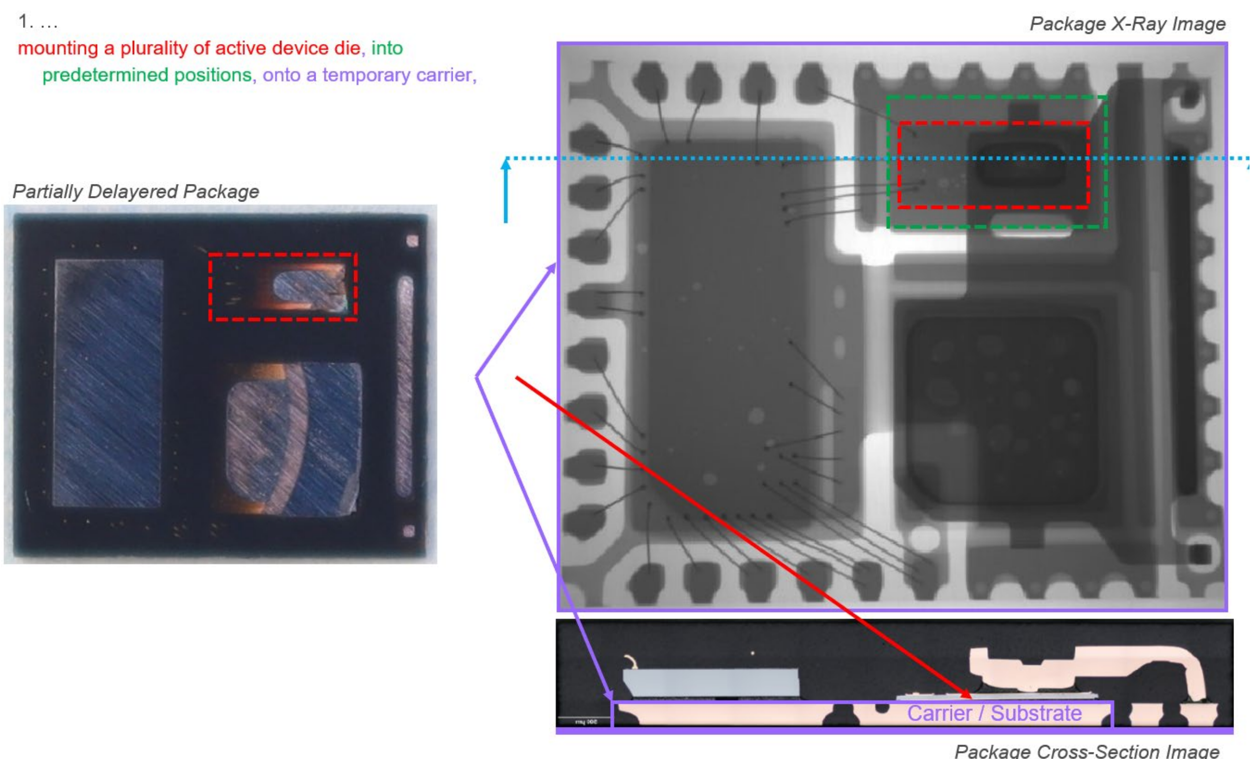
> 1. A method for packaging an integrated circuit (IC) device, the method comprising:
>
> > mounting a plurality of active device die, into predetermined positions, onto a temporary carrier, each said active device die having bond pads, each of said active device die having a solderable conductive surface on its underside; and having been subjected to back-grinding to a prescribed thickness;
> >
> > dispensing a solder paste onto the bond pads on the plurality active device die;
> >
> > attaching a lead frame to the temporary carrier, the lead frame having an array of device positions which correspond to the predetermined positions of the plurality of active device die, wherein upper lead frame portions contact the solder paste present on the bond pads and lower lead frame portions contact the temporary carrier; and
> >
> > reflowing the solder so that a connection is made between the upper lead frame portions and the bond pads of the plurality of active device die.

’299 Patent, Cl. 1.

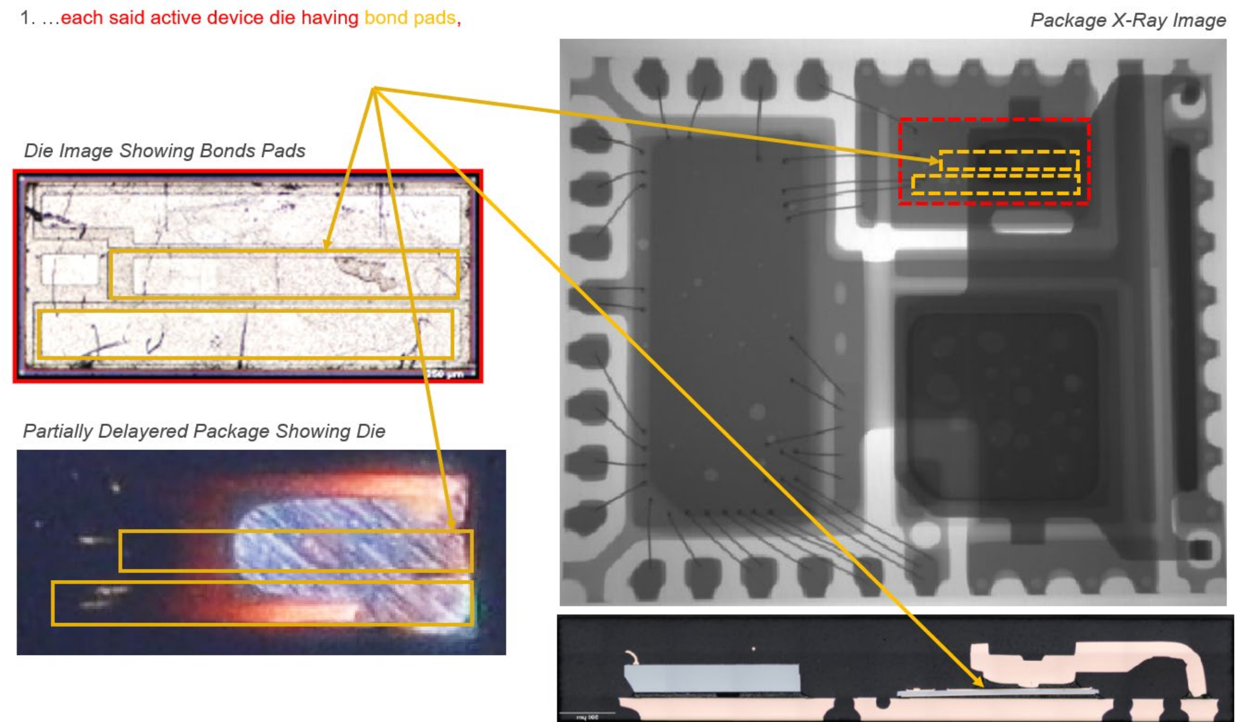
40. For example, the Infineon Buck Regulator implements a method for packaging an integrated circuit (IC) device. The integrated circuit (IC) device of the Infineon Buck Regulator is illustrated below:



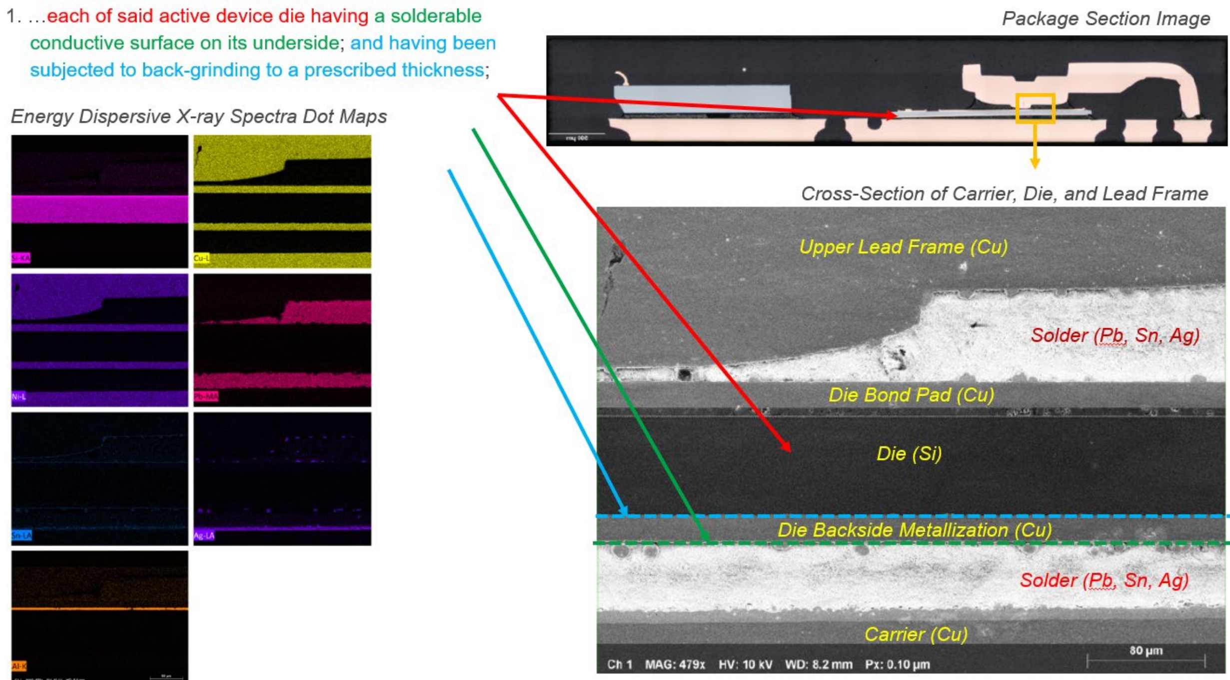
41. On information and belief, the Accused Products are manufactured using a process that mounts a plurality of active device die, into predetermined positions, onto a temporary carrier.



42. On information and belief, within the Accused Products each active die has bond pads.

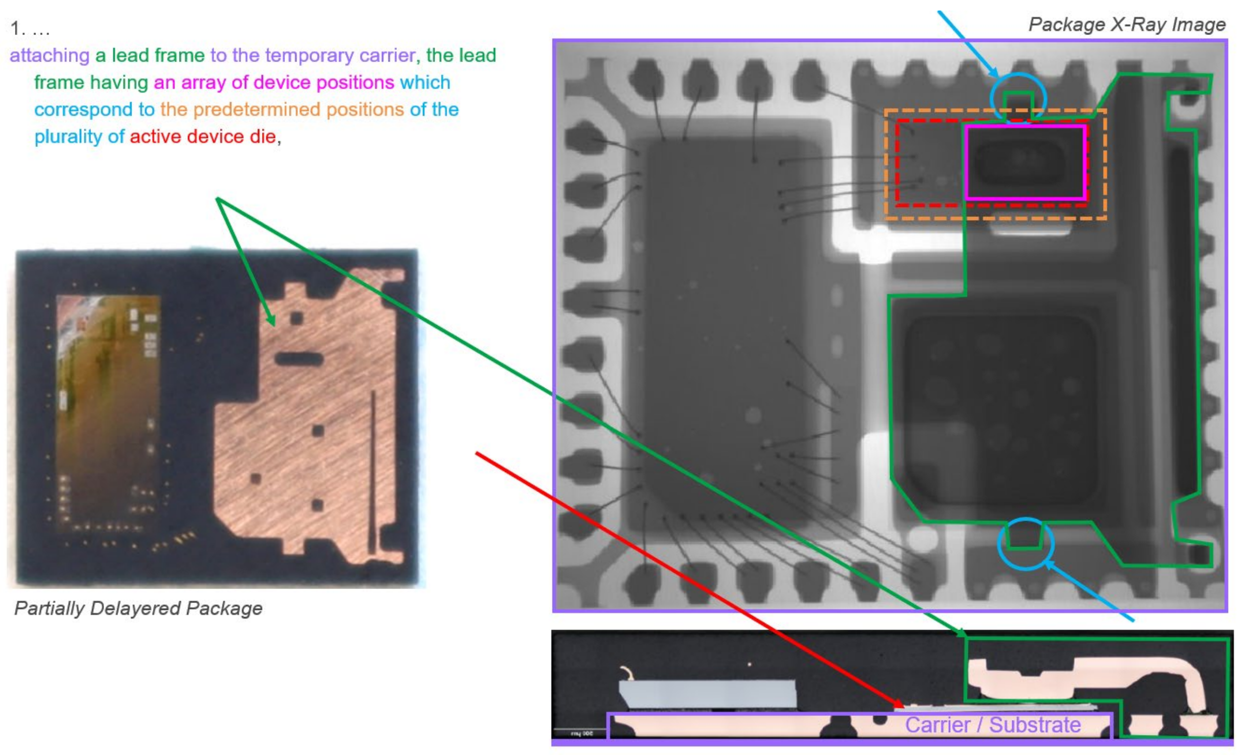


43. On information and belief, within the Accused Products each active die has a solderable conductive surface on its underside; and has been subjected to back-grinding to a prescribed thickness.



44. On information and belief, the Accused Products are manufactured using a process that dispenses a solder paste onto the bond pads on the plurality active device die.

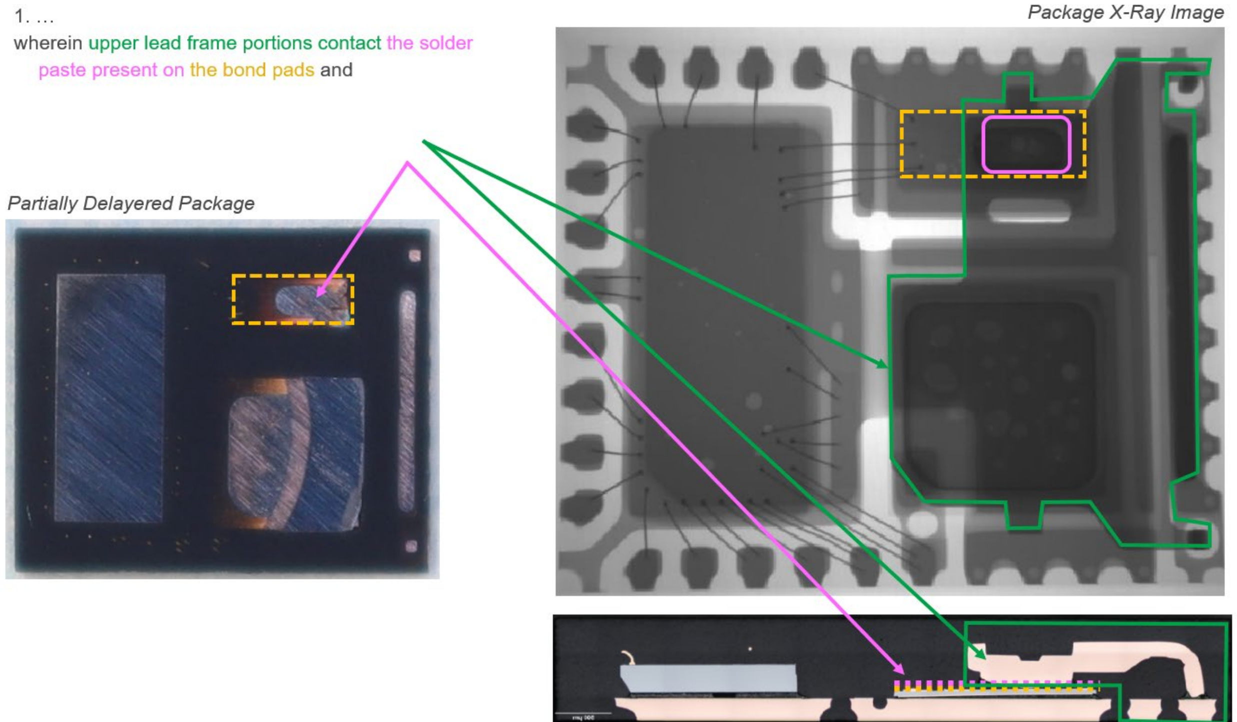
45. On information and belief, the Accused Products are manufactured using a process that attaches a lead frame to the temporary carrier, the lead frame having an array of device positions which correspond to the predetermined positions of the plurality of active device die.



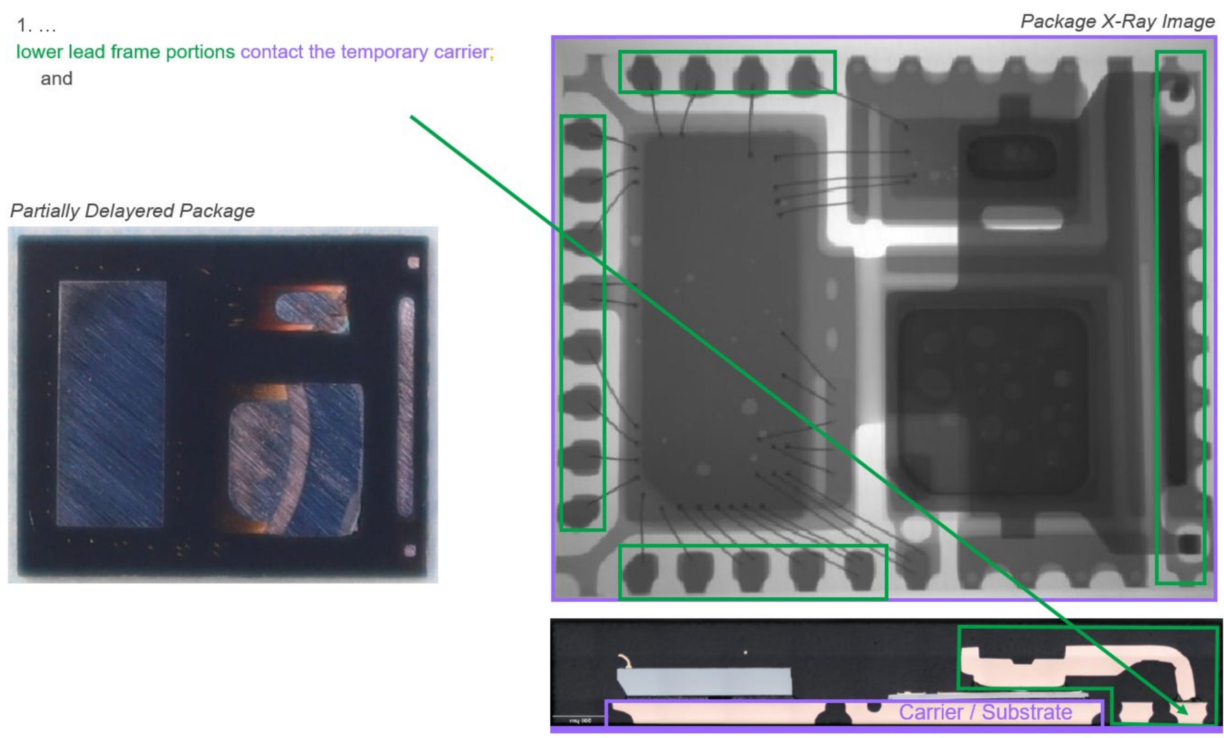
Partially Delayered Package

Package Cross-Section Image

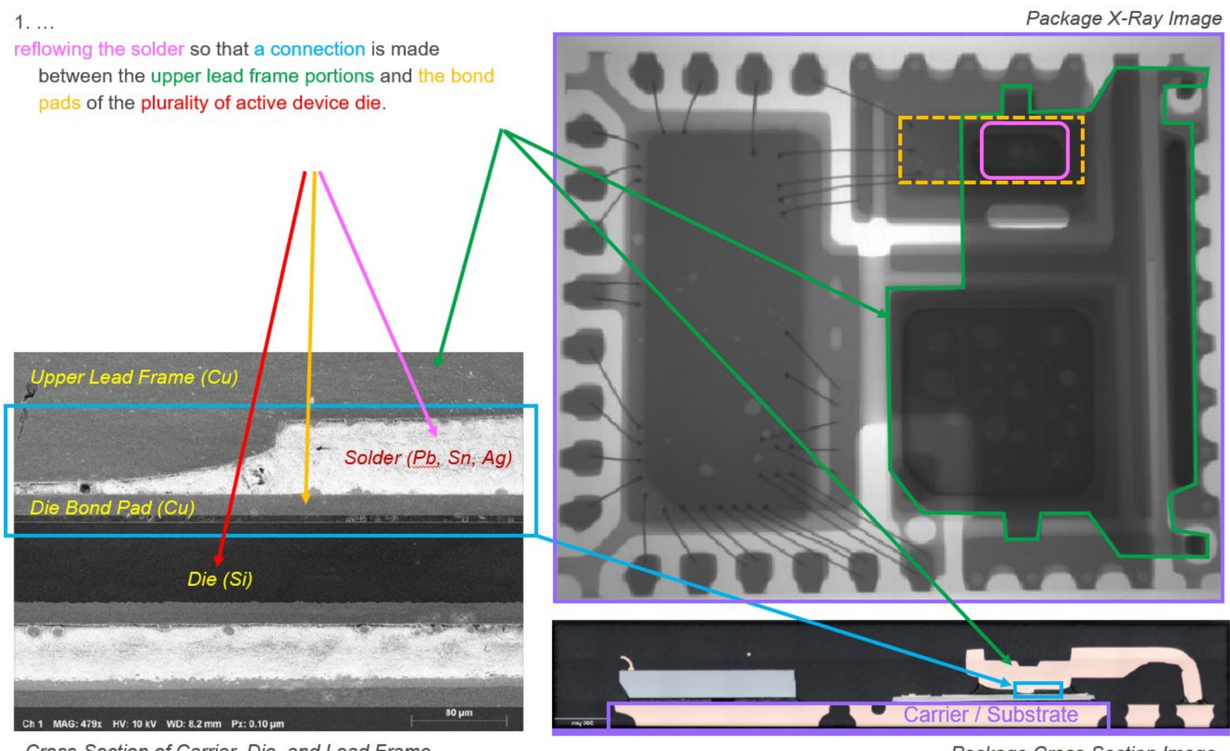
46. On information and belief, the Accused Products are manufactured using a process wherein the upper lead frame portions contact the solder paste present on the bond pads.



47. On information and belief, the Accused Products are manufactured using a process wherein the lower lead frame portions contact the temporary carrier.



48. On information and belief, the Accused Products are manufactured using a process that reflows the solder so that a connection is made between the upper lead frame portions and the bond pads of the plurality of active device die.



49. Fact and expert discovery are expected to confirm that the Accused Products infringe the ’299 Patent, for which further evidence may lie in whole or in part in technical documents to which Chip Packaging does not presently have access.

50. Further, on information and belief, Defendant has and continues to indirectly infringe one or more claims of the ’299 Patent, including claim 1, by knowingly and intentionally inducing others, including third-party semiconductor foundries, other types of third-party manufacturers, customers, and/or end-users to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

51. Defendant, with knowledge that these products, and/or the manufacture thereof, infringe the ’299 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce direct infringement of the ’299 Patent by contracting for the third-party manufacture of, and/or providing the Accused Products to direct infringers.

52. Defendant has induced infringement by others, including third-party semiconductor foundries, other types of third-party manufacturers, customers, and/or end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others infringe the ’299 Patent, but while remaining willfully blind to the infringement.

53. Defendant has and continues to infringe one or more claims of the ’299 Patent by importing into the United States or offering to sell, selling, or using within the United States a product which is made by a process patented in the United States.

54. Defendant is not licensed or otherwise authorized to practice the claims of the ’299 Patent.

55. Thus, by its acts, Defendant has injured Chip Packaging and is liable to Chip Packaging for directly and/or indirectly infringing one or more claims of the ’299 Patent, whether literally or under the doctrine of equivalents, including without limitation claim 1.

56. As a result of Defendant’s infringement of the ’299 Patent, Chip Packaging has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for Defendant’s infringement, but in no event less than a reasonable royalty with interest and costs.

SECOND COUNT
(Infringement of U.S Patent No. 9,299,646)

57. Chip Packaging incorporates by reference the allegations set forth in Paragraphs 1-56 of the Complaint as though fully set forth herein.

58. The claims of the ’646 Patent are valid and enforceable.

59. Infineon has and continues to directly infringe the ’646 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products made using the patented methods including, but not limited to, products that satisfy each and every limitation of one or more claims of the ’646 Patent. Upon information and belief, such products include at least the Infineon 32-bit TriCore AUDO MAX MCU Package TC1782N320F180HRBAKXUMA2 and all other products with power and ground bar arrangements that are not colorably different.

60. For example, the Accused Products incorporates and/or implements elements that are identical or equivalent to each claimed element of the patented invention pointed out by at least Claim 1 of the ’646 Patent.

61. Claim 1 of the ’646 Patent recites:

1. A semiconductor device, comprising:

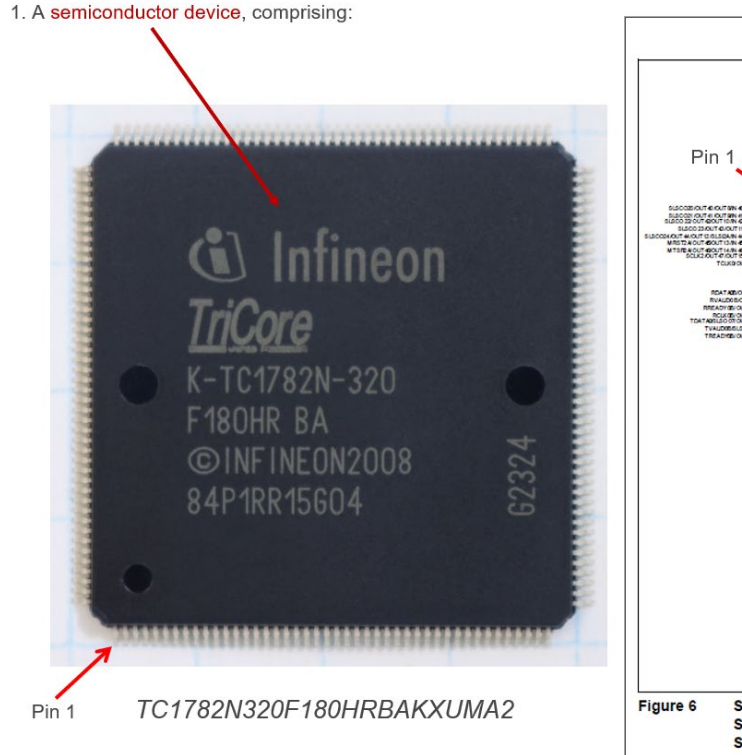
> a semiconductor die having a plurality of first contact pads and at least one second contact pad disposed on or exposed through a surface thereof;
>
> a package casing that covers the semiconductor die;
>
> a plurality of signal leads spaced apart from the semiconductor die and each having an embedded portion located within the package casing and an exposed portion located outside of the package casing, each of the signal leads being electrically connected to a respective one of the first contact pads;
>
> a power bar extending at least partially in an area between the embedded portions of the plurality of signal leads and the semiconductor die and having a first side opposing the signal leads and a second side opposing

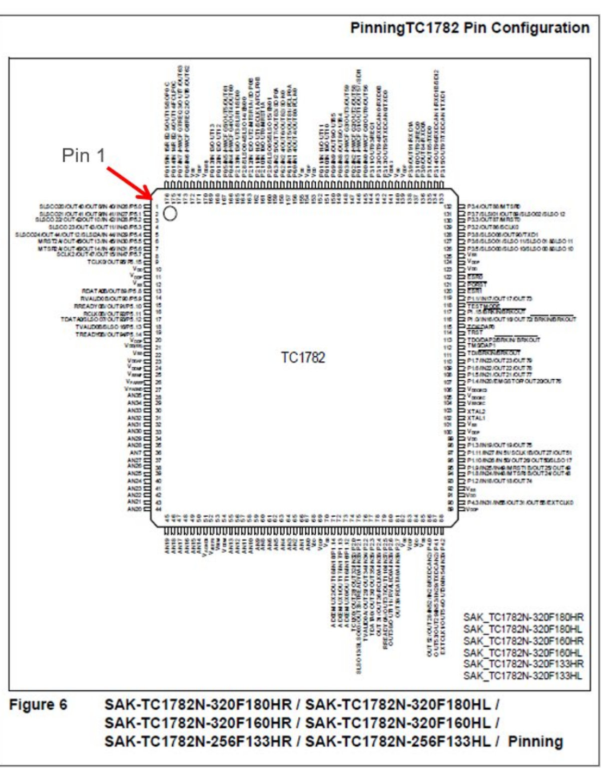
the semiconductor die, the power bar being electrically connected to the at least one second contact pad; and

a ground bar that is electrically grounded and extends at least partially in said area, the ground bar having a first portion disposed between the embedded portions of the plurality of signal leads and the first side of the power bar, and a second portion disposed between the second side of the power bar and the semiconductor die.

’646 Patent, Cl. 1.

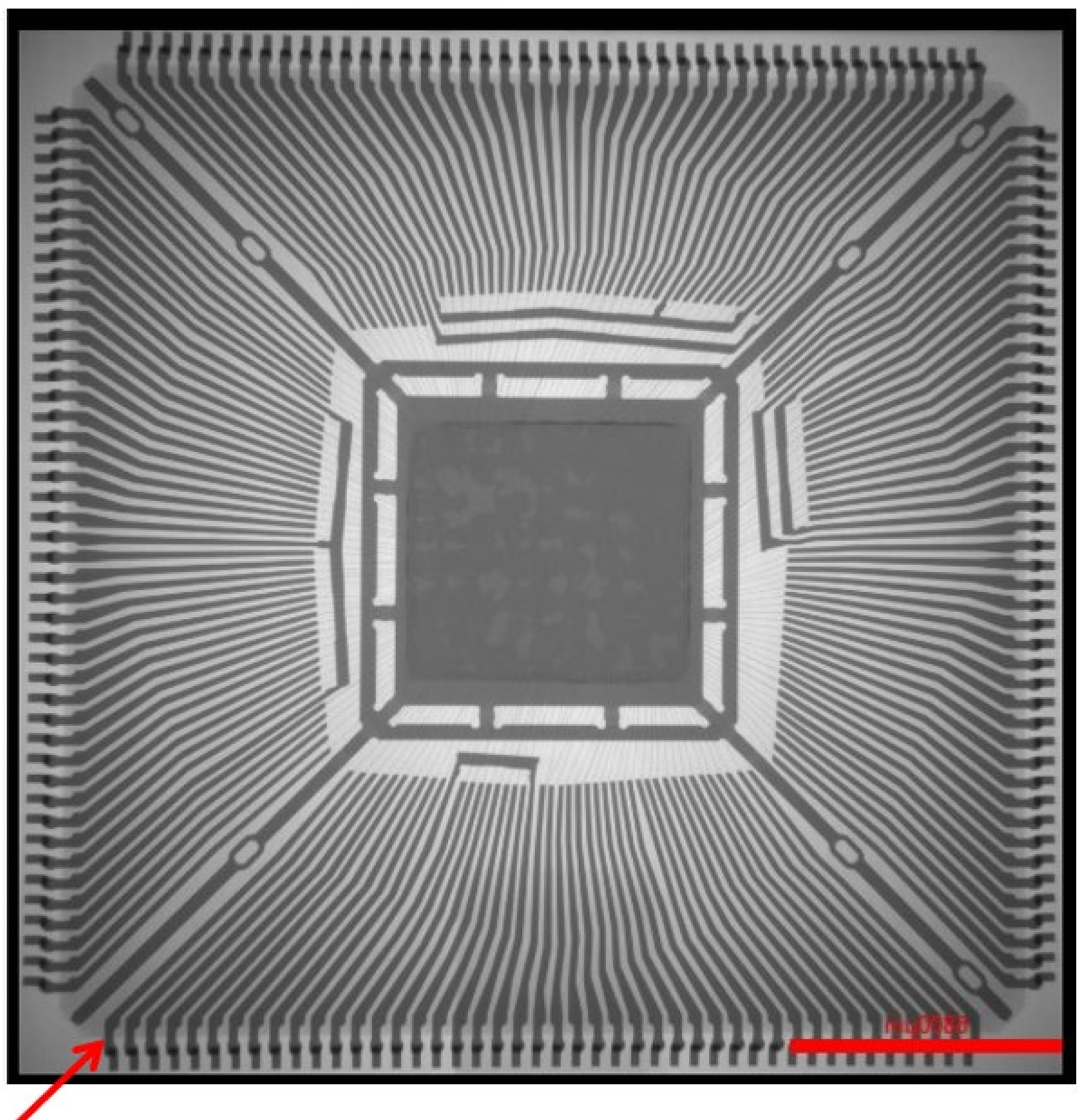
62. For example, the Infineon 32-bit MCU TriCore Package is a semiconductor device:





Source: Infineon TriCore TC1782 32-Bit MCU Datasheet

Infineon TriCore Package X–Ray Image

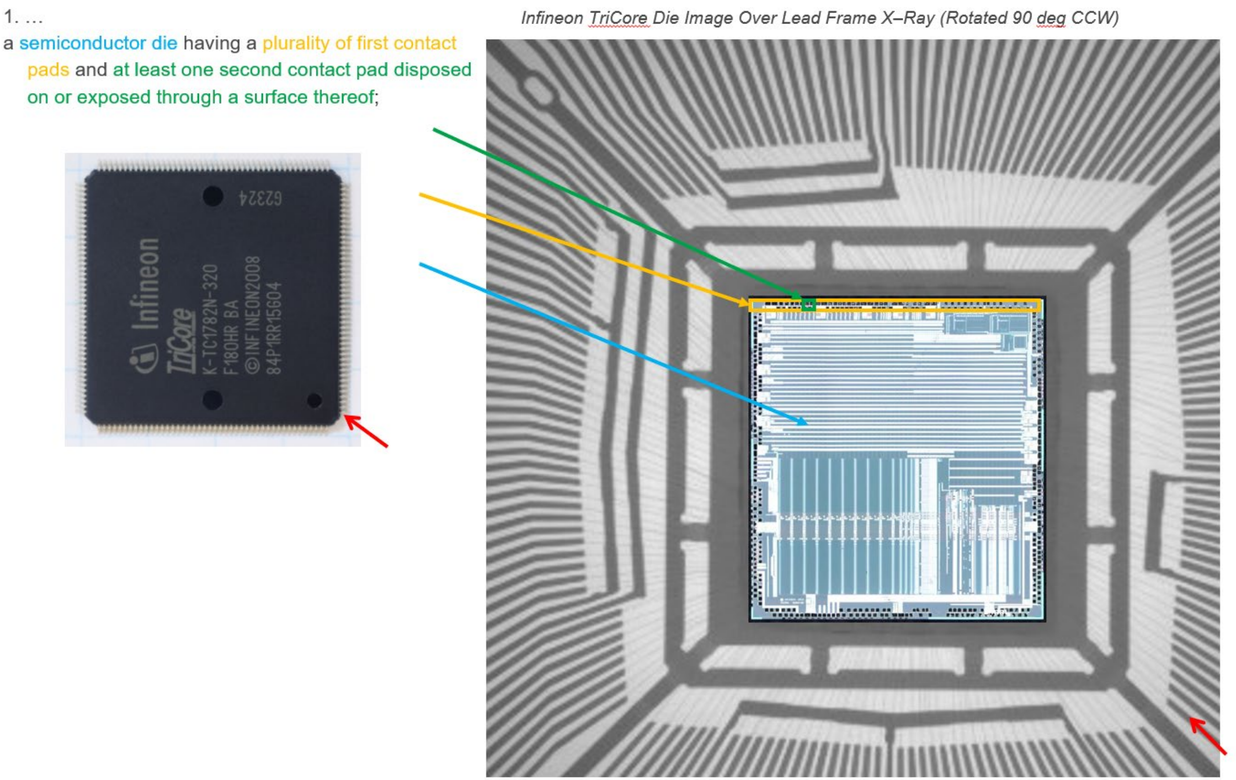


Pin 1

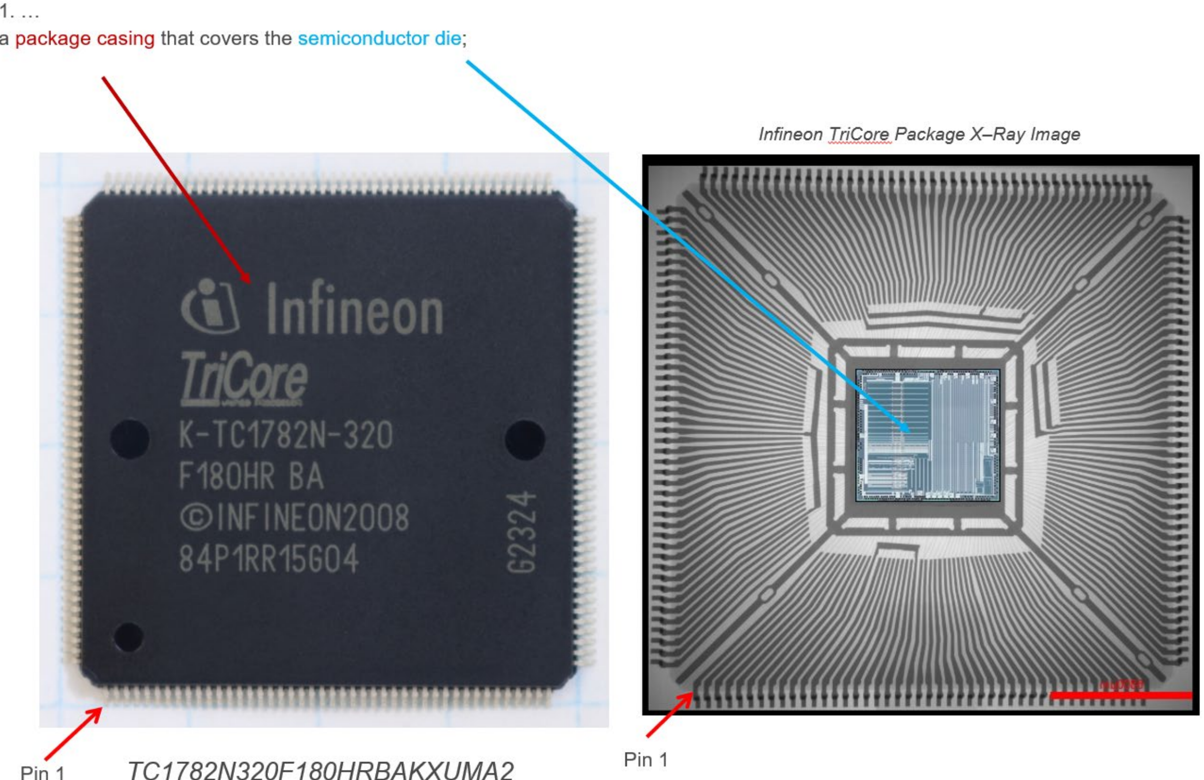
Infineon TriCore Die Image Overlayed Onto Lead Frame X–Ray Image

Pin 1

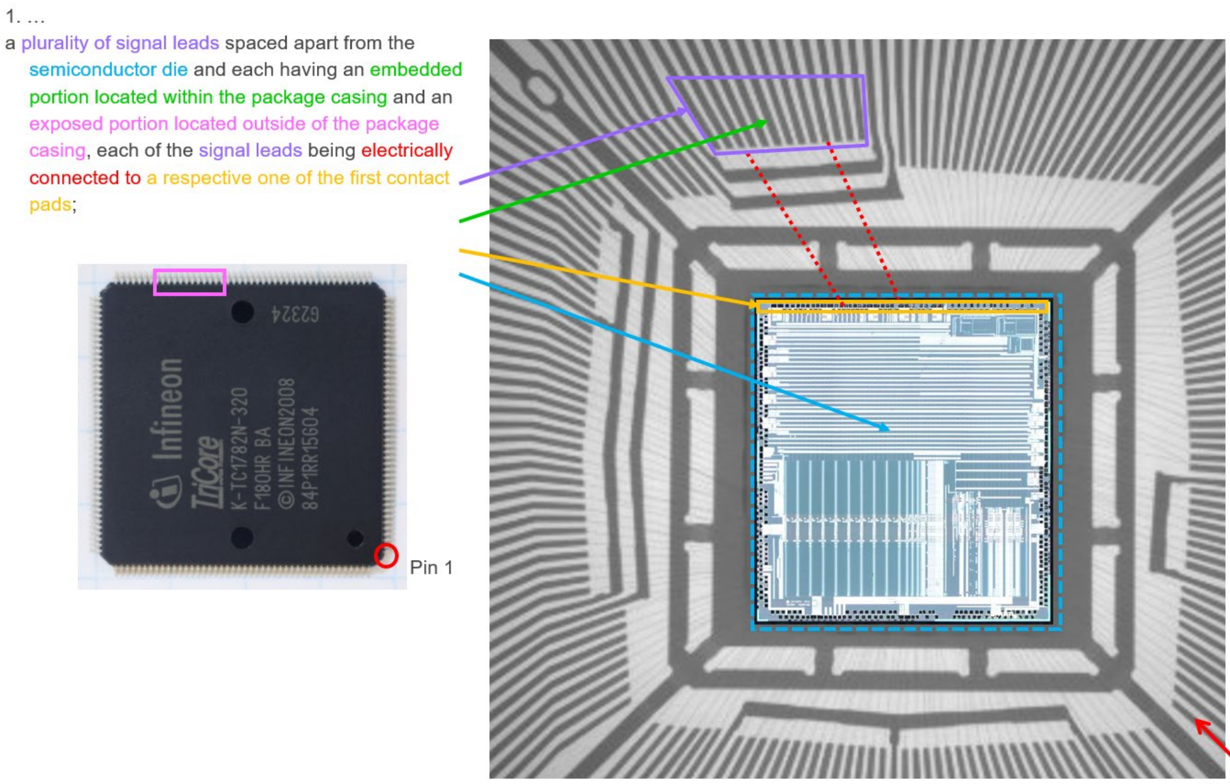
63. On information and belief, the Infineon 32-bit MCU TriCore Package includes a semiconductor die having a plurality of first contact pads and at least one second contact pad disposed on or exposed through a surface thereof.



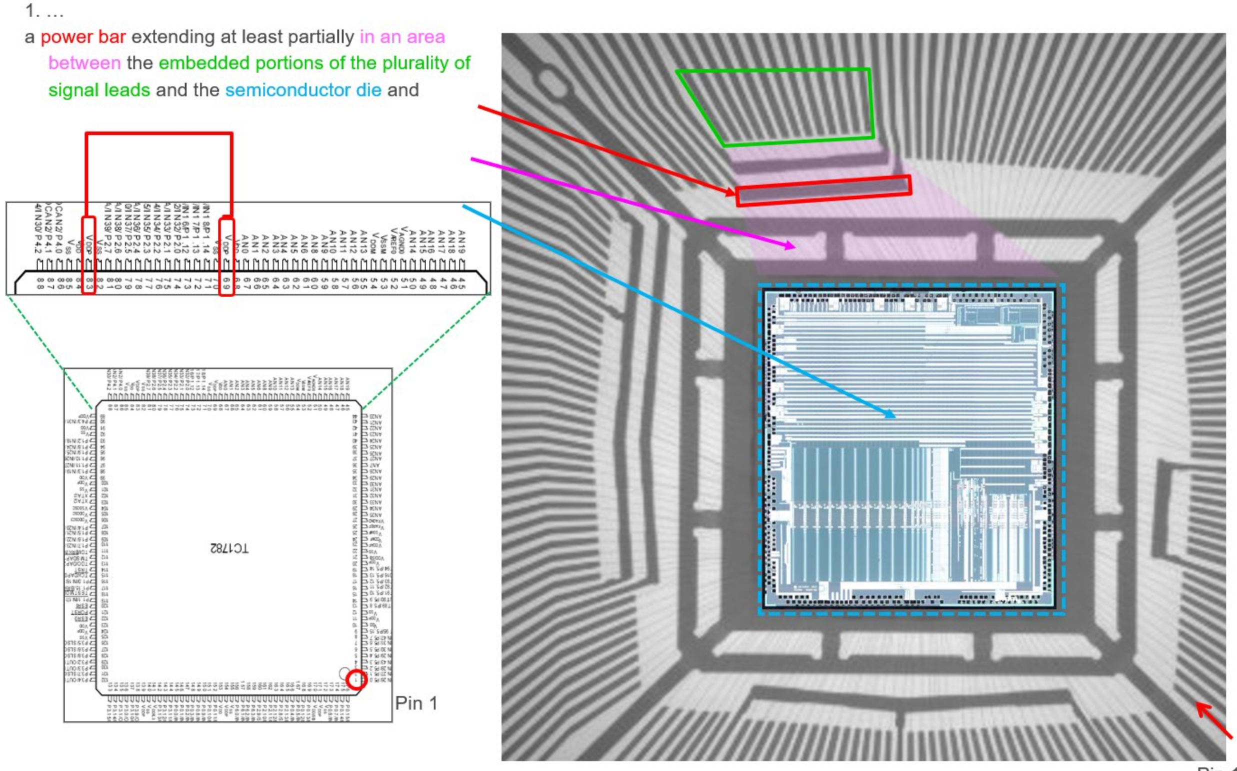
64. On information and belief, the Infineon 32-bit MCU TriCore Package includes a package casing that covers the semiconductor die.



65. On information and belief, the Infineon 32-bit MCU TriCore Package includes a plurality of signal leads spaced apart from the semiconductor die and each having an embedded portion located within the package casing and an exposed portion located outside of the package casing, each of the signal leads being electrically connected to a respective one of the first contact pads.

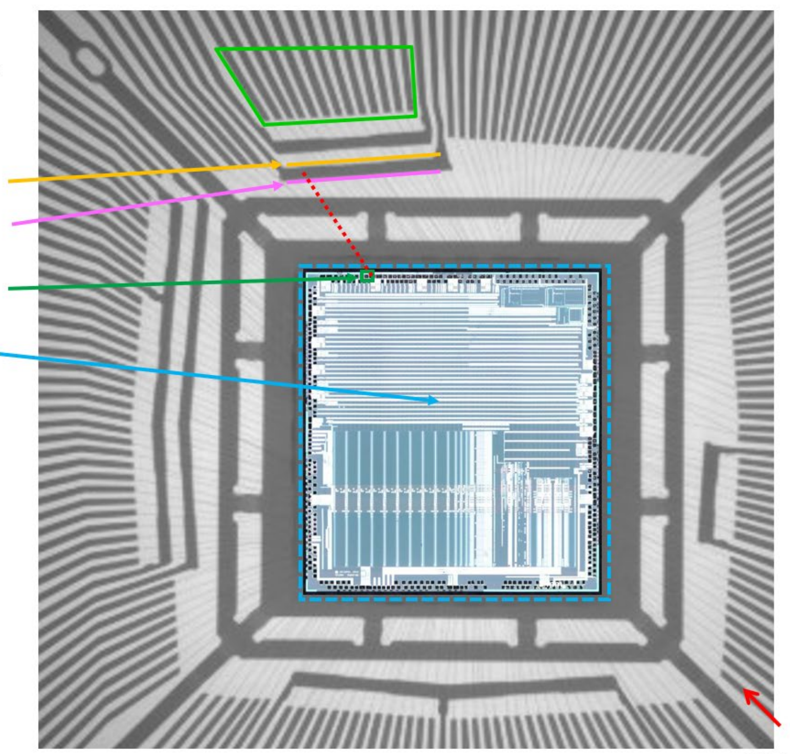


66. On information and belief, the Infineon 32-bit MCU TriCore Package includes a power bar extending at least partially in an area between the embedded portions of the plurality of signal leads and the semiconductor die.

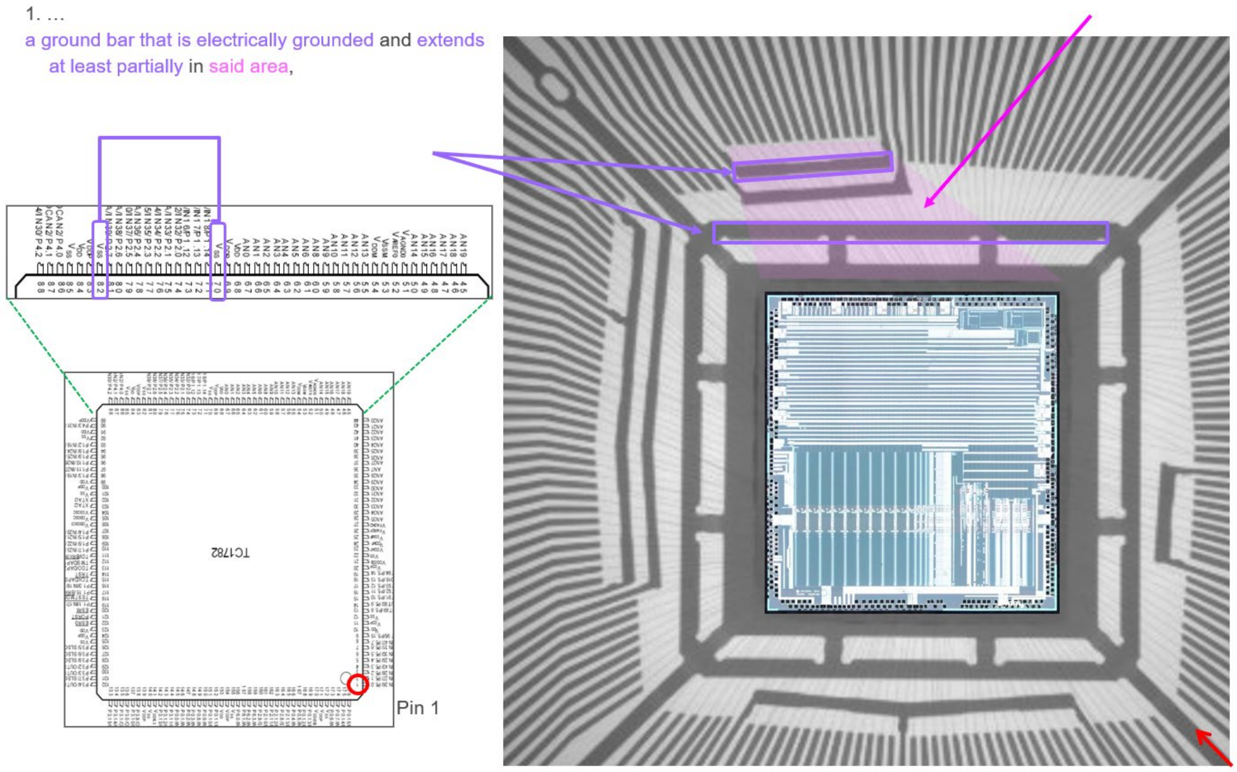


67. On information and belief, the Infineon 32-bit MCU TriCore Package includes a power bar having a first side opposing the signal leads and a second side opposing the semiconductor die, the power bar being electrically connected to the at least one second contact pad.

1. …
having a first side opposing the signal leads and a second side opposing the semiconductor die, the power bar being electrically connected to the at least one second contact pad; and

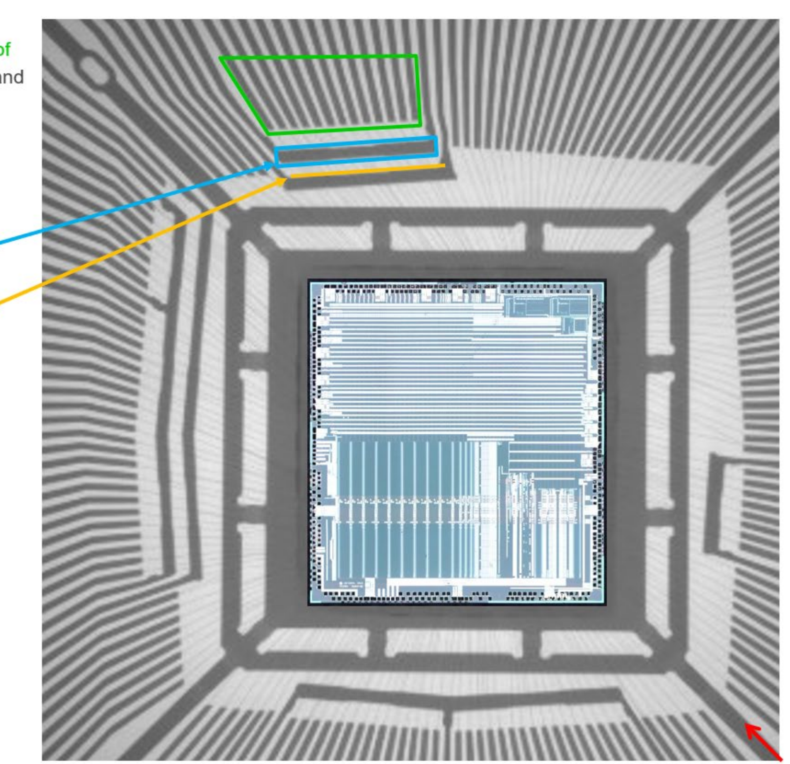


68. On information and belief, the Infineon 32-bit MCU TriCore Package includes a ground bar that is electrically grounded and extends at least partially in said area.



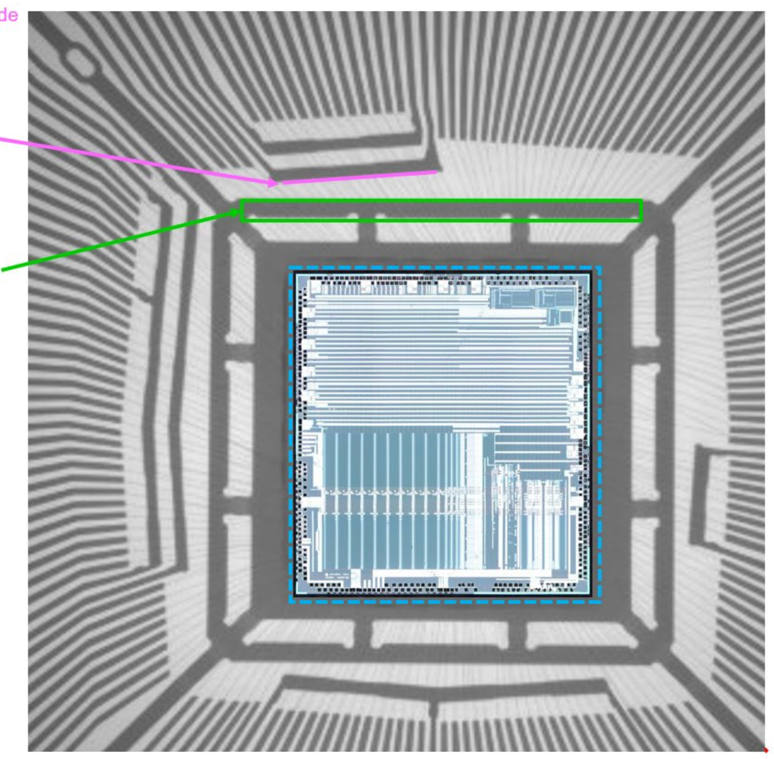
69. On information and belief, the Infineon 32-bit MCU TriCore Package includes a ground bar having a first portion disposed between the embedded portions of the plurality of signal leads and the first side of the power bar.

1. ...
the ground bar having a first portion disposed between the embedded portions of the plurality of signal leads and the first side of the power bar, and



70. On information and belief, the Infineon 32-bit MCU TriCore Package includes a ground bar having a second portion disposed between the second side of the power bar and the semiconductor die.

1. ...
a second portion disposed between the second side of the power bar and the semiconductor die.



Pin 1

71. Fact and expert discovery are expected to confirm that the Accused Products infringe the ’646 Patent, for which further evidence may lie in whole or in part in technical documents to which Chip Packaging does not presently have access.

72. Further, on information and belief, Defendant has and continues to indirectly infringe one or more claims of the ’646 Patent, including claim 1, by knowingly and intentionally inducing others, including third-party semiconductor foundries, other types of third-party manufacturers, customers, and/or end-users to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

73. Defendant, with knowledge that these products, and/or the manufacture thereof, infringe the ’646 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce direct infringement of the ’646

Patent by contracting for the third-party manufacture of, and/or providing the Accused Products to direct infringers.

74. Defendant has induced infringement by others, including third-party semiconductor foundries, other types of third-party manufacturers, customers, and/or end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others infringe the ’646 Patent, but while remaining willfully blind to the infringement.

75. Defendant is not licensed or otherwise authorized to practice the claims of the ’646 Patent.

76. Thus, by its acts, Defendant has injured Chip Packaging and is liable to Chip Packaging for directly and/or indirectly infringing one or more claims of the ’646 Patent, whether literally or under the doctrine of equivalents, including without limitation claim 1.

77. As a result of Defendant’s infringement of the ’646 Patent, Chip Packaging has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for Defendant’s infringement, but in no event less than a reasonable royalty with interest and costs.

THIRD COUNT
(Infringement of U.S Patent No. 8,258,611)

78. Chip Packaging incorporates by reference the allegations set forth in Paragraphs 1-77 of the Complaint as though fully set forth herein.

79. The claims of the ’611 Patent are valid and enforceable.

80. Infineon has and continues to directly infringe the ’611 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products made using the patented methods including, but not limited to, products that satisfy each and every

limitation of one or more claims of the ’611 Patent. Upon information and belief, such products include at least the Infineon IGI60F1414A1 CoolGaN Integrated Power Stage, Infineon TLF51801 OPTIREG Asynchronous DC/DC Step-Down Converter, Infineon TLE9872QT MOTIX Microcontroller, and Infineon TLE9461ES OPTIREG Power Management IC and all other products with delamination barrier structures that are not colorably different, including but not limited to CY9BF364LPMC1-G-JNE2, S6E1C12C0AGV20000, TC213L8F133NACKXUMA1, TC223S16F133FACKXUMA1, TC234L32F200NACKXUMA1, TC265D40F200NBCKXUMA1, TC275T64F200WDCKXUMA1, TC322LP16F160FAAKXUMA1, TC333LP32F200FAAKXUMA1, TC364DP64F300FAALXUMA1, TLE9877QTW40XUMA1.

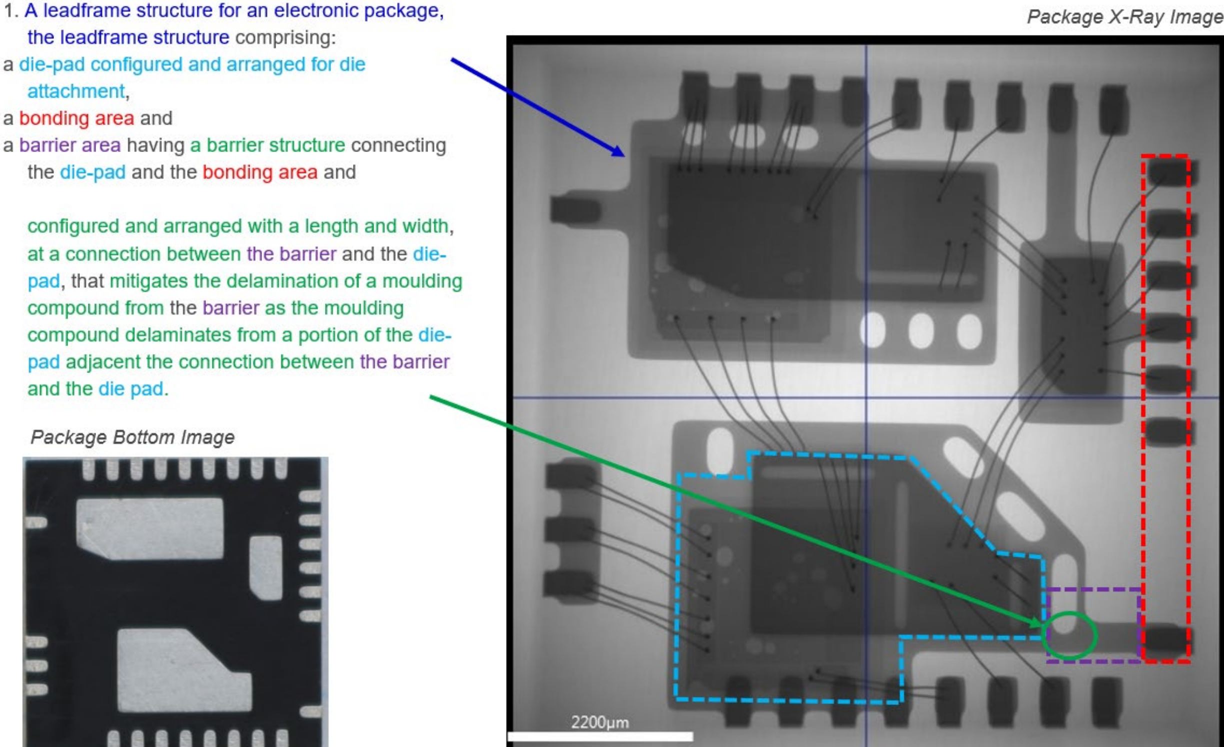
81. For example, the Accused Products incorporates and/or implements elements that are identical or equivalent to each claimed element of the patented invention pointed out by at least Claim 1 of the ’611 Patent.

82. Claim 1 of the ’611 Patent recites:

> 1. A leadframe structure for an electronic package, the leadframe structure comprising:
>
> a die-pad configured and arranged for die attachment,
>
> a bonding area and
>
> a barrier area having a barrier structure connecting the die-pad and the bonding area and configured and arranged with a length and width, at a connection between the barrier and the die-pad, that mitigates the delamination of a moulding compound from the barrier as the moulding compound delaminates from a portion of the die-pad adjacent the connection between the barrier and the die pad.

’611 Patent, Cl. 1.

83. For example, the Infineon IGI60F1414A1 is a lead frame structure for an electronic package that satisfies each claim element.

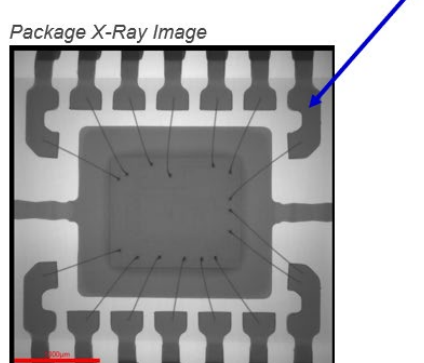


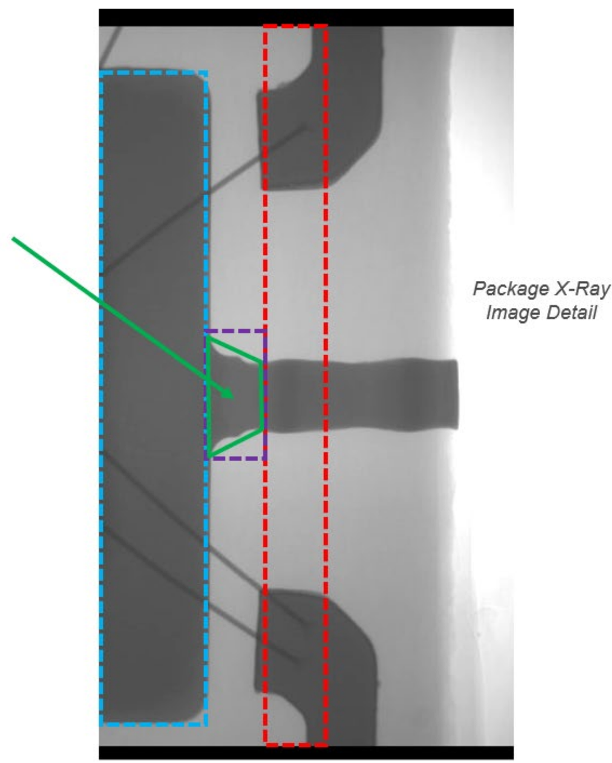
84. As another example, the Infineon TLF51801ELV is a lead frame structure for an electronic package that satisfies each claim element.

1. A leadframe structure for an electronic package, the leadframe structure comprising:
a die-pad configured and arranged for die attachment,
a bonding area and
a barrier area having a barrier structure connecting the die-pad and the bonding area and

configured and arranged with a length and width, at a connection between the barrier and the die-pad, that mitigates the delamination of a moulding compound from the barrier as the moulding compound delaminates from a portion of the die-pad adjacent the connection between the barrier and the die pad.

Package X-Ray Image





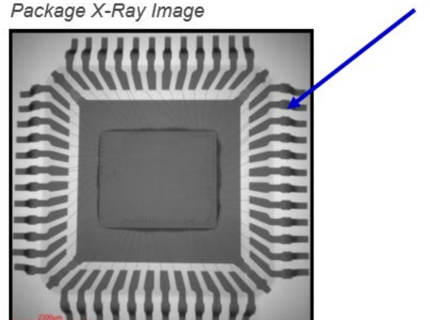
Package X-Ray Image Detail

85. As another example, the Infineon TLE9872QT is a lead frame structure for an electronic package that satisfies each claim element.

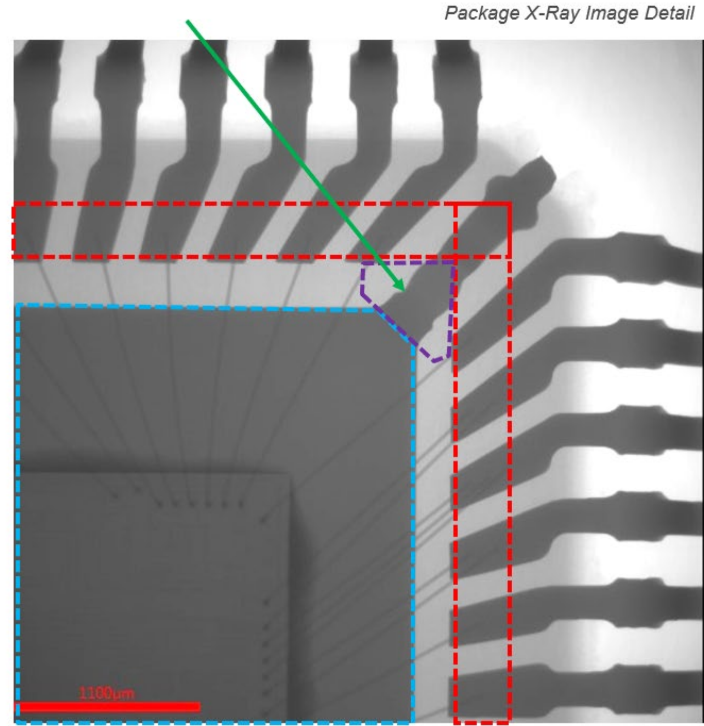
1. A leadframe structure for an electronic package, the leadframe structure comprising:
a die-pad configured and arranged for die attachment,
a bonding area and
a barrier area having a barrier structure connecting the die-pad and the bonding area and

configured and arranged with a length and width, at a connection between the barrier and the die-pad, that mitigates the delamination of a moulding compound from the barrier as the moulding compound delaminates from a portion of the die-pad adjacent the connection between the barrier and the die pad.

Package X-Ray Image



Package X-Ray Image Detail

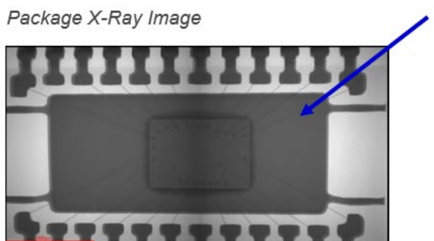


86. As another example, the Infineon TLE9461ES is a lead frame structure for an electronic package that satisfies each claim element.

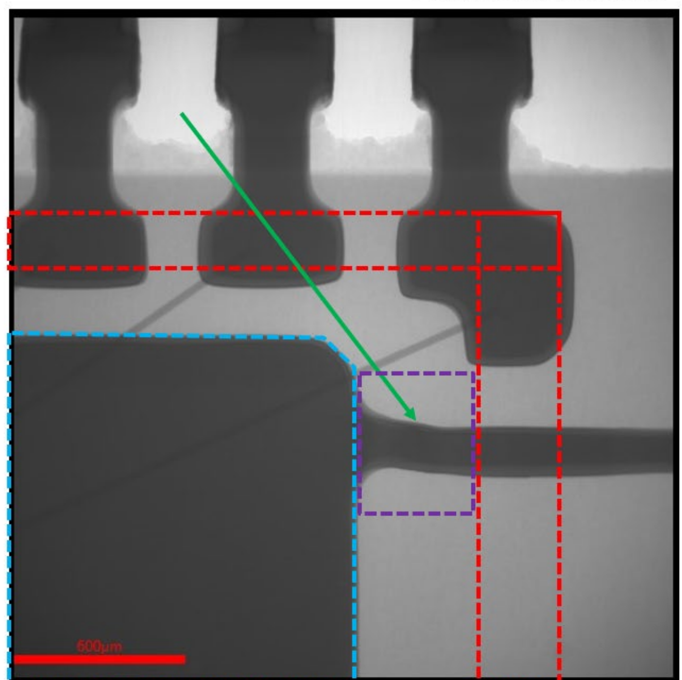
1. A leadframe structure for an electronic package, the leadframe structure comprising:
a die-pad configured and arranged for die attachment,
a bonding area and
a barrier area having a barrier structure connecting the die-pad and the bonding area and

configured and arranged with a length and width, at a connection between the barrier and the die-pad, that mitigates the delamination of a moulding compound from the barrier as the moulding compound delaminates from a portion of the die-pad adjacent the connection between the barrier and the die pad.

Package X-Ray Image



Package X-Ray Image Detail



87. Fact and expert discovery are expected to confirm that the Accused Products infringe the ’611 Patent, for which further evidence may lie in whole or in part in technical documents to which Chip Packaging does not presently have access.

88. Further, on information and belief, Defendant has and continues to indirectly infringe one or more claims of the ’611 Patent, including claim 1, by knowingly and intentionally inducing others, including third-party semiconductor foundries, other types of third-party manufacturers, customers, and/or end-users to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

89. Defendant, with knowledge that these products, and/or the manufacture thereof, infringe the ’611 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce direct infringement of the ’911

Patent by contracting for the third-party manufacture of, and/or providing the Accused Products to direct infringers.

90. Defendant has induced infringement by others, including third-party semiconductor foundries, other types of third-party manufacturers, customers, and/or end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others infringe the ’611 Patent, but while remaining willfully blind to the infringement.

91. Defendant is not licensed or otherwise authorized to practice the claims of the ’611 Patent.

92. Thus, by its acts, Defendant has injured Chip Packaging and is liable to Chip Packaging for directly and/or indirectly infringing one or more claims of the ’611 Patent, whether literally or under the doctrine of equivalents, including without limitation claim 1.

93. As a result of Defendant’s infringement of the ’611 Patent, Chip Packaging has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for Defendant’s infringement, but in no event less than a reasonable royalty with interest and costs.

FOURTH COUNT
(Infringement of U.S Patent No. 9,685,351)

94. Chip Packaging incorporates by reference the allegations set forth in Paragraphs 1-93 of the Complaint as though fully set forth herein.

95. The claims of the ’351 Patent are valid and enforceable.

96. Infineon has and continues to directly infringe the ’351 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products made using the patented methods including, but not limited to, products that satisfy each and every

limitation of one or more claims of the ’351 Patent. Upon information and belief, such products include at least the Infineon TC1782 TriCore 32-bit AUDO MAX MCU and all other products with positive mold lock structures that are not colorably different, including but not limited to TC213L8F133NACKXUMA1, TC223S16F133FACKXUMA1, TC234L32F200NACKXUMA1, TC265D40F200NBCKXUMA1, TC275T64F200WDCKXUMA1, TC322LP16F160FAAKXUMA1, TC333LP32F200FAAKXUMA1, TC364DP64F300FAALXUMA1.

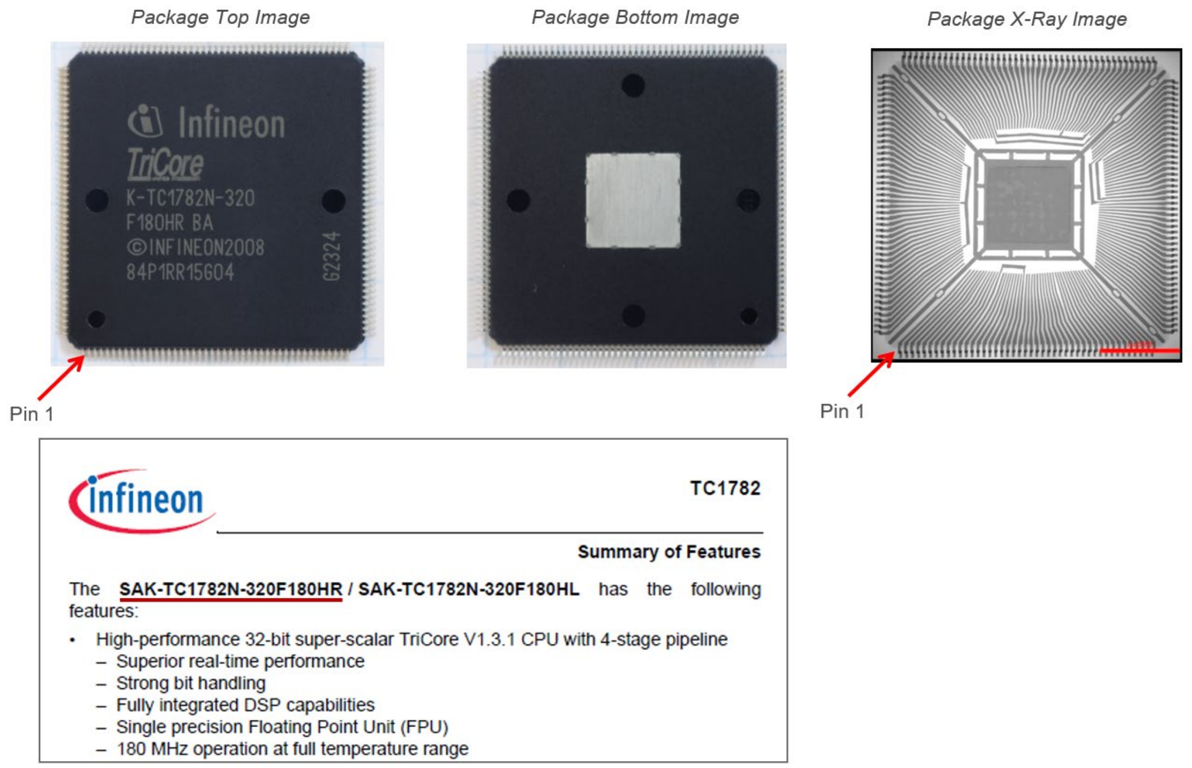
97. For example, the Accused Products incorporates and/or implements elements that are identical or equivalent to each claimed element of the patented invention pointed out by at least Claim 1 of the ’351 Patent.

98. Claim 1 of the ’351 Patent recites:

> 1. A method comprising:
>
> providing a lead frame comprising a first die paddle and one or more electrical connector elements; and
>
> forming one or more positive mold lock structures at predetermined locations on a top surface of the lead frame which laterally protrude above the top surface.

’351 Patent, Cl. 1.

99. For example, the Infineon 32-bit AUDO MAX MCU implements a method for fabricating a microchip structure. The microchip structure of the Infineon AUDO MAX 32-bit MCU is illustrated below:



infineon

TC1782

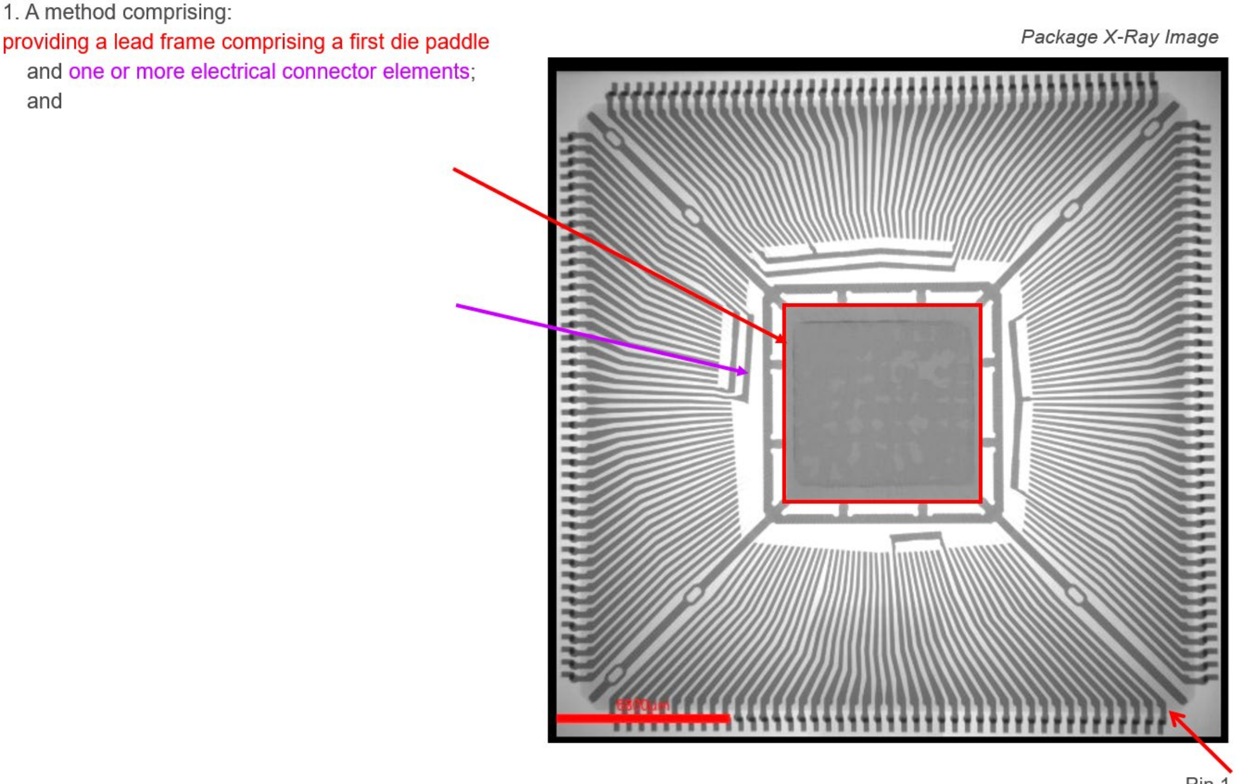
Summary of Features

The SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL has the following features:

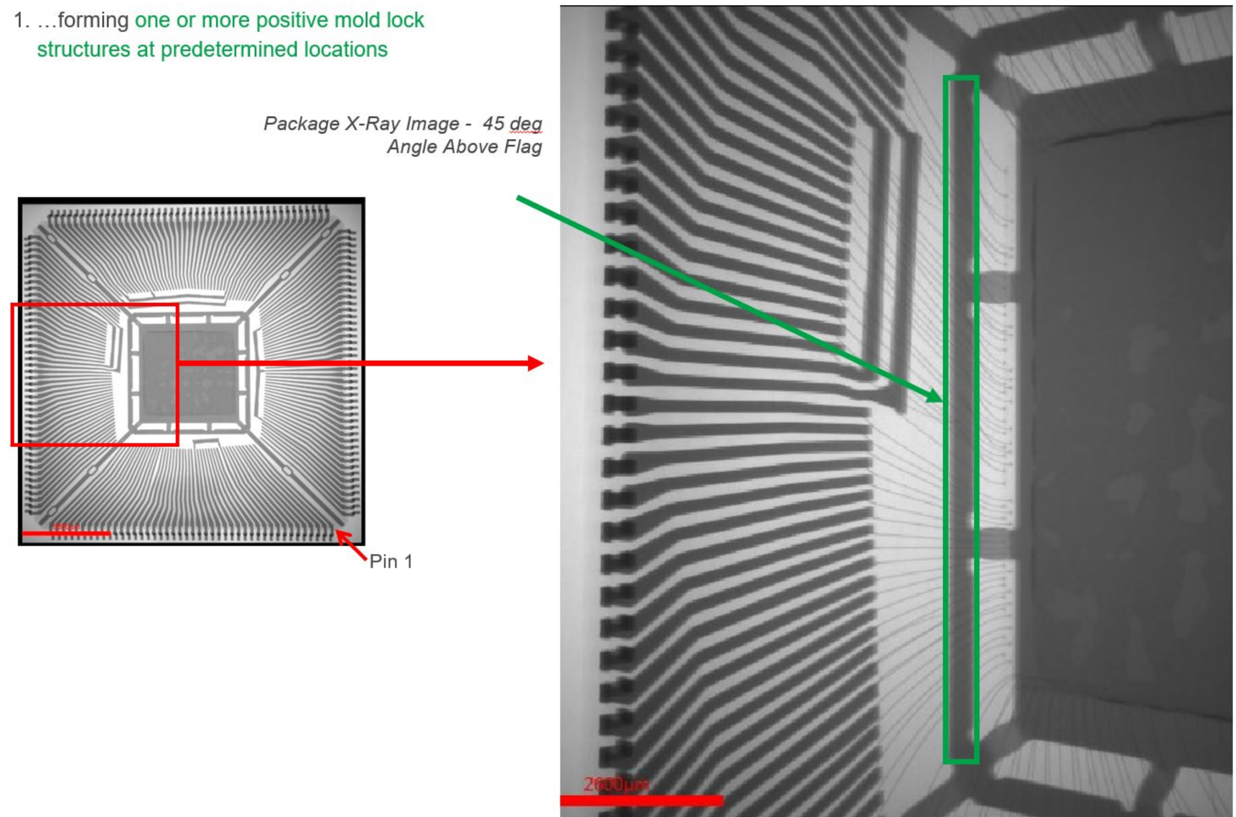
- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 180 MHz operation at full temperature range

Source: Infineon TC1782 Datasheet

100. On information and belief, the Accused Products are manufactured using a process that provides a lead frame comprising a first die paddle and one or more electrical connector elements.

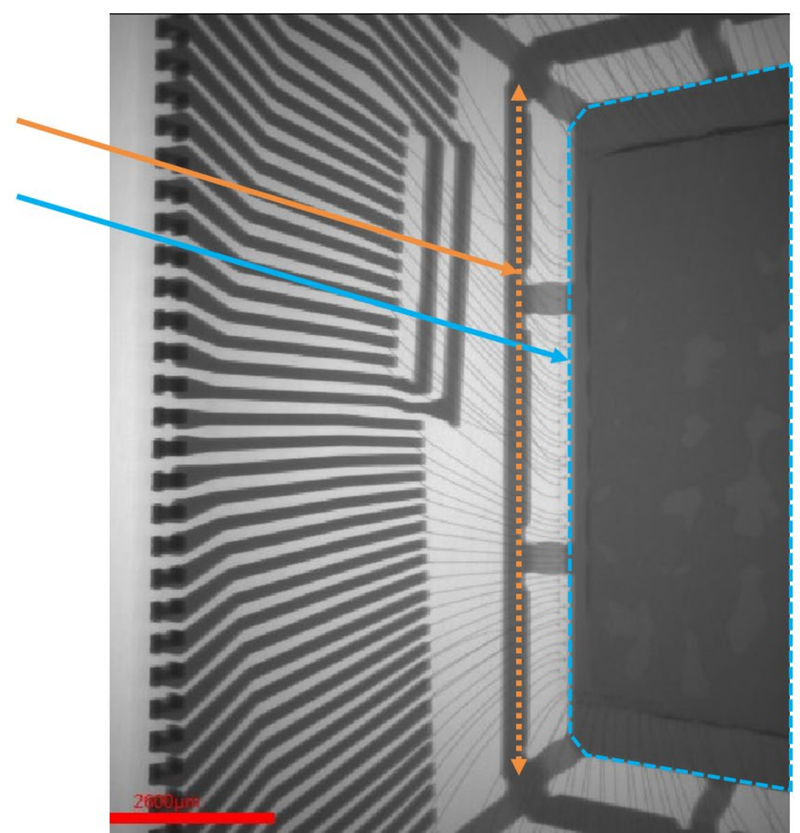


101. On information and belief, within the Accused Products are manufactured using a process that forms one or more positive mold lock structures at predetermined locations.



102. On information and belief, within the Accused Products are manufactured using a process that forms one or more positive mold lock structures at predetermined locations on a top surface of the lead frame which laterally protrude above the top surface.

1. …on a top surface of the lead frame which laterally protrude above the top surface.



103. Fact and expert discovery are expected to confirm that the Accused Products infringe the ’351 Patent, for which further evidence may lie in whole or in part in technical documents to which Chip Packaging does not presently have access.

104. Further, on information and belief, Defendant has and continues to indirectly infringe one or more claims of the ’351 Patent, including claim 1, by knowingly and intentionally inducing others, including third-party semiconductor foundries, other types of third-party manufacturers, customers, and/or end-users to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

105. Defendant, with knowledge that these products, and/or the manufacture thereof, infringe the ’351 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce direct infringement of the ’351

Patent by contracting for the third-party manufacture of, and/or providing the Accused Products to direct infringers.

106. Defendant has induced infringement by others, including third-party semiconductor foundries, other types of third-party manufacturers, customers, and/or end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others infringe the ’351 Patent, but while remaining willfully blind to the infringement.

107. Defendant has and continues to infringe one or more claims of the ’351 Patent by importing into the United States or offering to sell, selling, or using within the United States a product which is made by a process patented in the United States.

108. Defendant is not licensed or otherwise authorized to practice the claims of the ’351 Patent.

109. Thus, by its acts, Defendant has injured Chip Packaging and is liable to Chip Packaging for directly and/or indirectly infringing one or more claims of the ’351 Patent, whether literally or under the doctrine of equivalents, including without limitation claim 1.

110. As a result of Defendant’s infringement of the ’351 Patent, Chip Packaging has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for Defendant’s infringement, but in no event less than a reasonable royalty with interest and costs.

FIFTH COUNT
(Infringement of U.S Patent No. 8,394,713)

111. Chip Packaging incorporates by reference the allegations set forth in Paragraphs 1-110 of the Complaint as though fully set forth herein.

112. The claims of the ’713 Patent are valid and enforceable.

113. Infineon has and continues to directly infringe the ’713 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products made using the patented methods including, but not limited to, products that satisfy each and every limitation of one or more claims of the ’713 Patent. Upon information and belief, such products include at least the Infineon IGI60F1414A1L CoolGaN product line and all other products with a nickel layer on a bond pad and a palladium layer that are not colorably different.

114. For example, the Accused Products incorporates and/or implements elements that are identical or equivalent to each claimed element of the patented invention pointed out by at least Claim 1 of the ’713 Patent.

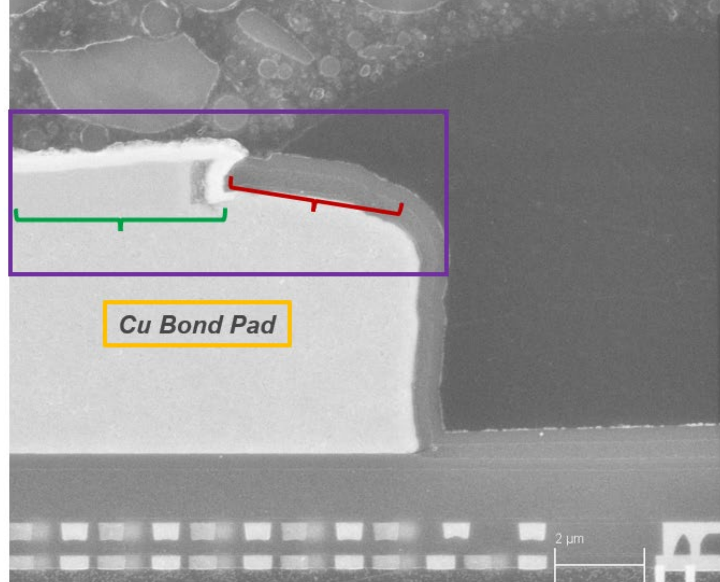
115. Claim 1 of the ’713 Patent recites:

> 1. A method for forming over pad metallization (OPM) on a semiconductor die having a bond pad in which the bond pad has an inner portion surrounded by a passivation layer, comprising:
>
> > depositing a nickel layer on the bond pad, wherein a lack of adhesion between the nickel layer and the passivation layer results in a space between the nickel layer and the passivation layer down to the bond pad;
> >
> > applying an isotropic etchant selective for nickel to the nickel layer to widen the space between the nickel layer and the passivation layer down to the bond pad; and
> >
> > depositing a palladium layer on the nickel layer and in the space so as to be in contact, in the space, with the bond pad, the passivation layer, and the nickel layer.

’713 Patent, Cl. 1.

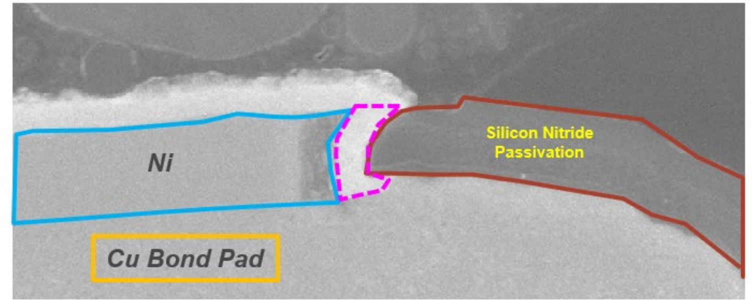
116. For example, the Infineon IGI60F1414A1L CoolGaN implements a method for forming over pad metallization on a semiconductor die having a bond pad in which the bond pad has an inner portion surrounded by a passivation layer.

1. A method for forming over pad metallization (OPM) on a semiconductor die having a bond pad in which the bond pad has an inner portion surrounded by a passivation layer, comprising:
depositing a nickel layer on the bond pad, wherein a lack of adhesion between the nickel layer and the passivation layer results in a space between the nickel layer and the passivation layer down to the bond pad;
applying an isotropic etchant selective for nickel to the nickel layer to widen the space between the nickel layer and the passivation layer down to the bond pad; and
depositing a palladium layer on the nickel layer and in the space so as to be in contact, in the space, with the bond pad, the passivation layer, and the nickel layer.



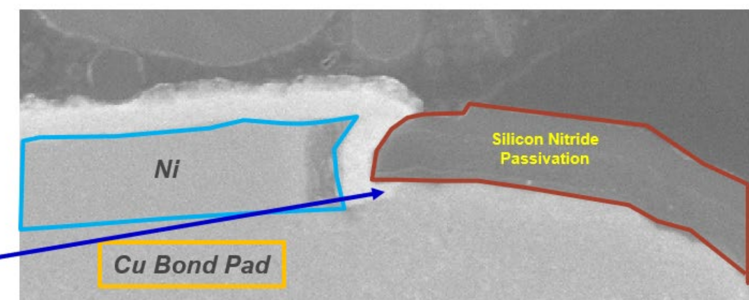
117. On information and belief, the Accused Products are manufactured using a process that deposits a nickel layer on the bond pad, wherein a lack of adhesion between the nickel layer and the passivation layer results in a space between the nickel layer and the passivation layer down to the bond pad.

1. A method for forming over pad metallization (OPM) on a semiconductor die having a bond pad in which the bond pad has an inner portion surrounded by a passivation layer, comprising:
depositing a nickel layer on the bond pad, wherein a lack of adhesion between the nickel layer and the passivation layer results in a space between the nickel layer and the passivation layer down to the bond pad;
applying an isotropic etchant selective for nickel to the nickel layer to widen the space between the nickel layer and the passivation layer down to the bond pad; and
depositing a palladium layer on the nickel layer and in the space so as to be in contact, in the space, with the bond pad, the passivation layer, and the nickel layer.



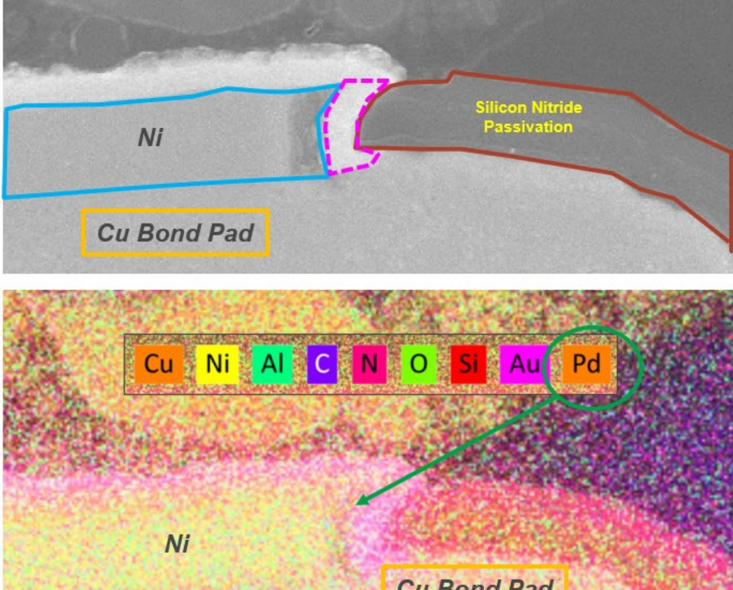
118. On information and belief, the Accused Products are manufactured using a process that applies an isotropic etchant selective for nickel to the nickel layer to widen the space between the nickel layer and the passivation layer down to the bond pad.

1. A method for forming over pad metallization (OPM) on a semiconductor die having a bond pad in which the bond pad has an inner portion surrounded by a passivation layer, comprising:
depositing a nickel layer on the bond pad, wherein a lack of adhesion between the nickel layer and the passivation layer results in a space between the nickel layer and the passivation layer down to the bond pad;
applying an isotropic etchant selective for nickel to the nickel layer to widen the space between the nickel layer and the passivation layer down to the bond pad; and
depositing a palladium layer on the nickel layer and in the space so as to be in contact, in the space, with the bond pad, the passivation layer, and the nickel layer.



119. On information and belief, , the Accused Products are manufactured using a process that deposits a palladium layer on the nickel layer and in the space so as to be in contact, in the space, with the bond pad, the passivation layer, and the nickel layer.

1. A method for forming over pad metallization (OPM) on a semiconductor die having a bond pad in which the bond pad has an inner portion surrounded by a passivation layer, comprising:
depositing a nickel layer on the bond pad, wherein a lack of adhesion between the nickel layer and the passivation layer results in a space between the nickel layer and the passivation layer down to the bond pad;
applying an isotropic etchant selective for nickel to the nickel layer to widen the space between the nickel layer and the passivation layer down to the bond pad; and
depositing a palladium layer on the nickel layer and in the space so as to be in contact, in the space, with the bond pad, the passivation layer, and the nickel layer.



120. Fact and expert discovery are expected to confirm that the Accused Products infringe the '713 Patent, for which further evidence may lie in whole or in part in technical documents to which Chip Packaging does not presently have access.

121. Further, on information and belief, Defendant has and continues to indirectly infringe one or more claims of the ’713 Patent, including claim 1, by knowingly and intentionally inducing others, including third-party semiconductor foundries, other types of third-party manufacturers, customers, and/or end-users to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

122. Defendant, with knowledge that these products, and/or the manufacture thereof, infringe the ’713 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce direct infringement of the ’713 Patent by contracting for the third-party manufacture of, and/or providing the Accused Products to direct infringers.

123. Defendant has induced infringement by others, including third-party semiconductor foundries, other types of third-party manufacturers, customers, and/or end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others infringe the ’713 Patent, but while remaining willfully blind to the infringement.

124. Defendant has and continues to infringe one or more claims of the ’713 Patent by importing into the United States or offering to sell, selling, or using within the United States a product which is made by a process patented in the United States.

125. Defendant is not licensed or otherwise authorized to practice the claims of the ’713 Patent.

126. Thus, by its acts, Defendant has injured Chip Packaging and is liable to Chip Packaging for directly and/or indirectly infringing one or more claims of the ’713 Patent, whether literally or under the doctrine of equivalents, including without limitation claim 1.

127. As a result of Defendant's infringement of the '713 Patent, Chip Packaging has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for Defendant's infringement, but in no event less than a reasonable royalty with interest and costs.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff prays for judgment and seeks relief from Defendant as follows:

a. For judgment that Defendant has infringed and continues to infringe the claims of the '299,'646, '611, '351, and '713 Patents;

b. For an accounting of all damages sustained by Plaintiff as a result of Defendant's acts of infringement;

c. For a mandatory future royalty payable by Defendant in relation to each sale of an Accused Product that is found to infringe one or more of the Asserted Patents and all future products which are not colorably different from products found to infringe;

d. For a judgment and order requiring Defendant to pay Plaintiff's damages, costs, expenses, and pre- and post-judgment interest for its infringement of the '299,'646, '611, '351, and '713 Patents as provided under 35 U.S.C. § 284;

e. For a judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to Plaintiff its reasonable attorneys' fees; and

f. For such other and further relief in law and in equity as the Court may deem just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Plaintiff demands a trial by jury in this action for all issues triable by a jury.

Dated: February 6, 2025

Respectfully Submitted,

/s/ Garland Stephens by permission Andrea L. Fair
Garland Stephens (Texas Bar No. 24053910)
garland@bluepeak.law
Justin Constant (Texas Bar No. 24067551)
justin@bluepeak.law
Robert Magee
robert@bluepeak.law
Richard Koehl (Texas Bar No. 24115754)
richard@bluepeak.law
Anna Dwyer
anna@bluepeak.law
Kate Falkenstien
kate@bluepeak.law
Heng Gong (*pro hac vice*)
heng@bluepeak.law
BLUE PEAK LAW GROUP LLP
3139 West Holcombe Blvd.
PMB 8160
Houston, TX 77025
Tel: (281) 972-3036

Of Counsel:

Charles Everingham IV
State Bar No. 00787447
chad@millerfairhenry.com
Andrea L. Fair
State Bar No. 24078488
andrea@millerfairhenry.com
MILLER FAIR HENRY, PLLC
1507 Bill Owens Parkway
Longview, Texas 75604
(903) 757-6400 (telephone)
(903) 757-2323 (facsimile)

ATTORNEYS FOR PLAINTIFF